TIM CHIP
V1016

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TIM_V2 board
TIM chip version: V1016

1 UPDATE Notes

V1016: TIM_STATUS has been moved to address …50
New SM_STATUS shows the status of the ROP-state machine.
COMMAND_PULSE can be read back, but still when setting a bit to = '1' a pulse will be generated.
VHDL: VME readout mux is implemented with 'ELSIF' structure.

V1015: Software not changed. Status register bits: unused bits connected because Precision Connected them incorrectly.

Precision: 'FrontEnd_2004' Compiler option selected ➔ seems to more reliable result.

V1014: Software not changed.
Circuit for dis_vdoo (VME data out) changed so that the register value only is presented while driver is open.
tim_vme_regs, signal_merger :
CASE statements replaced by 'WITH xxx SELECT yyyy <= aa WHEN "dddd", …

V1013: Software not changed.
Circuit for vme_dis_rd, vme_enn simplified to be as in V1010 Version.

V1012: For software V1012 is nearly identical to V1011.
TESTMASK4: bit 13: nreset_ttc // RESET_TIM(low active signal) ➔ RESET_B

V1011: BCRES_FLAG =1 shows selected external BCRES arrives every orbit

EVRES by VME cmd pulse is again possible.
New power up value for TIM_COMMAND_REG is set for DTTF
New register: DLY_TCS_ECL // defines delay of ORBIT_X for TCS
RES_TIM of the VME chip is inverted & transmitted as RESET_B to TTCrq module.
TESTMASK1: reassigned bit

V1010:
LOCKED_TIM <= DCM_LOCKED and CLK40 so that 'locked' goes off with missing clock signal
All other logic as in V1009.

V1009: New Test Point assignment to check Bgo signals from TCS.
Selection for 'Event Cntr Reset' has been simplified. See TIM_COMMAND Register.
TIM_STATUS: DISCONNECTED overwrites errors and all other states

V1008: Same Registers and functions as in V1007.
ROBUS, L1A, BCRES, L1RES signals are sent now with inverted clock40 to the backplane. As already in previous versions the signals from the TTCrx chip are stored also with the inverted clock40.

V1007: Design done with FPGA-Advantage software from Mentor Graphics.

2 TTCrx signals from TTCrq or TTCrm mezzanine board

Clock: Clock 40Des1 is used as TTC clock until QPLL is working.
Clock 40, Clock 40Des2 are connected to TIM chip but not used
Channel A: L1Accept
Channel B: Bgo commands
Broadcast Data Interface: Brcst[7:2], EvCntRes, BCntRes; BrcstStr1, BrcstStr2;
Data Interface: Dout[7:0], SubAddr[7:0], DQ[3:0], DoutStr
Counter Interface: BCnt[11:0], EvCntHStr, EvCntLStr, BCntStrb
Internal Registers:
BCcntr 12 bits, EvCntr 24 bit...reset by broadcast Reset

Signals used in TIM chip:
SINERRSTR, DBERRSTR, … TTCrx errors
BR_CST(5:2), BRCST_STR1 …to receive Bgo commands
L1ACCEPT, BCNTRES, EVCNTRES, TTCREADY

V1011:
RES_TIM of the VME chip is inverted & transmitted as RESET_B to reset the TTCrx chip on the TTCrq mezzanine board.
Reason: While TTCrx is being reset, the 40 MHz clock is stopped and the TIM_chip cannot run.

3 DELAYS for BCRES, L1A

Min. Latency from TIM chip input to TIM chip output: VHDL Simulation
ORBITX (rising/leading edge)➔ bcres_l/r: 5.5bx ? (output of TIM chip)
BCNTRES(ttcrx) ➔ bcres_l/r: 5.5bx (output of TIM chip)
L1A_X (LEMO) ➔ l1a_l/r: 3.5 bx = 75 + 12.5 ns
L1ACCEPT (TTCrq) ➔ l1a_l/r: 3.5 bx = 75 + 12.5 ns

Remark1:
The BCRES signal from the BC-counter is delayed by 2bx before being sent to the backplane, so that that the L1A and Bgo Signals generated in the BC-table address=0 are sent concurrently with the BCRES signal.

Remark2:

Condition:Delays for ORBITX are set to the same values for the TIM and the TCS board.
➔ When using the ORBITX the BCRES signal to the TCS board is sent 2 bx earlier than to all other boards. Therefore the BC-table in the TIM and TCS board run concurrently.

4 Front Panel

4.1 LEDs driven by tim_chips

L1A_LED: Every L1A signal fires the L1A_LED for 1.4 ms.
TTC_ERR: Every single and double bit error of the TTCrx chip flashes the TTC_ERR LED

4.2 LEMO

See tim6u_module.pdf

5 Backplane Signals

5.1 Encoded Control Signals to other boards (DTTF+GT)

L1A could arrive concurrently with BCRES. Other BGO commands are never sent concurrently with L1A or BCRES and can be coded.
Agreement 20. Oct 03 with J. Eroe:
Therefore the encoding shown in table below is implemented in TIM chip versions V1004, V1005, V1007 to send 5 BGO commands via 3 signal lines to the DTTF/GT boards.
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L1A	BCRES	L1RES	Command
0	0	1	L1RES /RESET/RESYNC
0	1	0	BCRES
0	1	1	EVENT CNTR RESET
1	0	0	L1A
1	0	1	GO/STOP *
1	1	0	Concurrent L1A , BCR
1	1	1	ORBIT CNTR RESET

Table 1 Encoded L1A and BGO commands

- The GO/STOP command forces an inactive circuit into the RUN state and a data taking circuit into the STOP state. The L1RES signal forces the circuit always into the stop-state.
- L1A and GO/STOP should never appear at the same time. The L1A should be inhibited before sending a STOP command.

Remarks:
The other BGO commands (Test_EN, Private_GAP, Private_Orbit, HardRes) are not used in DTTF. DTTF sends calibration events like any other events during data taking runs. The calibration events are flagged in the data records.
DTTF and GT ignore Private Gaps and Orbits and also ‘private’ BGO commands.
It is assumed that no ‘official’ BGO cmds are sent during Private Gaps and Orbits.
The TIM chip always forwards L1A signals (=new in V1007).

5.2 RO-BUS signals (GT crate)

In the GlobalTrigger Crate the TIM board a 16 bit bus carries various slow control signals to all boards. Bits 6 to 0 carry decoded Bgo commands and bits 12-8 carry the original 4 bit Bgo bits with the strobe signal. Bits 7 and 13 are not used.

Normally the boards use only the encoded control signals as described above. But if required the full set of Bgo commands can be used in the GT crate.

ROBUS bits ------

-- robus is not used except bits 5 and 6
-- robus 15: rdqst // = OR of strobes
-- robus 14: test_strobe
-- robus 13: 0 //(previous MON_RQST_STROBE)
-- robus 12: BGO_STROBE
-- robus 11: BGO_3
-- robus 10: BGO_2
-- robus 9: BGO_1
-- robus 8: BGO_0
-- robus 7: 0 // reserved for other BGo command
-- robus 6: STOP_RUN <== used here
-- robus 5: START_RUN <== used here
-- robus 4: RES_ORBITNR
-- robus 3: HARD_RES
-- robus 2: PRIVATE_ORBIT
-- robus 1: PRIVATE_GAP
-- robus 0: TEST_EN

BGO commands:

0001 = 1 BC0	0010 = 2 Test Enable
0011 = 3 Private Gap	0100 = 4 Private Orbit
0101 = 5 Resync/L1Reset	0110 = 6 Hard Reset
0111 = 7 Reset Event Counter	1000 = 8 Reset Orbit Counter
1001 = 9 Start Run	1010 = A Stop Run

5.3 GT crate signals

In the GT crate on each card a PLL clock driver chip regenerates the clock signal and broadcasts it to all chips on the board with a maximum phase difference of less than 1 ns. The PLL circuits are synchronised 40ms after the start of the clock signal. A 40 MHz on board oscillator can be used instead of the TTC clock for stand-alone tests.

5.3.1 Signals between TIM and TCS board (GT crate)

8 TCS to TIM signals

bit 15: **L1A_from_TCS** → **used by GT**
bit 14, 13 not used
bit 12-8: **BGO_from_TCS(3:0)** → **used by GT**

8 TIM to TCS signals

bit 7-0: (L1Res…as dummy signal)

5.3.2 Signals between TIM and FDL board (GT crate)

8 FDL to TIM signals

bit 15-8: not used

8 TIM to FDL signals

bit 7-4: (L1Res…as dummy signal)
bit 3-0: **TIM_STATUS** (ready, warning,….) to be combined with other status bits on the FDL board.The result goes as GT_status to the TCS board.

5.3.3 Signals between TIM and GTFE board (GT crate)

1 GTFE to TIM signal

bit1: GTFE_READY = not used; Control function is done by the TCS board

1 TIM to GTFE signal
bit0: (L1Res…as dummy signal)

6 Definition of Left-Right Slots in the GT_9U crate

SLOT #	**BOARD NAME**		**TIM register**	**Alternative delay**	**Remark**
5	L1AOUT_1		DLY_L9		
6	L1AOUT_2		DLY_L8		
7	TCS		DLY_L7	DLY_TCS_ECL	**JMP DTFF=0**
8	empty		---		
9	PSB_T		DLY_L6		
10	FDL		DLY_L5		
11	GTL_1		DLY_L4		
12	GTL_2		DLY_L3		
13	PSB_1 (GTL)		DLY_L2		
14	PSB_2 (GTL)		DLY_L1		
15	PSB_3 (GTL)		DLY_R1		
16	TIM		---		
17	GTFE		DLY_R2		
18	GMT		DLY_R3		
19	PSB_4 (GMT)		DLY_R4		
20	PSB_5 (GMT)		DLY_R5		
21	PSB_6 (GMT)		DLY_R6		
--	Not used		DLY_R7		
--	Not used		DLY_R8		

7 Definition of Left-Right Slots in the DTTF crate

DTTF Backplane Version 3

SLOT#	DDTF#	BOARD Name	TIM register	
2		CSC_TRANS_AN	-	
3	15	PHTF_A_N2	DLY_L8	
4	13	PHTF_A_N1	DLY_L7	
5	11	PHTF_A_N0	DLY_L6	
6	9	ETTF - A	DLY_L5	
7	7	WS - A	DLY_L4	
8	5	PHTF_A_P0	DLY_L3	
9	3	PHTF_A_P1	DLY_L2	
10	1	PHTF_A_P2	DLY_L1	
11	-	CSC_TRANS_AP_BN	-	
12	16 to DAQ	TIM + DAQ	DLY_L9	
13	0	PHTF_B_N2	DLY_R1	
14	2	PHTF_B_N1	DLY_R2	
15	4	PHTF_B_N0	DLY_R3	
16	6	ETTF - B	DLY_R4	
17	8	WS - B	DLY_R5	
18	10	PHTF_B_P0	DLY_R6	
19	12	PHTF_B_P1	DLY_R7	
20	14	PHTF_B_P2	DLY_R8	
21		CSC_TRANS_BP	-	

8 ROP for test records to GTFE

A readout processor ROP has been implemented for tests that sends a test record to the GTFE board. The data values are fixed; only the BC-nr and the Event-nr. are inserted correctly.
8000 = IDLE the state machine is idle and waits for a L1A signal.
4000 = ERROR The FIFO that stores the BC-nrs of the L1A is full.
L1A signals are accepted only when a data taking run has been started (RUN_FF =1).
The commands 'L1Reset/Resync' command and 'Reset Eventnumber' are accepted before and after an event transfer.

9 VME addresses

A31 .....A24	A23 …A20	A19	A18		*Address Modes*
BASE ADDRESS_GT	xxxx	x	x		*Extended Base address*
xxxx xxxx not available	BASE ADDRESS_DTTF				*Standard Base address*

	A17	A16	A15…12	A11...8	A7...4	A3...A1, x
TIM chip	**0**	**1**	**a a a a**	**a a a a**	**a a a a**	**a a a 0**
registers	**0**	**1**	**0x**	**0x**	**00 –6E**	
~~TTCrxdump~~	**0**	**1**	**0x**	**0x**	**80 – 9E**	
Free space	**0**	**1**	**0x**	**0x**	**A0 – FE**	
Free space	**0**	**1**	**0x**	**100 – 1FFE**		
BC-Table 4k W16	**0**	**1**	**2000 – 3FFE**			
~~RING BUFFER 1k W16~~	**0**	**1**	**4000 – 47FE**			
free nn k W16	**0**	**1**	**4800 – FFFE**			
Free space	*2 0000 – 3 FFFE*					

9.1 Overview VME addresses

---1 0000	DLY_L1	w/r
---1 0002	DLY_R1	w/r
---1 0004	DLY_L2	w/r
---1 0006	DLY_R2	w/r
---1 0008	DLY_L3	w/r
---1 000A	DLY_R3	w/r
---1 000C	DLY_L4	w/r
---1 000E	DLY_R4	w/r
---1 0010	DLY_L5	w/r
---1 0012	DLY_R5	w/r
---1 0014	DLY_L6	w/r
---1 0016	DLY_R6	w/r
---1 0018	DLY_L7	w/r
---1 001A	DLY_R7	w/r
---1 001C	DLY_L8	w/r
---1 001E	DLY_R8	w/r

---1 0020	DLY_L9	w/r	
---1 0022	DIS_BOARDS	w/r	
---1 0024	DLY_TIM	w/r	
---1 0026	DLY_PAN	w/r	
---1 0028	DLY_CRATE_TTC	w/r	
---1 002A	DLY_CRATE_ECL	w/r	
---1 002C	DLY_TCS_ECL	w/r	
---1 002E	dummy_2e	w/r	without function
---1 0030	TRIG_PERIOD	w/r	
---1 0032	BGO_PERIOD	w/r	
---1 0034	**ORBIT_LENGTH_1**	w/r	-
---1 0036	TTC SUBADDRESS	w/r	exists but not used
---1 0038	COMMAND PULSE	w/-	
~~---1 0038~~	~~STATUS Register~~	~~-/r~~	removed since V1016
---1 003A	COMMAND Register	w/r	
---1 003C	ROCMD_REG	w/r	
---1 003E	DLY_L1A_TCS	w/r	
---1 0040	**TESTMASK1**	w/r	
---1 0042	**TESTMASK2**	w/r	
---1 0044	**TESTMASK3**	w/r	
---1 0046	**TESTMASK4**	w/r	
---1 0048	TESTDATA	w/r	
---1 004A	**TTCrx_ ERRORS**	-/r	
---1 004C	**L1A_ERRORS**	-/r	
---1 004E	**BC_ ERRORS**	-/r	
---1 0050	TIM_STATUS	-/r	since V1016
---1 0052	SM_STATUS	-/r	since V1016
---1 0054	**LAST_MAX_BCNR**	-/r	
---1 0056	xxxx	-/r	value=0000
---1 0058	xxxx	-/r	value=0000
---1 005A	xxxx	-/r	value=0000
---1 005C	xxxx	-/r	value=0000
---1 005E	xxxx	-/r	value=0000
---1 0060	**CHIP_ID_H**	-/r	
---1 0062	**CHIP_ID_L**	-/r	
---1 0064	**CHIP_ VERSION_H**	-/r	
---1 0066	**CHIP_ VERSION_L**	-/r	
---1 0068	DAY_MONTH	-/r	day+month as hex char's
---1 006a	YYEAR	-/r	year as hex char's
---1 006c	xxxx	-/r	value=0000
---1 006e	xxxx	-/r	value=0000

9.2 TIM chip registers

9.2.1 Delay Registers for boards on left and right side

- BCRES = 'Bunch Counter Reset' signal defines begin of a new LHC orbit
- L1A = 'Level 1 Accept' trigger signal to read an event.
- L1_RESET/RESYNC/RESET = various names for the signal to resynchronize the boards
- EVCNT_RES = resets the event counters after a resynchronization procedure.

- ORBIT CNTR_RESET = resets the orbit counter, normally done at begin of a new data taking run.
- GO/STOP = same signal for START and STOP command

L1A	BCRES	L1RES	Command
0	0	1	L1RES /RESET/RESYNC
0	1	0	BCRES
0	1	1	EVENT CNTR RESET
1	0	0	L1A
1	0	1	GO/STOP
1	1	0	Concurrent L1A , BCR
1	1	1	ORBIT CNTR RESET

Table 2 Encoded L1A and BGO commands

The TIM board sends the encoded signals to the other boards in the DTTF or GT crate. The delays for the signals are defined by the registers below. The register names DLY_Lx (L=left) and DLY_Rx (R=right) should indicate the position of the target boards relative to the TIM board. But see the tables for the implemented backplane wiring.
The total delay consists of (dly_H +1) + (dly_L +1). Each hex-number programs a 15bx delay circuit. The value 'F' means 'no delay'. The minimum delay 'FF' =0 bx and the maximum delay 'EE'=30 bx (=14+14+2).
POWER UP VALUES = X"FFFF" for all DLY_xx to get minimum delay.

Address A17-A0	**Register**	**D15–12, D11-8 L1A_dly**	**D7-4, D3-0 BCRES_dly**	**GT slot**	**DTTF slot**
1 0000	DLY_L1	dly_H, dly_L	dly_H, dly_L	14: PSB_2	10: PHTF_A_P2
1 0002	DLY_R1	dly_H, dly_L	dly_H, dly_L	15: PSB_3	13: PHTF_B_N2
1 0004	DLY_L2	dly_H, dly_L	dly_H, dly_L	13: PSB_1	9: PHTF_A_P1
1 0006	DLY_R2	dly_H, dly_L	dly_H, dly_L	17: GTFE	14: PHTF_B_N1
1 0008	DLY_L3	dly_H, dly_L	dly_H, dly_L	12: GTL2	8: PHTF_A_P0
1 000A	DLY_R3	dly_H, dly_L	dly_H, dly_L	18: GMT	15: PHTF_B_N0
1 000C	DLY_L4	dly_H, dly_L	dly_H, dly_L	11: GTL1	7: WS - A
1 000E	DLY_R4	dly_H, dly_L	dly_H, dly_L	19: PSB_4	16: ETTF - B
1 0010	DLY_L5	dly_H, dly_L	dly_H, dly_L	10: FDL	6: ETTF - A
1 0012	DLY_R5	dly_H, dly_L	dly_H, dly_L	20: PSB_5	17: WS - B
1 0014	DLY_L6	dly_H, dly_L	dly_H, dly_L	9: PSB_T	5: PHTF_A_N0
1 0016	DLY_R6	dly_H, dly_L	dly_H, dly_L	21: PSB_6	18: PHTF_B_P0
1 0018	DLY_L7	dly_H, dly_L	dly_H, dly_L	7: TCS	4: PHTF_A_N1
1 001A	DLY_R7	dly_H, dly_L	dly_H, dly_L	Not used	19: PHTF_B_P1
1 001C	DLY_L8	dly_H, dly_L	dly_H, dly_L	6: L1AOUT2	3: PHTF_A_N2
1 001E	DLY_R8	dly_H, dly_L	dly_H, dly_L	Not used	20: PHTF_B_P2
1 0020	DLY_L9	dly_H, dly_L	dly_H, dly_L	5: L1AOUT1	12: DAQ
1 0024	DLY_TIM	dly_H, dly_L	dly_H, dly_L	TIM chip: Channel Link ROP*	
1 0026	DLY_ PAN+	dly_H, dly_L	dly_H, dly_L	*Testpoints on TIM board*	

*) DLY_TIM used in V1011 again:

To delay the selected BCRES signal for the readout record indepently from the BC-counter that is used as address by the BC_TABLE.

+) DLY_PAN defines delays for signals RESET_PAN, BCRES_PAN and L1A_PAN that can be switched to TESTPOINT-LEMO connectors on front panel. See TESTMASK0…3 registers

9.2.2 DISABLE Boards in Crate

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0022	DIS_ BOARDS	L 8	R 8	L 7	R 7	L 6	R 6	L 5	R 5	L 4	R 4	L 3	R 3	L 2	R 2	L 1	R 1
	default values	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

EXAMPLE: BIT D14=1 disables board L(eft) 7

DIS_BOARD_L9: *See COMMAND register bit11 in 9.2.9.*

9.2.3 CRATE delays

GT-CRATE: Jumper is set to DTTF =0.

If the ORBIT ECL_signal is used as the bunch counter reset signal BCRES then the

- DLY_CRATE_ECL is used to adjust the GT crate to the LHC orbit and
- DLY_TCS_ECL provides a delayed BCRES signal for the TCS board, **but only when Jumper DTTF = 0.**

TEST mode:

If BCRES signal from the TTCrx chip is used then the adjustment is done either by programming the TTCrx chip or by programming the DLY_CRATE_TTC register.

DTTF-CRATE:

In DTTF crate normally the Bgo=0001 command is used to make a BCRES signal.

Total delay = 1 + delay[15:0].

Warning: The circuit uses a 16-bit counter and therefore the delay value has to be set smaller then 3564. Otherwise the previous BCRES will be suppressed.

Address A17-A1	Registername	D15 ……D0	Remarks
1 0028	DLY_CRATE_TTC	*value < 3564; default =0*	Used for tests
1 002A	DLY_CRATE_ECL	*value < 3564*	Used in GT crate
1 002C	DLY_TCS_ECL	*value < 3564*	**Used when Jumper DTTF=0**

9.2.4 DUMMY_2E

No function

Address A17-A1	Registername	D15 …….. D0
1 002C	DUMMY_2C	--

Without any function.

9.2.5 SIMULATION PERIODS

The registers define the time (unit=1 LHC orbit) between active orbits. During an active orbit simulated Trigger signals or BGO commands or UserMessages are sent according to the values in the BC-Table. If xx_PERIOD=0 then the messages are sent every orbit. See also chapter PERIODIC SIMULATION

Address A17-A1	Registername	D15 …… D0
1 0030	TRIG_PERIOD	*Period for L1A*
1 0032	BGO_PERIOD	*Period for Bgo signals and UserMessages*

9.2.6 OBIT LENGTH_1

Address A17-A1	Registername	D15-D12	D11 – D8	D7 – D4	D3 – D0
1 0034	ORBIT_ LENGTH_1	16 bit number			
	Default value Power-up	***0***	***D***	***E***	***B***

The ORBIT_LENGTH_1 defines the length of the LHC orbit. Default value =3564-1 (= 0DEB hex) bunch crossings. *The BC counters run from 0 until 3564 – 1=3563.* The orbit length is used to reset the bunch crossing counter if the BCRES signal is missing, for example when running without LHC signals in LHC orbit simulation mode.
The logic consists of a 16-bit counter+16 bit comparator. The upper 4 bits are always zero.
Check: The programmed BC LIMIT is compared against the content of the local BC-counter at the arrival time of the common BCRES signal. Any difference sets the error flag BAD_MAX_BC and increments the BC_ERRORS counter. *The reason for this error could be a bad clock signal or a bad BCRES signal.*

Remark: For Heavy Ion runs every 5th tick contains a bunch crossing.

9.2.7 TTC_Message_Subaddress register

V1007: TTC SUBADDRESS is not implemented!!

Address A17-A1	Registername	D15-D12	D11 – D8	D7 – D4	D3 – D0
1 0036	TTC SUBADDRESS	Last TTC Message *(read only)*		TTC Subaddress *(write/read)*	

- TTC Subaddress defines the address for individual addressed messages/commands. The command byte is stored in the last address ("…F") of the TTC_DUMP memory. See also chapter 9.3. Functions for individual messages are neither defined nor implemented.
- Last TTC Message contains the last system and user message code that has been received from the TTCrx chip.

9.2.8 COMMAND PULSE w/r

Set the COMMAND REGISTER bits before sending COMMAND PULSES (bit11…0)
Warning:
→ The VME instruction generates a pulse when a data bit is set equal 1. ←
Since V1016 this "register" can be read back.
The command bits 0…9 are used to simulate the corresponding BGo commands, which are received during data taking by the TTCrx link. See also CMD register 9.2.9. **The command pulses (bits 11 to 0) can be used only if the SELECT bits in the TIM_Command Register have been set before.**
HARD_RES_VME will stop in any case the BC-Table signal generation.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0038	COMMAND PULSE	*See description of bits below.*															
	default values	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

Bit 15, 14: **not used anymore**

V1011:

RES_TIM of the VME chip is inverted & transmitted as RESET_B to reset the TTCrx chip on the TTCrq mezzanine board.

Reason: While TTCrx is being reset, the 40 MHz clock is stopped and the TIM_chip cannot run.

Bit 13: not used

Bit 12: SEND_TESTDATA (GT only!)

SEND_TESTDATA =1 sends test data via RO-Bus to all GT boards.

See VHDL module: signal_merger

9.2.8.1 VME generated L1A

See VHDL module: signal_merger

Bit 11: L1A_VME

L1A _VME=1 simulates a L1A signal, *if SEL_L1A_[2:0]=000 has been set before.* The L1A signal is sent immediately to the GT-boards.

Bit 10: L1A_VME_SYNC

L1A _VME=1 simulates a L1A signal, if SEL_L1A_[2:0]=000 has been set and if a START_RUN_(VME) has been sent to set the RUN_FF=1.

The L1A signal is sent to the GT-boards according to the BC-Table content. For this test option only one L1A should be programmed into the BC-Table.

9.2.8.2 VME generated BGO commands

See VHDL module: signal_merger

Bit 9: DO_TEST_EN_VME^{+}) =1 run a calibration cycle.

Bit 8: DO_PRIV_GAP_VME^{+}) =1 run a private gap procedure

Bit 7: DO_PRIV_ORBIT_VME^{+}) =1 run a private orbit procedure

Bit 6: RES_ORBIT_VME^{+}) =1 sends a RESET ORBIT counter command

Bit 5: START_RUN_VME^{+}) =1 sets RUN_FF *+)

Bit 4: STOP_RUN_VME^{+}) =1 clears RUN_FF *+)

Bit 3: EVCNT_RES_VME *) =1 resets the Event Counter in all boards

Bit 2: L1RES_VME *) =1 sends a L1RESET to all boards (alias names RESET, RESYNC)

Bit 1: HARD_RES_VME^{+}) =1 sends 'HARD RES' (used by GTFE only) via ROBUS

Bit 0: BCRES_VME …not useful anymore because the BC-counter runs always regardless if an external BCRES signal arrives or not as soon as ORBIT_LENGTH_1 has been set correctly.

**) This command is also sent sent as a fast LVDS signal via the back-plane to all boards in the DTTF and GT crate.*

$^{+}$) *This command is sent via the back-plane RO-BUS to all boards in the GT crate; but not in the DTTF crate.*

*+) START_RUN and STOP_RUN send as a START/STOP as LVDS signals to all boards. IN GT crate better use the original signals on the ROBUS.

9.2.9 TIM_COMMAND Register

Set the COMMAND REGISTER bits before sending COMMAND PULSES.

Address A17-A1	Registername	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 003A	TIM COMMAND Register	*TIM status*						SEL_ EV RES		SEL_ BGO		SEL_ BCRES			SEL_ L1A		

	DTTF default	*1*	*0*	*0*	*0*	*0*	*1*	***1***	***1***	***0***	***1***	***1***	***0***	***0***	***0***	***0***	***1***
	GT default	*1*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*	*1*	*0*	*1*	*0*	*1*	*0*	*0*

POWER_UP value(DTTF): X"0361" Firmware is set for DTTF.
Software default value for GT: X"03D4"

Bit 15, 14: TIM STATUS for TCS

00 = TIM DISCONNECTED
10 = TIM_READY
01 = TIM_BUSY
11 = TIM DISCONNECTED

The programmed status is included into the TIM status code sent via the FDL to the TCS board. The TIM status can be overruled by error flags.

Bit 13: **not used anymore**

TTC_RDY_VME *The bit was used to* simulate a TTC_RDY status´.

Bit 12: not used anymore but still useful for a test of the TTCci board

CHECK_TTC_CHAIN

TIM always checks now if every L1A received directly from the TCS board has also been received via the optical TTC fiber. *The L1A_TCS_DLY delays the L1A sent by the TCS board over the backplane so that it arrives concurrently with the L1A sent via the TTC fiber. See also L1A_TCS_DLY register below. Any difference between both L1A signals increments the counter for L1A_ERRORS.*

Attention: The L1A_TCS_DLY value changes the local L1A latency in theGT crate when L1A from TCS is used (standard mode).

Bit 11: **DIS_BOARD_L9**

DIS_BOARD_L9 =1 stops timing signals to the L9 board. See also 9.2.2 for other boards.

Bit 10: **DIS_RO_BUS**

DIS_RO_BUS =1 disables the Readout Request bus (GT crate only).

SELECT 'EVENT COUNTER RESET'

Bit9: SEL_EVRES_1,
Bit8: SEL_EVRES_0

V1011: include vme cmd_pulse again as test option.
V1009 and later: When the special TTCrx signal is not selected the ‚event counter reset' is generated by the selected Bgo command source like any other Bgo command.

Code Bits 9-8	Selected source of EVENT COUNTER RESET command
00	Take EVENT COUNTER RESET from VME command pulse (bit 3) // = default after power-up
01	Take EVCNTRES signal of the TTCrx chip
10	Take EVENT COUNTER RESET from the active/selected BGO source
11	Take EVENT COUNTER RESET from the active/selected BGO source //== **default after power-up(DTTF) and for GT**

SELECT source of BGO commands

Bit7: SEL_BGO_1,
Bit6: SEL_BGO_0

Code Bits 7-6	Selected source of BGO commands
00	Only VME generated BGO commands are allowed.

01	BGO from TTCrx chip //== **default after power-up(DTTF)**
10	Periodic BGO internally generated
11	BGO from TCS board via back-plane //=software default for GT

The same selection is valid also for the 'USER MESSAGES', which are generated either periodically or by the TTC system.

SELECT BCRES
Bit5: SEL_BCRES_2
Bit4: SEL_BCRES_1
Bit3: SEL_BCRES_0

Code Bits 5-3	Selected source of BCRES signal
000	The VME command 'BCRES_VME' resets 1x the BC-counter
001	BCNTRES from TTCrx chip
010	ORBIT_X from Front Panel (ECL/NIM signal) //=software default for GT
011	**Not used anymore.**
100	**From BGO command decoder. // = default after power-up(DTTF)**
others	*Codes 101..111 inhibit all sources of BCRES*

V1010: BGo cmd=0001 is used again to make BCRES in the TIM chip. Necessary for DTTF crate.

The circuit consisting of the BC-Counter and a limit comparator always sends the 'end_of_orbit' as 'BCRES' signal via the backplane to the other boards in the crate. The signal that resets the BC-Counter either once or periodically comes from one of three possible sources. After power-up the BCNTRES of the TTCrx chip is selected as external source to generate the BCRES signal. It is required that the ORBIT_LENGTH has been loaded with the correct value.

SELECT L1A
Bit2: SEL_L1A_2
Bit1: SEL_L1A_1
Bit0: SEL_L1A_0

Code Bits 2-0	Selected source of L1A signal
000	Only VME command 'L1A_VME' is allowed. //
001	L1ACCEPT from TTCrx chip //= **default after power-up in DTTF**
010	L1A_X from Front Panel (ECL/NIM signal)
011	Periodic L1A internally generated using the BC-Table
100	L1A from TCS board via back-plane //=software default in GT crate
others	*Codes 101..111 inhibit all sources of L1A*

9.2.10 RO_CMD Register

This register is used in GT crate only.
The register contains the control bits to extract data on the TIM chip in case of a L1A.
This logicis not used.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 003C	ROCMD _REG	*See description of bits below.*															

	default values	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

Bit15-12: not used

Bit 11: **RO_LINK_ON =EN_CHLINK**

RO_LINK_ON=1 enables the Channel Link chip to allow transmission of data to the GTFE readout board.

Default = 0 because normally TIM data are not included into the event data.

V1007: The Channel Link sends counter data to the GTFE to test the hardware.

Bit10-9: **not used**

Bit 8: **EN_BC_CHECK =1** BC-errors are included into TIM_STATUS ➔ FDL➔TCS

Checks BC number at arrival time (=3563) of BCRES

➔ *Status bits: ERR_MAX_BC, BAD_MAX_BC*

Bit 7: **EN_TTC_CHECK=1**

Double bit errors and missing TTC_READY signal of TTCrx are included into TIM_STATUS ➔ FDL➔TCS

Bit 6: **not used** ~~**EN_EVNR_CHECK=1 …not implemented**~~

~~Compares with TTC EVnr with local Eventr~~

~~➔ *Status bits: ERR_LOCAL_EV, BAD_ LOCAL_EV*~~

Bit 5: **not used**

Bit 4: **not used**

Bit 3: **not used**

Bit 2: **not used**

Bit 1: **not used**

Bit 0: **not used**

9.2.11 Delay L1A from TCS Register

DTTF crate: DLY_L1A_TCS is not used.

The delayed L1A signal from the TCS board goes to the Signal Merger and is selected and distributed in the GT crate when the TTCrq is not used.

Attention: **The L1A_TCS_DLY value changes the local L1A latency in theGT crate when L1A from TCS is used (standard mode).**

The total delay consists of (DLY_L +1) + (DLY_H +1). Each hex-number programs a 16bx delay circuit. ***The value 'F' means 'no delay'***. The minimum delay 'FF' =0 bx and the maximum delay 'EE'=32 bx.

Address A17-A1	Registername	D15 .....D8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 003E	DLY_L1A_TCS	Not used	RES_DLY_H				RES_DLY_L			
V1011	Power_up value =default value	0 0	F				F			

Non standard mode in GT crate:

If the TTCrq is used in the GT crate to provide clk, bcres and Bgo commands the L1A_TCS_DLY can be used to compare the L1A signal from the TTCrq with the L1A received directly from the TCS board via the backplane.

The L1A_TCS_DLY delays the L1A from the TCS board so that it arrives concurrently with the L1A sent via the TTC fiber. See also bit 12 in the TIM_CMD register 9.2.9 above.

9.2.12 TESTMASK1

V1011

The TESTMASK1 register switches the signals below to the T1 LEMO output on the frontpanel and the testpoint TEST1 on the board. If a mask bit =1 the corresponding signal is connected. If more mask bits are set then the 'OR' of the signals will be monitored.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0040	TESTMASK1																

Power-up value: X"8000"

15:	**bcres_pan**	**// BCRES to this LEMO delayed by R9 register**
14:	l1a_bctable	// L1A generated by BC_table
13:	evcntres_ttc	// EVENT_CNTR_RESET from TTCrx
12:	bcres2cntr	//merged bcres going to BC-counter
11:	ORBITX	// converted ECL signal from front panel LEMO
10:	BCNTRES_TTC	// from TTCrx
9:	l1a_from_tcs	// L1A from TCS board
8:	vme_en	// VME access on TIM chip
7:	tp_inc_bcerr	// increments the BC-error counter
6:	bcres_lemo_tcs	// BCRES from LEMO delayed for TCS, after tcs_delay
5:	reset_r(3)	// L1_RESET to backplane to GT_slot18 resp DTTF_slot15
4:	reset_r(2)	// L1_RESET to backplane to GT_slot17 resp DTTF_slot14
3:	reset_r(1)	// L1_RESET to backplane to GT_slot15 resp DTTF_slot13
2:	bcres_r(3)	// BCRES to backplane to GT_slot18 resp DTTF_slot15
1:	bcres_r(2)	// BCRES to backplane to GT_slot17 resp DTTF_slot14
0:	bcres_r(1)	// BCRES to backplane to GT_slot15 resp DTTF_slot13

9.2.13 TESTMASK2

V1011…V1008

The TESTMASK1 register switches the signals below to the T2 LEMO output on the frontpanel and the testpoint TEST2 on the board. If a mask bit =1 the corresponding signal is connected. If more mask bits are set then the 'OR' of the signals will be monitored.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0042	TESTMASK2																

Power-up value: X"8000"

15:	**l1a_pan**	**// L1A to this LEMO delayed by R9 register**
14:	l1a_lemo	// from LEMO connector
13:	l1a_ttc	// L1A from TTCrq module
12:	bcres_bccntr	// from BC-counter
11:	bcres_lemo	// BCRES from LEMO delayed for GT-crate, after crate_delay
10:	bcres_ttc	// BCNTRES signal from TTCrx after DLY_CRATE_TTC
9:	l1a_tcs_dlyed	// L1A from TCS board after DLY_L1A_TCS (max 32 bx)
8:	vme_wr	// WRITE signal of VME access
7:	l1_reset_to_tim	// from selected, decoded Bgo to reset error flags in TIM chip
6:	tp_inc_ttcrx_err	// single & double bit errors increment ttcrx error counter
5:	l1a_l(3)	// L1A to backplane to GT_slot12 resp DTTF_slot8
4:	l1a_l(2)	// L1A to backplane to GT_slot13 resp DTTF_slot9
3:	l1a_l(1)	// L1A to backplane to GT_slot14 resp DTTF_slot10
2:	l1a_r(3)	// L1A to backplane to GT_slot18 resp DTTF_slot15
1:	l1a_r(2)	// L1A to backplane to GT_slot17 resp DTTF_slot14
0:	l1a_r(1)	// L1A to backplane to GT_slot15 resp DTTF_slot13

9.2.14 TESTMASK3

V1009 new assignments old IDLE_VALUE

The TESTMASK3 register switches the signals below to the testpoint TEST3 on the board. If a mask bit =1 the corresponding signal is connected. If more mask bits are set then the 'OR' of the signals will be monitored.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0044	TESTMASK3																

Power-up value: X"8000"

15: reset_pan // L1_RESET to TP3 switched by R9 register
14: ttc_rdy // TTC READY signal from TTCrx chip 1= running
13: l1a_from_tcs // L1A received from TCS board via wire tcs2tim(7)
12: l1a_to_led // selected internal L1A signal extended to 1.4 ms
11: dtack // internal DTACK signal of a VME access
10: wr_40_4e(2) // VME write access to register 44 = TESTMASK3
9: wr_20_3e(1) // VME write access to register 22 = DIS_BOARDS
8: wr_00_1e(0) // VME write access to register 00 = DLY_L1
7: end_of_orbit // =1 when bc-cntr = max_bc_nr, should be = selected ext. bcres
6: robus(6) // STOP_RUN … Bgo command
5: robus(5) // START_RUN
4: robus(4) // RES_ORBITNR
3: robus(3) // HARD_RES
2: robus(2) // PRIVATE_ORBIT
1: robus(1) // PRIVATE_GAP
0: robus(0) // TEST_EN

9.2.15 TESTMASK4

V1009 new assignments

The TESTMASK4 register switches the signals below to the testpoint TEST4 on the board. If a mask bit =1 the corresponding signal is connected. If more mask bits are set then the 'OR' of the signals will be monitored.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0044	TESTMASK4																

Power-up value: X"8000"

15: clk40 // 40MHz clock inside chip
14: dttf_board // Position of DTTF JUMPER on board: 1=DTTF crate, 0=GT-crate
13: nreset_ttc // =RESET_TIM from VME chip(low active) ➔ RESET_B to TTCrx
12: l1a_bctable // periodic L1A from BC_TABLE (bit 8) sent every n-th orbit
11: rd_60_6e(3) // VME read access to 66 = CHIP_ VERSION_L
10: rd_40_5e(2) // VME read access to 44 = TESTMASK3
9: rd_20_3e(12) // VME read access to 22 = TIM_STATUS_REG
8: rd_00_1e(0) // VME read access to 00 = DLY_L1
7: lock_bgo // signal inhibits Bgo commands from BC_TABLE
6: lock_l1a // signal inhibits L1A from BC_TABLE
5: en_bc_tab // VME access to the BC_TABLE

4: ro_rdrqst // =1 when sending a coded + decoded Bgo command to the RO_bus
3: tcs2tim(3) //= Bgo(3) from TCS
2: tcs2tim(2) //= Bgo(2) from TCS
1: tcs2tim(1) //= Bgo(1) from TCS
0: tcs2tim(0) //= Bgo(0) from TCS

9.2.16 TESTDATA Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0048	TESTDATA	*Test data for RO_RQST bus*															

Power-up value: X"1234"
Used by GT only. Write and read access.
Test data to be sent via the RO-RQST bus to the boards in the crate.
Write and read access.

9.2.17 TTCrx ERRORS

New in V1007

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 004A	TTCrx ERRORS	*Number of errors X"FFFF" = overflow*															

Read only access.
The register contains the number of single and double bit errors since the last read access. A read access first moves the actual content of the error counter into the register and clears then the counter. In case of many errors the counter stops at FFFF.

9.2.18 L1A_ERRORS

V1011: not useful in DTTF and not used in GT with BCRES_ECL
New in V1007.

Address A17-A1	Registername	D15 …….. D0
1 004C	L1A_ERRORS	*Number of errors*

Read only access.
Whenever the L1A signals from TCS and TTC disagree the error counter is incremented. A VME read access moves the actual counter content into a register and also clears the error counter. The counter stops counting at X"FFFF" to indicate an overflow.

9.2.19 BC_ERRORS

New in V1007.

Address A17-A1	Registername	D15 …….. D0
1 004E	BC_ERRORS	*Number of errors*

Read only access.
Whenever the selected external and the internal BCRES signals disagree the error counter is incremented. A VME read access moves the actual counter content into a register and also clears the error counter. The counter stops counting at X"FFFF" to indicate an overflow.

9.2.20 TIM_STATUS Register

Since V1016 on this address.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0

1 0050	TIM STATUS Register	*See description of bits below.*

Bit15 – 6 show the status of the TIM Readout circuits and used in the GT crate only.

Bit 15: =junk…**ignore this bit**

Bit 14: ROP ERROR //GT-crate only
FIFO overflow because too many L1A are waiting
Bit 13: ROP_FIFO_WARN //GT-crate only
The FIFO that buffers L1A signals has been filled to the warning level
Bit 12: ROP_FIFO_EMPTY //GT-crate only
The FIFO that buffers L1A signals is empty.
Bit 11 – 8: TIM_STATUS //GT -crate only
The status bits are transmitted via the FDL to the TCS Trigger Control board.
See also bits 15, 14 in TIM_COMMAND_REG where the status will be set to 'ready', 'busy' and 'disconnected'. Other states are set by the ROP logic when running.
-- 1100=error, 1000=ready, 0100=busy, 0010= out_of_sync, 0001=warning
-- 1111=disconnected (0000=disconnected)
Bit 7: EN_CHLINK //GT-crate only
1= switches on the Channel Link chip to transfer data to the GTFE board. This option is used only for tests in the GT crate.
Bit 6: **RUN_FF** is set and cleared by 'start run' and 'stop run' commands
Bit 5: L1A_ERR //GT -crate only
L1A from TCS and TTC did not agree since last reading the L1A-Error Counter. *Will not be useful anymore, when ECL clock and 'orbit' have are used in GT crate.*
Ignored when in DTTF crate.
Bit 4: **BCNTR_ERR**
=1 when the selected external BCRES and internal 'end_of_orbit' signals do not agree. The flag is cleared when reading the BC-Error Counter.
3 error reasons:

- The selected external BCRES signal is bad.
- The MAX_BCNR register contains a wrong value.
- The clock signal is not 40 MHz.

Bit 3: **BCRES_FLAG**
=1 when the selected external BCRES signal arrives every orbit
=0 when the BC counter runs without any external BCRES signal
Bit 2: **TTCRX_ERR**
1= There was a single or double bit error in the TTCrx chip since last reading the ttcrx error counter
Bit 1: **DBERR_TTCRX**
This bit shows the actual status of the double bit error signal in the TTCrx chip.
Bit 0: **TTC_READY**
TTC_READY=1: The TTCrx chip is working correctly. For the QPLL see VME chip.

9.2.21 SM_STATUS Register

Since V1016.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0052	SM STATUS Register	*See description of bits below.*															

STATE_MACHINE STATUS register shows the state of the readout processor ROP that sends a test record to the GTFE board. The data values are fixed; only the BC-nr and the Event-nr. are inserted correctly.
8000 = IDLE the state machine is idle and waits for a L1A signal.
4000 = ERROR The FIFO that stores the BC-nrs of the L1A is full.
L1A signals are accepted only when a data taking run has been started (RUN_FF =1).

9.2.22 NBAD_L1A_TTC Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0050	BAD_L1A_ TTC Register	*See description of bits below.*															

Read access only.

9.2.23 BCDIFF Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0052	BC_DIFF Register	*BC difference between local BC counter and TTCrx*															

Read access only. The register is used to check for hardware errors.

9.2.24 MAX_BCNR Register

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0054	MAX_ BCNR Register	*Maximum value of the Bunch Crossing Counter when the last external BCRES arrived.*															

Read access only. The register is used to check for hardware errors.

9.2.25 TTC_BCNR Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0056	TTC_BCNR Register	*Bunch counter number from TTCrx chip.*															

Read access only.

9.2.26 LOC_EVNR_H Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0058	LOC_EVNR _H Register	*High part of Local Event number*															

Read access only.

9.2.27 LOC_EVNR_L Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 005A	LOC_EVNR _L Register	*Low part of Local Event number*															

Read access only.

9.2.28 TTC_EVNRH Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 005C	TTC_EVNR H	*High part of Event number from the TTCrx chip*															

Read access only.

9.2.29 TTC_EVNRL Register

NOT IMPLEMENTED

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 005E	TTC_EVNR L	*Low part of Event number from the TTCrx chip*															

Read access only.

9.2.30 CHIP IDENTIFIER Registers

The DAQ group wants 32 bit identifiers for the chips. This address is reserved for that purpose. The bit format is preliminary.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0060	CHIP_ID_H	*chip type bits 31...16: =0001 for GT crate*															
1 0062	CHIP_ID_L	*chip type bits 15…0: =4211 /hardwired by design*															

Bits 15-12: = 4 for TIM card Bits 12 - 8: = 2 for TIM chip
Bits 7 - 4: = card# Bits 3 - 0: = 1 chip# *//There is only 1 TIM chip on board.*

9.2.31 CHIP VERSION Registers

Version numbers 1…1000(hex) are test designs.
Version numbers 1000…FFFF FFFF (hex) are standard designs.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0064	CHIP_ VERSION_H	*Version number bits 31…16 0000*															
1 0066	CHIP_ VERSION_L	*Version number bits 15…0 1007*															

Example: Version_1007: CHIP_VERSION_H = 0000; CHIP_VERSION_L = 1007

9.2.32 CHIP DATE Registers

Date is defined as hex. Characters.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0068	DAY_MONTH	*DAY*								*MONTH*							
1 0066	YYEAR	*YEAR*															

Example: Version_1007: 26 March 2006 ➔
DAY_MONTH = X"2603"; YYEAR = X"2006" = Hex Characters

9.3 TTC dump addresses

NOT IMPLEMENTED
The 16 addresses below contain the TTCrx registers of the last dump action. See also description of TTCvi module and of TTCrx chip.
Only lower 8 bits are used. Read access only.

Address A17-A1	Registername	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
1 0080	xxxx	----------								*xxxx*							
1 0082	xxxx	----------								*xxxx*							
1 0084	xxxx	----------								*xxxx*							
1 0086	xxxx	----------								*xxxx*							
1 0088	xxxx	----------								*xxxx*							
1 008A	xxxx	----------								*xxxx*							
1 008C	xxxx	----------								*xxxx*							
1 008E	xxxx	----------								*xxxx*							
1 0090	xxxx	----------								*xxxx*							
1 0092	xxxx	----------								*xxxx*							
1 0094	xxxx	----------								*xxxx*							
1 0096	xxxx	----------								*xxxx*							
1 0098	xxxx	----------								*xxxx*							
1 009A	xxxx	----------								*xxxx*							
1 009C	xxxx	----------								*xxxx*							
1 009E	xxxx	----------								*xxxx*							

9.4 BC – Table for Simulation

Address range: 1 2000 – 1 3FFE for 4k memory of BC table
The address corresponds to the bunch-crossing (BC) number. During Signal generation a BC-counter provides the read addresses. If a bit in the BC-Table is set to '1' at address 'aa' then a signal pulse will be sent at BC-number 'aa'. The signals are sent every n-th orbit as defined by the SIMULATION PERIOD register. Bits 15-8 are sent according to TRIG_PERIOD and bits 7-0 according to BGO_PERIOD.

Bit 15-12: free bits
Bit 11- 9: free bits
Bit 8: PER_L1A // sends a trigger to read event data; periodic simulation of L1A

Bit 7: free bit
Bit 6: free bit
Bit 5: free bit

Bit 4: PER_BGO_4 // simulate a BGO STROBE command
Bit 3: PER_BGO_3 // simulate bit3 of a BGO command
Bit 2: PER_BGO_2 // simulate bit2 of a BGO command
Bit 1: PER_BGO_1 // simulate bit1 of a BGO command
Bit 0: PER_BGO_0 // simulate bit0 of a BGO command

9.4.1 BGO codes

0000 = *not used*
0001 = *'BC0'…not used in TIM chip*
0010 = TEST_ENABLE
0011 = PRIVATE_GAP
0100 = PRIVATE_ORBIT
0101 = L1RESET (or RESYNC)
0110 = HARD_RESET
0111 = RESET_EVENT_COUNTER
1000 = RESET_ORBIT
1001 = START RUN
1010 = STOP RUN
1011…1111….*free for private purpose*

9.5 RING BUFFER 1k memory

NOT IMPLEMENTED
Address range: 0 4000 – 0 47FE for 1k memory of Ring buffer.
First set FREEZE_RIBUF=1 to stop any input data and set INHIB_L1A_ON_TIM=1 in the RO_CMD register to stop triggered readout. Then it is possible to access the Ring Buffer memory by VME.
To check external or simulated signals often just freeze the Ring Buffer and read data from all addresses.
INPUT bits for the Ring-buffer:
Bit15: L1A_FROM_TCS *// arrives via the back-plane from the TCS board*
Bit 14: L1A_FROM_TCS_DLYED *// check programmed delay*
Bit13: L1A_FROM_TTC *// Bit 13 and 14 should appear at the same time*
// if the delay for L1A_TCS is set correctly.
Bit12: L1A_FROM_LEMO *// External trigger input*
Bit11: PER_MONRQST *// simulated periodic Monitoring Request*
Bit10: PER_L1A *// simulated periodic L1A*
Bit 9: 0 *// not used*
Bit 8: RES_EVCNT *// RESET Event Counter generated by any source*
Bit 7: ORBIT_P *// Pulse at begin of ORBIT signal (LEMO, ECL)*
Bit 6: BCRES_LEMO *// Delayed BCRES from Orbit signal*
Bit 5: BCNT_RES_TTC *// Bunch Counter Reset from TTC*
Bit 4: BCRES_TTC *// Bunch Counter Reset from TTC after optional delay*
// BCRES_LEMO and BCRES_TTC should appear at the
// same time if both are connected.
Bit 3: L1_RESET *// generated by any source*
Bit 2: PRIV_ORBIT *// generated by System Message or any BGO command*
Bit 1: PRIV_GAP *// generated by System Message or any BGO command*
Bit 0: TEST_EN *// generated by System Message or any BGO command*

10 FAQ

10.1 Channel Link records to GTFE (GT crate)

10.1.1 Test without TCS board

- Select sources for CLOCK, L1A, BCRES, Reset_EventNr and other Bgo-commands.
  - Set register TIM_CMD: X”8000” :
    tim_ready =1 RES_EVNR: fromVME,
    Bgo: from VME; BCRES: stand alone L1A: fromVME
- Set DLY_TIM to get correct value for BCnr in the record
- Start Run:
  TIM_CMD_PULSE bit 5: START_RUN_VME =1 sets RUN_FF to allow the ROP state machine to transmitted records with every L1A signal.
- Send L1_RESET
  TIM_CMD_PULSE bit 2: L1RES_VME =1 resets flags at begin in all boards..
- Reset Event Counter
  TIM_CMD_PULSE bit3: EVCNT_RES_VME =1 the Event Counter in all boards.
- Now send several L1A signals with:
  TIM_CMD_PULSE bit11: L1A_VME =1
- Finally stop run:
  TIM_CMD_PULSE bit4: STOP_RUN_VME =1 clears RUN_FF and inhibits the rop_state machine in the TIM chip.

10.1.2 Test with TCS board

- Select sources for CLOCK, L1A, BCRES, Reset_EventNr and other Bgo-commands.
  - Set register TIM_CMD: X”83D4” :
    tim_ready =1 RES_EVNR: selected Bgo,
    Bgo: from TCS; BCRES: from ORBIT_X(LEMO) L1A: fromTCS
- Set DLY_TIM to get correct value for BCnr in the record
- **In TCS board:**
  - Start Run of the PTC to which the GT is connected.
    ➔ L1_RESET is sent automatically
    ➔ RESET EVENT COUNTER is sent automatically
- Now send several L1A signals from the TCS or
  set TIM_CMD: X”83D0” to send single L1A by VME
  (TIM_CMD_PULSE bit11: L1A_VME =1)

10.1.3 Remarks

- The Event Number can be cleared also during the RUN.
- When RUN is stopped the TIM chip will not send any trigger and the FIFO might become full. Therefore clear the FIFO with a L1RESET before starting a new RUN.
- If the TIM_STATUS bit7=1 = rop_error the rop_state machine does not work anymore and needs a L1RESET to return to the initial state.

10.1.4 TIM record of V1011

The IDLE code and the last EOR word X"F00FFFF" are not written into the GTFE.
The EOF is needed to tell GTFE that an event has been transmitted.

```
--Assign values for TIM record
  idle_code  <= X"555AAAA";
  tim_rec(0) <= X"A00" & ev_cntr(15 downto 0);    -- Event number L
  tim_rec(1) <= X"B0000" & ev_cntr(23 downto 16); -- Event number H
```

```
tim_rec(2) <= X"C00" & bc_nr;                -- BC_number of L1A
tim_rec(3) <= X"D00ADAD";      -- board ID = ADAD
tim_rec(4) <= X"1001111";      -- send all 16 values
tim_rec(5) <= X"1002222";
tim_rec(6) <= X"1003333";
tim_rec(7) <= X"1004444";
tim_rec(8) <= X"1005555";
tim_rec(9) <= X"1006666";
tim_rec(10) <= X"1007777";
tim_rec(11) <= X"1008888";
tim_rec(12) <= X"1009999";
tim_rec(13) <= X"100AAAA";
tim_rec(14) <= X"100BBBB";
tim_rec(15) <= X"100CCCC";
tim_rec(16) <= X"100DDDD";
tim_rec(17) <= X"100EEEE";
tim_rec(18) <= X"100FFFF";
tim_rec(19) <= X"1000000";
tim_rec(20) <= X"E003210";   -- Last W64 with 'E'
tim_rec(21) <= X"E007654";
tim_rec(22) <= X"E00BA98";
tim_rec(23) <= X"E00FEDC";
tim_rec(24) <= X"F00FFFF";   -- End of record
```

11 BGo commands in TIM

11.1 Start/Stop

'Start' sets a RUN_FF and 'Stop' clears it. The RUN_FF allows to send a Channel Link record to the GTFE board with every L1A.

11.2 L1_RESET in TIM chip

- The selected 'L1_Reset' in
  - **rop_tim** (Channel Link state machine)
    - moves the State Machine into the initial state & clears error flag,
    - clears the FIFO but
    - does not clear the Even counter(!).
  - **check_bc_l1a**: clears error flags but not the error counters
  - **fdl_tcs_tim**: sent as dummy signal to fdl, tcs boards

11.3 Reset Eventnr

- The selected 'Reset Eventnumber' in
  - **rop_tim** (Channel Link state machine)
    - clears the FIFO and
    - resets the Event Counter.

The selected 'Reset Eventnumber' is acknowledged at the end of a record transmission.

12 RESET trees

The L1_RESET signal is forwarded to all boards in the VME crate. HARD_RES is not used. L1_RESET goes also to the TIM chip logic and clears Erroflags but no other register. Both reset signals are generated either by software (VME) or by BGo signals arriving from the

TCS (Trigger Control System) via the TTC optical link or by Message signals from the TTC link or are simulated periodically by the BC Table

12.1 HARD_RES

Signal sources:
- HARD_RES_VME *(software)*
- HARDRES_MSG: r*eceived as MESSAGE bits from TTC*
- HARDRES_BGO:
  - TCS_BGO: BGO signals received from TCS via TTC links
  - PER_BGO: BGO signals simulated by the BC-TABLE inside the TIM chip

Functions:
  - HARD_RES is not used in the TIM board

12.2 L1_RESET

Signal sources:
- L1RES_VME *(software)*
- L1RES_MSG: *received as MESSAGE bits from TTC*
- L1RES_BGO:
  - TCS_BGO: BGO signals received from TCS via TTC links
  - PER_BGO: BGO signals simulated by the BC-TABLE inside the TIM chip

Functions:
- L1_RESET resets/resynchronizes all boards in the VME crate.

12.3 RESET_DCM_TIM

Resynchronizes the clock inside the TIM chip and also sets all registers to their initial values.

12.4 RESET_TIM

..clears all registers in the TIM chip.

12.5 INACTIVE

... keeps all IO pins in HIGH-Z state.

12.6 STOP_RUN

- STOP_RUN also clears TEST_ENABLE FF

13 Chip Design

Compatibility Problems with TIM6U:
- INACTIVE signal is not connected in TIM6U prototype board
- L1A_LED and TTC_ERR might have wrong polarity for TIM6U.

PRECISION finds not, but ISE finds time constraints for CLR.

Tim_chip_area_report : 268 ports, 266 IO, 262 registers mapped ??
268 io are in listing: 16 iobuf + 150 obuf + 100 ibuf + 2 ibufg = 268

No INFF:
CE for INFF: BCNTSTR, DOUT_STR,
IBUFG: CLK_FB, CLOCK40DES1
IBUF: INACTIVE, RESET_TIM, RESET_DCM_TIM,

No OUTFF:
OBUF: CLK_LOCKED, CLK0_FOR_FB, CLK_TIM, CLK_TIM_LEMO,

NDTACK_TIM, NBERR_TIM, NIRQ_FR_TIM, RO_CLK, TEST_T4 (clk40 output)
Fixed Value: NEN_TIMFDL(1:0), NEN_TIMTCS(1:0), NIRQ_FR_TIM, RO_DAT(27:24), STROB(1),
Problem: NBERR_TIM has OUTFF with INIT=1

14 Pin assignment TIM chip

The TIMING chip is a FPGA from XILINX, called XC2V1000-4FG456C. There is an EXCEL-file containing the pin assignment of the TIM CHIP (see tim_chip.xls). The pintable is extracted from the XILINX datasheet of the FG456-package (ds031-4.pdf). (Extraction was done using Acrobat Reader 4.0 with ***Zusatzmodule/ACE*** enabled or using Acrobat4. Select the table that should be extracted and use right-mouse-button ***Extract Table.*** Save it as text file. Start EXCEL , open the text file and convert it. Do the same for each page.
The batch-file ..*tim_check**make_pin_nr_tim_chip.bat* provides a possibility "**to make" pin-numbers** of symbols in VIEWDRAW from the EXCEL-file.
The batch-file ..*tim_check**check_symbol_tim_chip.bat* provides a possibility "**to compare" pin-numbers** of symbols and the EXCEL-file (text-file of EXCEL-sheet). The comparision output is written into the file ..*tim_check**tim_check_symbol.log*