Declarations

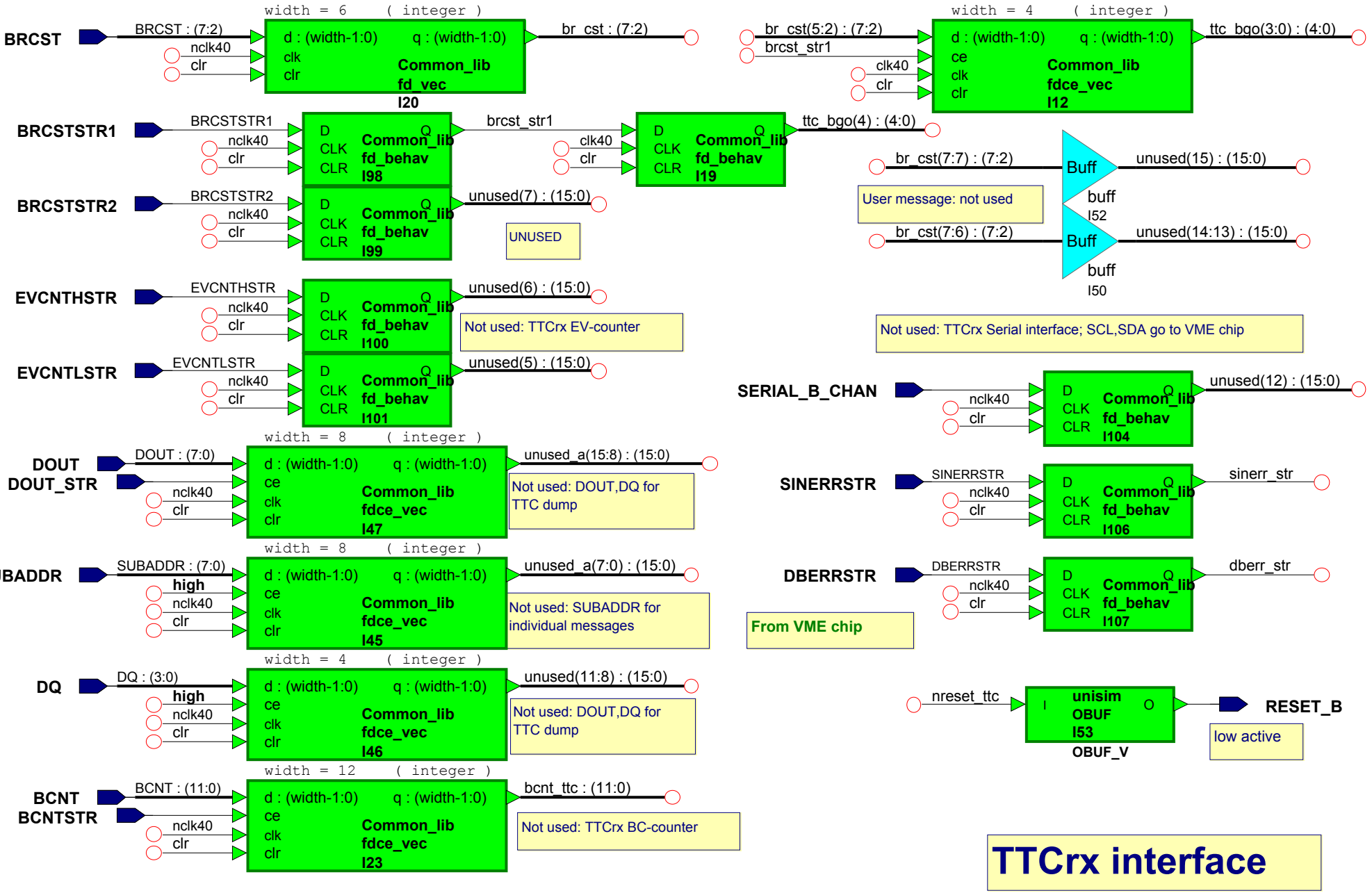
Ports:

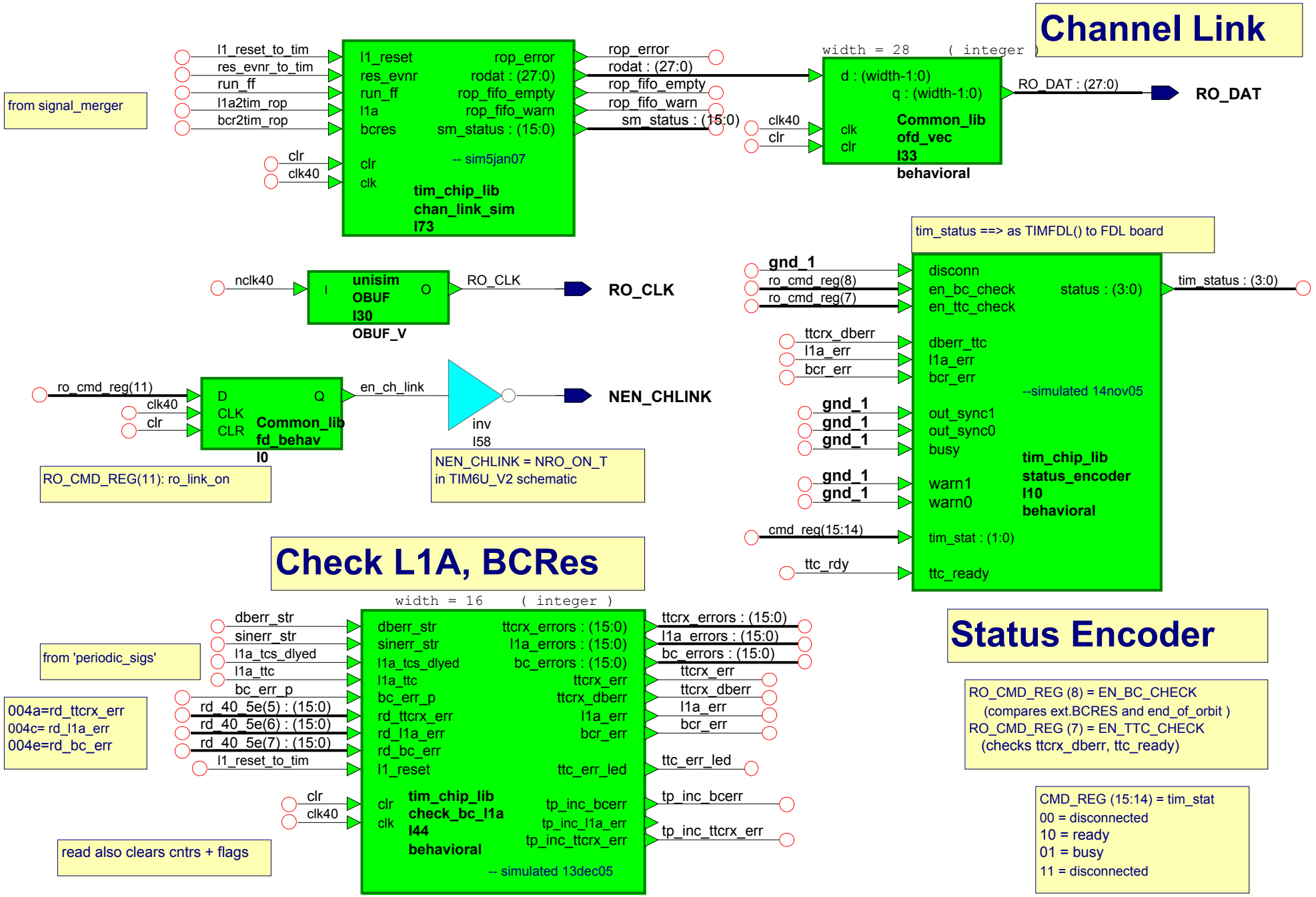
```
    ADDR             : std_logic_VECTOR(19 DOWNTO 1)
    BCNT             : std_logic_vector(11 DOWNTO 0)
    BCNTRES          : std_logic
    BCNTSTR          : std_logic
    BRCST            : std_logic_vector(7 DOWNTO 2)
    BRCSTSTR1        : std_logic
    BRCSTSTR2        : std_logic
    CLK_FB           : std_logic
    CLK_LOCAL        : std_logic
    CLOCK40          : std_logic
    CLOCK40DES1      : std_logic
    CLOCK40DES2      : std_logic
    CLOCKL1ACCEPT    : std_logic
    DBERRSTR         : std_logic
    DOUT             : std_logic_vector(7 DOWNTO 0)
    DOUT_STR         : std_logic
    DQ               : std_logic_vector(3 DOWNTO 0)
    DTTF_MODE        : std_logic
    EN_TIM           : std_logic
    EVCNTHSTR        : std_logic
    EVCNTLSTR        : std_logic
    EVCNTRES         : std_logic
    INACTIVE         : std_logic
    L1ACCEPT         : std_logic
    L1A_X            : std_logic
    ORBIT_X          : std_logic
    RESET_DCM_TIM    : std_logic
    RESET_TIM        : std_logic
    SEL_TTCLK        : std_logic
    SERIAL_B_CHAN    : std_logic
    SINERRSTR        : std_logic
    SUBADDR          : std_logic_vector(7 DOWNTO 0)
    TIMFDL_H         : std_logic_vector(15 DOWNTO 8)
    TIMGTFE1         : std_logic
    TIMTCS_H         : std_logic_vector(15 DOWNTO 8)
    TTCREADY         : std_logic
    WR_TIM           : std_logic
    BX               : std_logic_vector(11 DOWNTO 0)
    CLK0_FOR_FB      : std_ulogic
    CLK_LOCKED       : std_logic
    CLK_TIM          : std_ulogic
    CLK_TIM_LEMO     : std_ulogic
    L1A_LED          : std_logic
    L_BCRES          : std_logic_vector(9 DOWNTO 1)
    L_L1A            : std_logic_vector(9 DOWNTO 1)
    L_RESET          : std_logic_vector(9 DOWNTO 1)
    NBERR_TIM        : std_logic          := '1'
    NDTACK_TIM       : std_logic REGISTER := '1'
    NEN_CHLINK       : std_logic
    NEN_RO_BUS_T     : std_logic
    NEN_TIMFDL       : std_logic_vector(1 DOWNTO 0)
    NEN_TIMTCS       : std_logic_vector(1 DOWNTO 0)
    NIRQ_FR_TIM      : std_logic
    NL_EN            : std_logic_vector(9 DOWNTO 1)
    NR_EN            : std_logic_vector(8 DOWNTO 1)
    RDRQST_T         : std_logic
    RESET_B          : std_logic
    RO_CLK           : std_logic
    RO_DAT           : std_logic_vector(27 DOWNTO 0)
    R_BCRES          : std_logic_vector(8 DOWNTO 1)
    R_L1A            : std_logic_vector(8 DOWNTO 1)
```

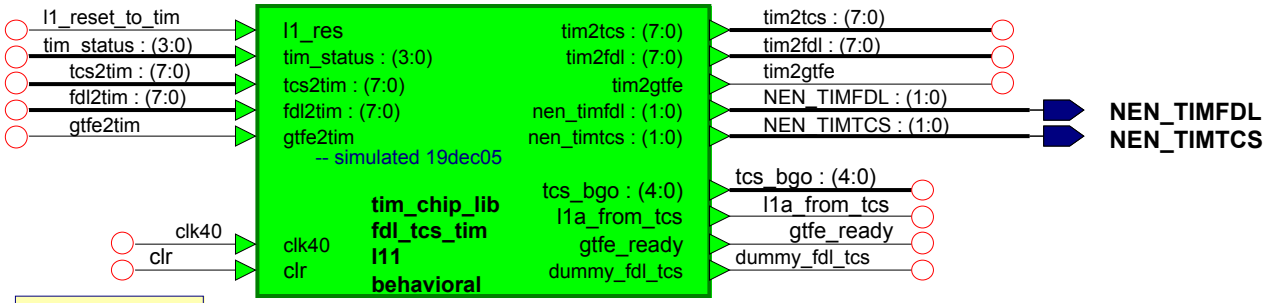
Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
USE IEEE.VITAL_Timing.all;
LIBRARY STD;
USE STD.TEXTIO.all;
LIBRARY unisim;
USE unisim.VPKG.all;
LIBRARY rop_chip_lib;
USE rop_chip_lib.all;
LIBRARY tim_chip_lib;
USE tim_chip_lib.all;
```

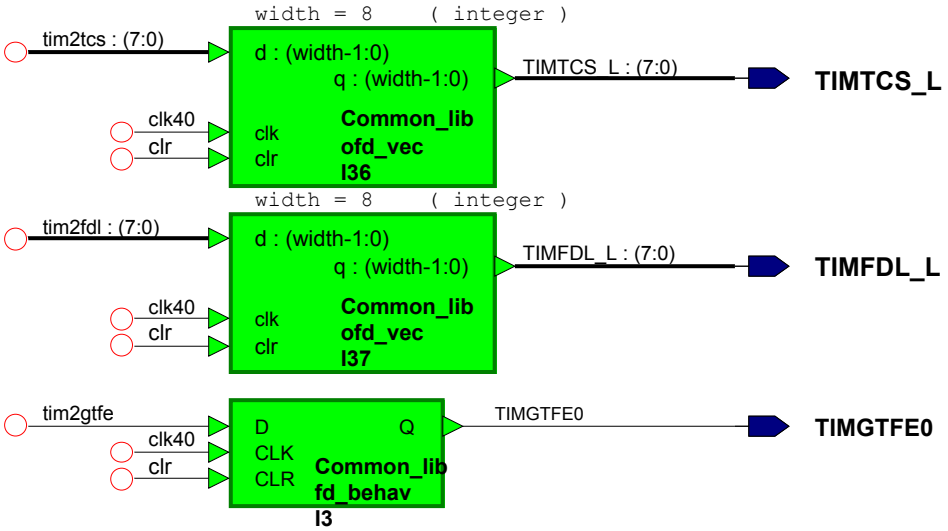
HEPHY Vienna		Project:	tim_chip
		tim_chip for TIM6UV2 board	
Title:	TIM_CHIP		
Path:	tim_chip_lib/tim_chip/struct		
Edited:	by taurok on 26 Mär 2007		


BRCST
BRCST : (7:2)
nclk40
clr
width = 6 (integer)
d : (width-1:0) q : (width-1:0)
clk
clr
Common_lib
fd_vec
I20
br_cst : (7:2)
BRCSTSTR1
BRCSTSTR1
nclk40
clr
D Q
CLK
CLR
Common_lib
fd_behav
I98
brcst_str1
clk40
clr
I19
BRCSTSTR2
BRCSTSTR2
I99
unused(7) : (15:0)
UNUSED
EVCNTHSTR
EVCNTHSTR
I100
unused(6) : (15:0)
Not used: TTCrx EV-counter
EVCNTLSTR
EVCNTLSTR
I101
unused(5) : (15:0)
DOUT
DOUT_STR
DOUT : (7:0)
width = 8 (integer)
d : (width-1:0) q : (width-1:0)
ce
clk
clr
Common_lib
fdce_vec
I47
unused_a(15:8) : (15:0)
Not used: DOUT,DQ for TTC dump
SUBADDR
SUBADDR : (7:0)
high
I45
unused_a(7:0) : (15:0)
Not used: SUBADDR for individual messages
DQ
DQ : (3:0)
I46
unused(11:8) : (15:0)
Not used: DOUT,DQ for TTC dump
BCNT
BCNTSTR
BCNT : (11:0)
width = 12 (integer)
I23
bcnt_ttc : (11:0)
Not used: TTCrx BC-counter
br_cst(5:2) : (7:2)
brcst_str1
width = 4 (integer)
ttc_bgo(3:0) : (4:0)
I12
ttc_bgo(4) : (4:0)
br_cst(7:7) : (7:2)
Buff
unused(15) : (15:0)
User message: not used
buff
I52
br_cst(7:6) : (7:2)
unused(14:13) : (15:0)
I50
Not used: TTCrx Serial interface; SCL,SDA go to VME chip
SERIAL_B_CHAN
I104
unused(12) : (15:0)
SINERRSTR
I106
sinerr_str
DBERRSTR
I107
dberr_str
From VME chip
nreset_ttc
I
O
unisim
OBUF
I53
OBUF_V
RESET_B
low active
TTCrx interface


Channel Link
from signal_merger
l1_reset_to_tim
res_evnr_to_tim
run_ff
l1a2tim_rop
bcr2tim_rop
clr
clk40
l1_reset
res_evnr
run_ff
l1a
bcres
clr
clk
-- sim5jan07
tim_chip_lib
chan_link_sim
l73
rop_error
rodat : (27:0)
rop_fifo_empty
rop_fifo_warn
sm_status : (15:0)
width = 28 (integer)
d : (width-1:0)
q : (width-1:0)
clk
clr
Common_lib
ofd_vec
l33
behavioral
clk40
clr
RO_DAT : (27:0)
RO_DAT
nclk40
I
unisim
OBUF
l30
O
OBUF_V
RO_CLK
RO_CLK
ro_cmd_reg(11)
clk40
clr
D
CLK
CLR
Q
Common_lib
fd_behav
l0
en_ch_link
inv
l58
NEN_CHLINK
NEN_CHLINK = NRO_ON_T
in TIM6U_V2 schematic
RO_CMD_REG(11): ro_link_on
tim_status ==> as TIMFDL() to FDL board
gnd_1
ro_cmd_reg(8)
ro_cmd_reg(7)
ttcrx_dberr
l1a_err
bcr_err
gnd_1
gnd_1
gnd_1
gnd_1
gnd_1
cmd_reg(15:14)
ttc_rdy
disconn
en_bc_check
en_ttc_check
dberr_ttc
l1a_err
bcr_err
out_sync1
out_sync0
busy
warn1
warn0
tim_stat : (1:0)
ttc_ready
status : (3:0)
--simulated 14nov05
tim_chip_lib
status_encoder
l10
behavioral
tim_status : (3:0)
Check L1A, BCRes
width = 16 (integer)
from 'periodic_sigs'
004a=rd_ttcrx_err
004c= rd_l1a_err
004e=rd_bc_err
dberr_str
sinerr_str
l1a_tcs_dlyed
l1a_ttc
bc_err_p
rd_40_5e(5) : (15:0)
rd_40_5e(6) : (15:0)
rd_40_5e(7) : (15:0)
l1_reset_to_tim
clr
clk40
dberr_str
sinerr_str
l1a_tcs_dlyed
l1a_ttc
bc_err_p
rd_ttcrx_err
rd_l1a_err
rd_bc_err
l1_reset
clr
clk
tim_chip_lib
check_bc_l1a
l44
behavioral
-- simulated 13dec05
ttcrx_errors : (15:0)
l1a_errors : (15:0)
bc_errors : (15:0)
ttcrx_err
ttcrx_dberr
l1a_err
bcr_err
ttc_err_led
tp_inc_bcerr
tp_inc_l1a_err
tp_inc_ttcrx_err
ttcrx_errors : (15:0)
l1a_errors : (15:0)
bc_errors : (15:0)
ttcrx_err
ttcrx_dberr
l1a_err
bcr_err
ttc_err_led
tp_inc_bcerr
tp_inc_ttcrx_err
read also clears cntrs + flags
Status Encoder
RO_CMD_REG (8) = EN_BC_CHECK
(compares ext.BCRES and end_of_orbit)
RO_CMD_REG (7) = EN_TTC_CHECK
(checks ttcrx_dberr, ttc_ready)
CMD_REG (15:14) = tim_stat
00 = disconnected
10 = ready
01 = busy
11 = disconnected

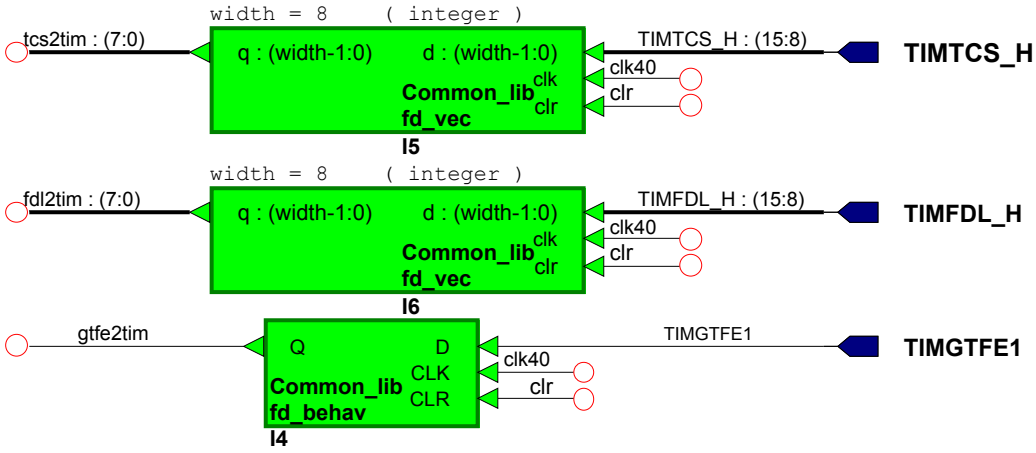


Outputs to TCS/GTFE disabled;
outputs to FDL enabled to send status for TCS
inputs from all enabled.



Backplane Signals

TIM-TCS,FDL,GTFE



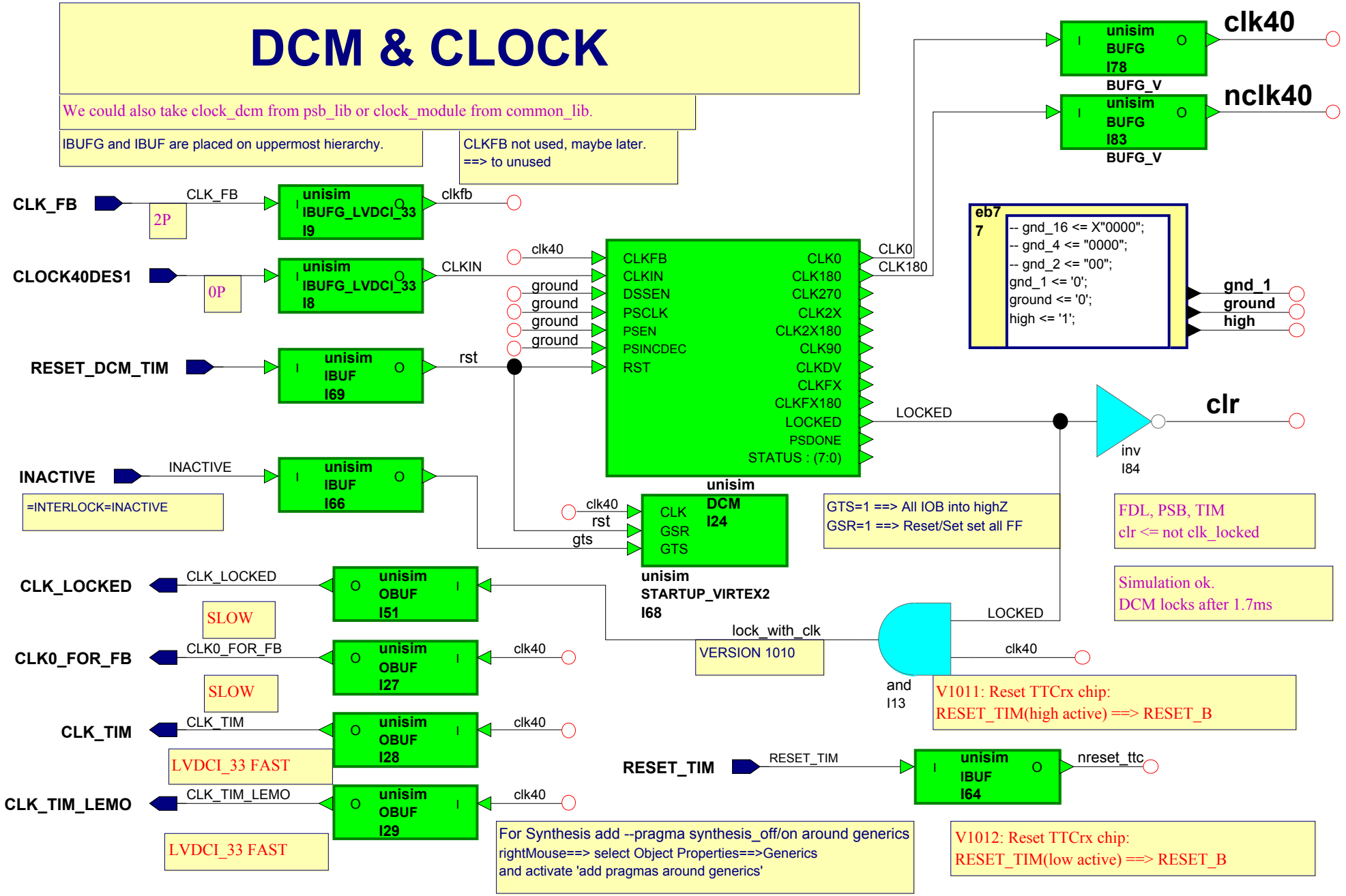
```
R_RESET          : std_logic_vector(8 DOWNTO 1)
STROB            : std_logic_vector(2 DOWNTO 0)
TEST_T1          : std_logic
TEST_T2          : std_logic
TEST_T3          : std_logic
TEST_T4          : std_logic
TIMFDL_L         : std_logic_vector(7 DOWNTO 0)
TIMGTFE0         : std_logic
TIMTCS_L         : std_logic_vector(7 DOWNTO 0)
TTC_ERR          : std_logic
VDATA            : std_logic_vector(15 DOWNTO 0)
```

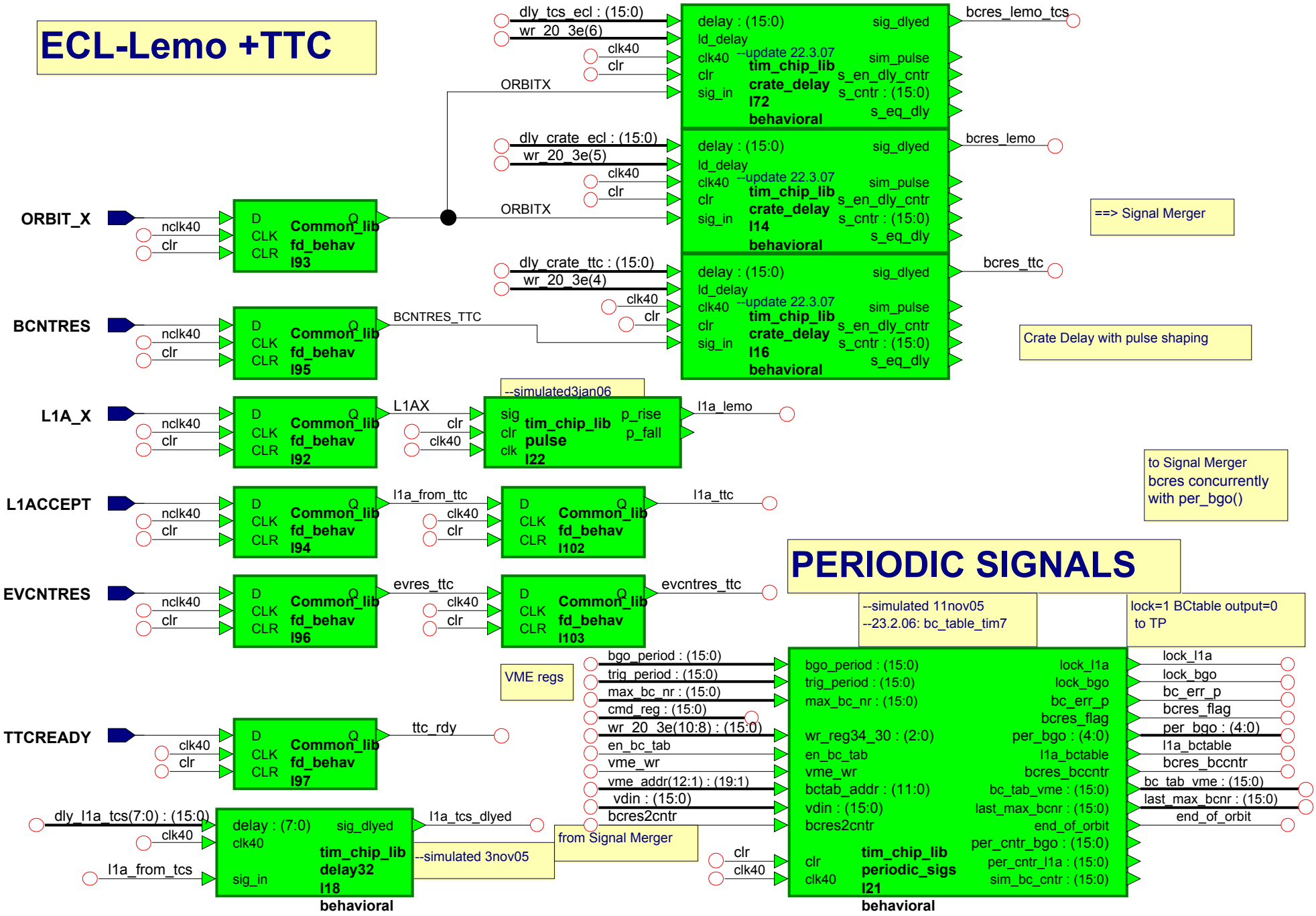
Diagram Signals:

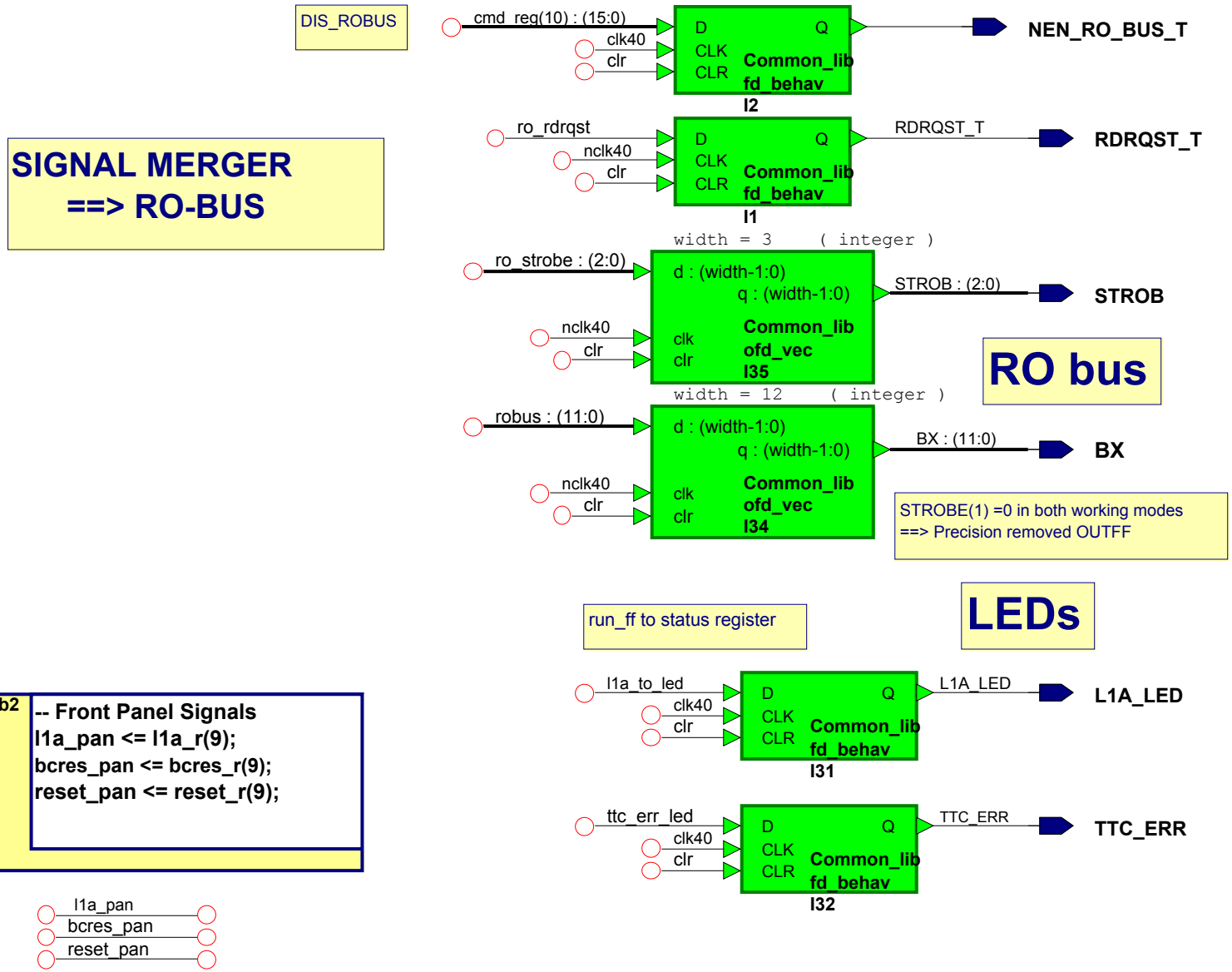
```
SIGNAL BCNTRES_TTC      : std_logic
SIGNAL CLK0             : std_ulogic         := '0'
SIGNAL CLK180           : std_ulogic         := '0'
SIGNAL CLKIN            : std_logic
SIGNAL L1AX             : std_logic
SIGNAL LOCKED           : std_logic
SIGNAL ORBITX           : std_logic
SIGNAL bc_err_p         : std_logic
SIGNAL bc_errors        : std_logic_vector(15 DOWNTO 0)
SIGNAL bc_tab_vme       : std_logic_vector(15 DOWNTO 0)
SIGNAL bcnt_ttc         : std_logic_vector(11 DOWNTO 0)
SIGNAL bcr2tim_rop      : std_logic
SIGNAL bcr_err          : std_logic
SIGNAL bcres2cntr       : std_logic
SIGNAL bcres_bccntr     : std_logic
SIGNAL bcres_flag       : std_logic
SIGNAL bcres_l          : std_logic_vector(9 DOWNTO 1)
SIGNAL bcres_lemo       : std_logic
SIGNAL bcres_lemo_tcs   : std_logic
SIGNAL bcres_pan        : std_logic
SIGNAL bcres_r          : std_logic_vector(9 DOWNTO 1)
SIGNAL bcres_ttc        : std_logic
SIGNAL berr             : std_logic
SIGNAL bgo_period       : std_logic_vector(15 DOWNTO 0)
SIGNAL br_cst           : std_logic_vector(7 DOWNTO 2)
SIGNAL brcst_str1       : std_logic
SIGNAL chip_idh         : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_idl         : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_versh       : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_versl       : std_logic_vector(15 DOWNTO 0)
SIGNAL clk40            : std_logic
SIGNAL clkfb            : STD_ULOGIC
SIGNAL clr              : std_logic
SIGNAL cmd_pulse        : std_logic_vector(15 DOWNTO 0)
SIGNAL cmd_reg          : std_logic_vector(15 DOWNTO 0)
SIGNAL day_month        : std_logic_vector(15 DOWNTO 0)
SIGNAL dberr_str        : std_logic
SIGNAL dis_boards       : std_logic_vector(15 DOWNTO 0)
SIGNAL dis_vdoo         : std_logic
SIGNAL dly_crate_ecl    : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_crate_ttc    : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l1           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l1a_tcs      : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l2           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l3           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l4           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l5           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l6           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l7           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l8           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_l9           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_pan          : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r1           : std_logic_vector(15 DOWNTO 0)
```

```
TimingChecksOn                        = true                    ( boolean          )
InstancePath                          = "*"                     ( string           )
Xon                                   = true                    ( boolean          )
MsgOn                                 = false                   ( boolean          )
thold_PSEN_PSCLK_negedge_posedge      = 0.000 ns                ( VitalDelayType   )
thold_PSEN_PSCLK_posedge_posedge      = 0.000 ns                ( VitalDelayType   )
thold_PSINCDEC_PSCLK_negedge_posedge  = 0.000 ns                ( VitalDelayType   )
thold_PSINCDEC_PSCLK_posedge_posedge  = 0.000 ns                ( VitalDelayType   )
tipd_CLKFB                            = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tipd_CLKIN                            = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tipd_DSSEN                            = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tipd_PSCLK                            = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tipd_PSEN                             = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tipd_PSINCDEC                         = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tipd_RST                              = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tpd_CLKIN_LOCKED                      = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tpd_PSCLK_PSDONE                      = (0.000 ns, 0.000 ns)    ( VitalDelayType01 )
tperiod_CLKIN_POSEDGE                 = 0.000 ns                ( VitalDelayType   )
tperiod_PSCLK_POSEDGE                 = 0.000 ns                ( VitalDelayType   )
tpw_CLKIN_negedge                     = 0.000 ns                ( VitalDelayType   )
tpw_CLKIN_posedge                     = 0.000 ns                ( VitalDelayType   )
tpw_PSCLK_negedge                     = 0.000 ns                ( VitalDelayType   )
tpw_PSCLK_posedge                     = 0.000 ns                ( VitalDelayType   )
tpw_RST_posedge                       = 0.000 ns                ( VitalDelayType   )
tsetup_PSEN_PSCLK_negedge_posedge     = 0.000 ns                ( VitalDelayType   )
tsetup_PSEN_PSCLK_posedge_posedge     = 0.000 ns                ( VitalDelayType   )
tsetup_PSINCDEC_PSCLK_negedge_posedge = 0.000 ns                ( VitalDelayType   )
tsetup_PSINCDEC_PSCLK_posedge_posedge = 0.000 ns                ( VitalDelayType   )
CLKDV_DIVIDE                          = 2.0                     ( real             )
CLKFX_DIVIDE                          = 1                       ( integer          )
CLKFX_MULTIPLY                        = 4                       ( integer          )
CLKIN_DIVIDE_BY_2                     = false                   ( boolean          )
CLKIN_PERIOD                          = 0.0                     ( real             )
CLKOUT_PHASE_SHIFT                    = "NONE"                  ( string           )
CLK_FEEDBACK                          = "1X"                    ( string           )
DESKEW_ADJUST                         = "SYSTEM_SYNCHRONOUS"    ( string           )
DFS_FREQUENCY_MODE                    = "LOW"                   ( string           )
DLL_FREQUENCY_MODE                    = "LOW"                   ( string           )
DSS_MODE                              = "NONE"                  ( string           )
DUTY_CYCLE_CORRECTION                 = true                    ( boolean          )
FACTORY_JF                            = X"C080"                 ( bit_vector       )
MAXPERCLKIN                           = 1000000 ps              ( time             )
MAXPERPSCLK                           = 100000000 ps            ( time             )
PHASE_SHIFT                           = 0                       ( integer          )
SIM_CLKIN_CYCLE_JITTER                = 300 ps                  ( time             )
SIM_CLKIN_PERIOD_JITTER               = 1000 ps                 ( time             )
STARTUP_WAIT                          = false                   ( boolean          )
```

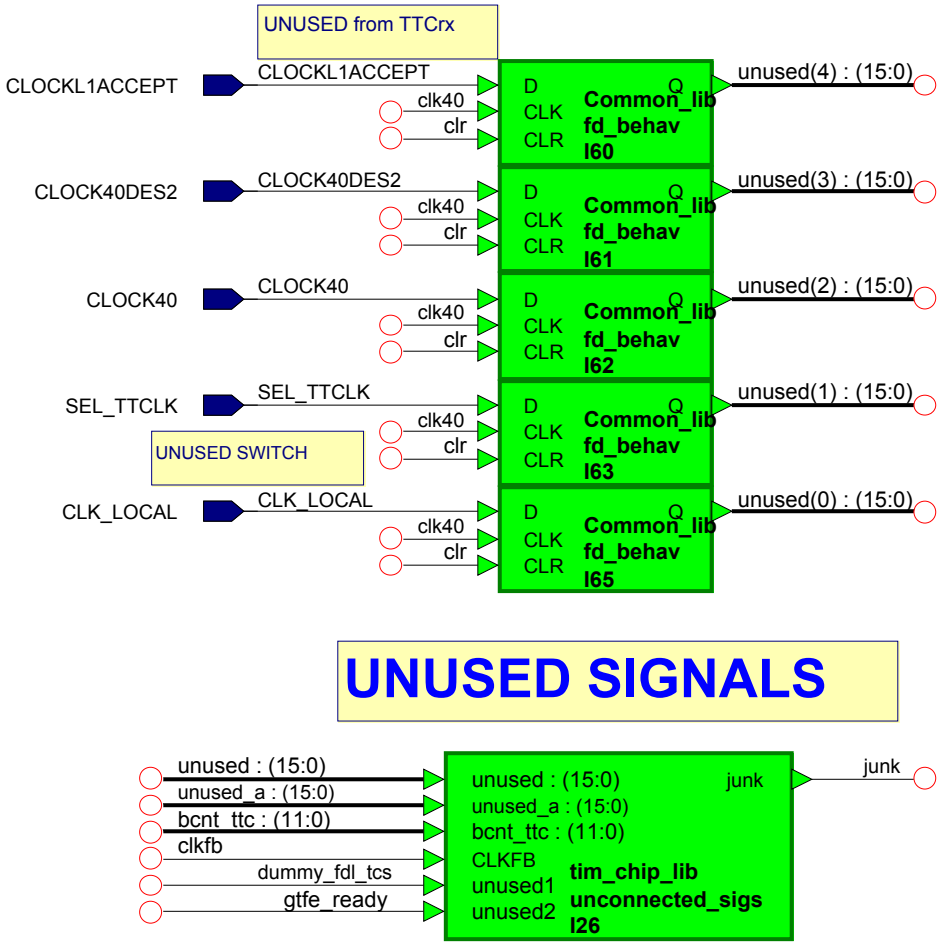
DCM & CLOCK

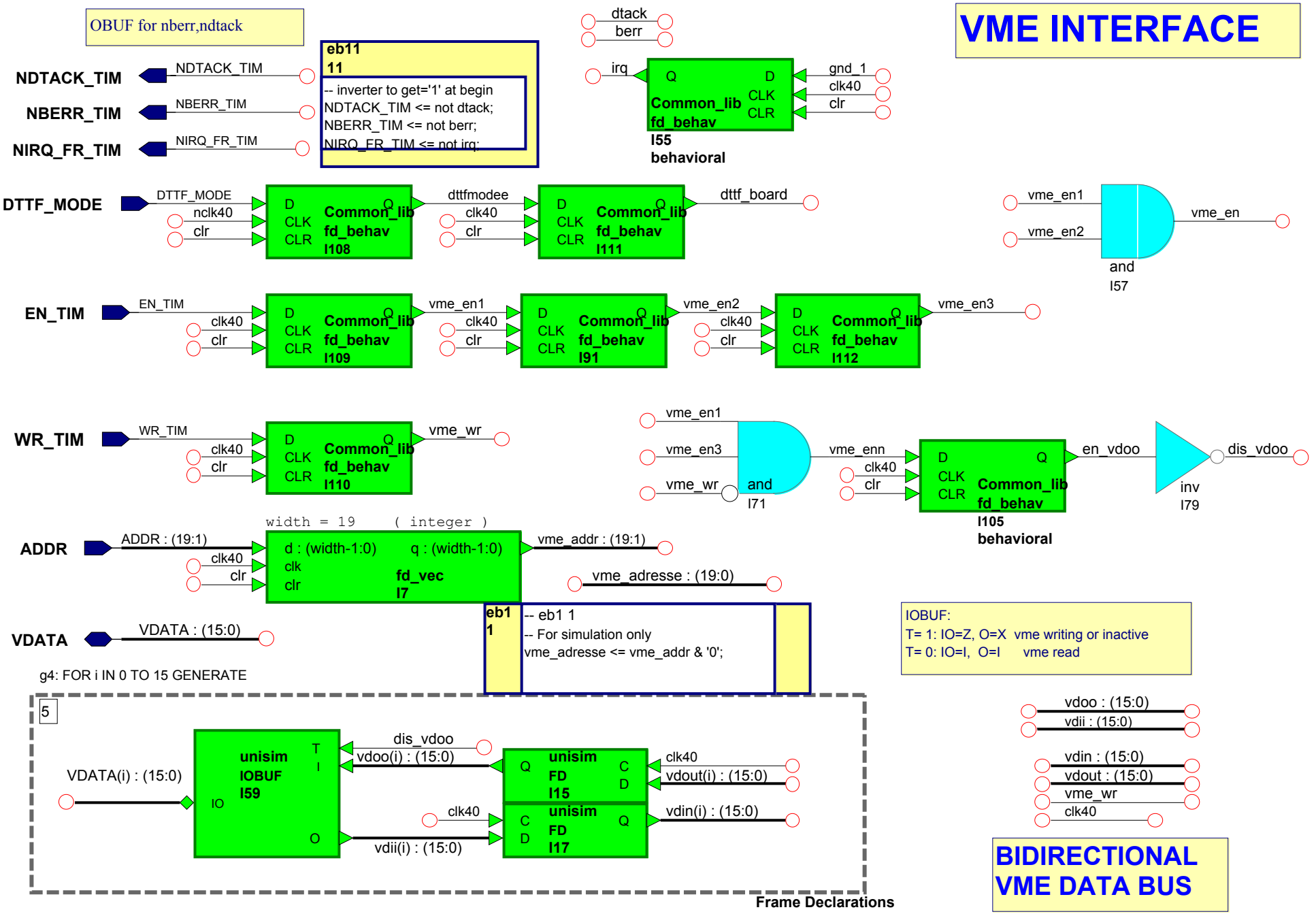

We could also take clock_dcm from psb_lib or clock_module from common_lib.
IBUFG and IBUF are placed on uppermost hierarchy.
CLKFB not used, maybe later.
==> to unused
CLK_FB
2P
CLK_FB
unisim IBUFG_LVDCI_33 I9
clkfb
CLOCK40DES1
0P
unisim IBUFG_LVDCI_33 I8
CLKIN
clk40
ground
ground
ground
ground
RESET_DCM_TIM
unisim IBUF I69
rst
CLKFB
CLKIN
DSSEN
PSCLK
PSEN
PSINCDEC
RST
CLK0
CLK180
CLK270
CLK2X
CLK2X180
CLK90
CLKDV
CLKFX
CLKFX180
LOCKED
PSDONE
STATUS : (7:0)
unisim DCM I24
CLK0
CLK180
unisim BUFG I78
BUFG_V
clk40
unisim BUFG I83
BUFG_V
nclk40
eb77
-- gnd_16 <= X"0000";
-- gnd_4 <= "0000";
-- gnd_2 <= "00";
gnd_1 <= '0';
ground <= '0';
high <= '1';
gnd_1
ground
high
LOCKED
inv I84
clr
INACTIVE
INACTIVE
unisim IBUF I66
=INTERLOCK=INACTIVE
clk40
rst
gts
CLK
GSR
GTS
unisim STARTUP_VIRTEX2 I68
GTS=1 ==> All IOB into highZ
GSR=1 ==> Reset/Set set all FF
FDL, PSB, TIM
clr <= not clk_locked
Simulation ok.
DCM locks after 1.7ms
CLK_LOCKED
CLK_LOCKED
unisim OBUF I51
SLOW
lock_with_clk
VERSION 1010
LOCKED
clk40
and I13
CLK0_FOR_FB
CLK0_FOR_FB
unisim OBUF I27
clk40
SLOW
CLK_TIM
CLK_TIM
unisim OBUF I28
clk40
LVDCI_33 FAST
V1011: Reset TTCrx chip:
RESET_TIM(high active) ==> RESET_B
RESET_TIM
RESET_TIM
unisim IBUF I64
nreset_ttc
CLK_TIM_LEMO
CLK_TIM_LEMO
unisim OBUF I29
clk40
LVDCI_33 FAST
For Synthesis add --pragma synthesis_off/on around generics
rightMouse==> select Object Properties==>Generics
and activate 'add pragmas around generics'
V1012: Reset TTCrx chip:
RESET_TIM(low active) ==> RESET_B

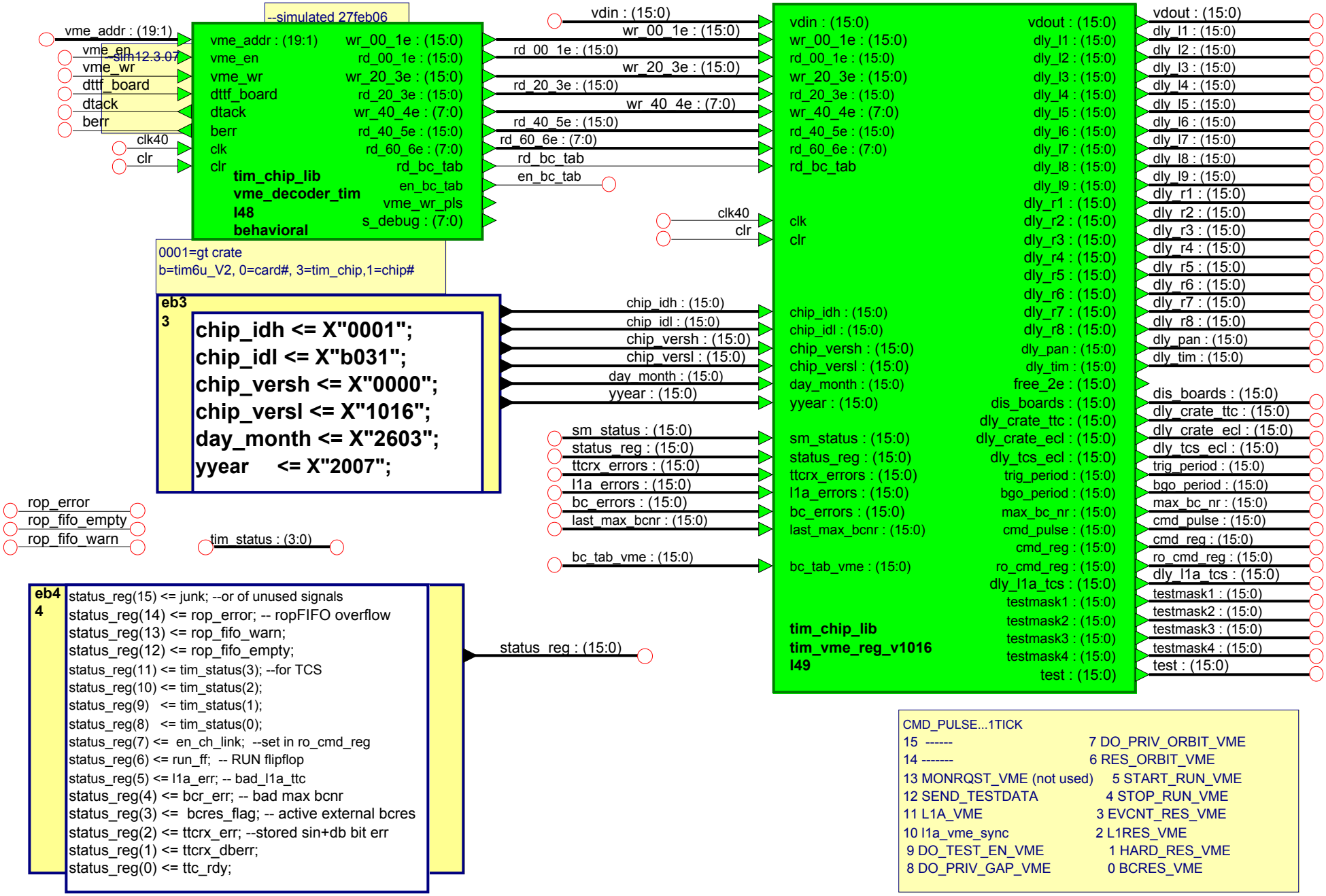

ECL-Lemo +TTC
dly_tcs_ecl : (15:0)
wr_20_3e(6)
clk40
clr
ORBITX
delay : (15:0)
ld_delay
clk40
clr
sig_in
--update 22.3.07
tim_chip_lib
crate_delay
I72
behavioral
sig_dlyed
sim_pulse
s_en_dly_cntr
s_cntr : (15:0)
s_eq_dly
bcres_lemo_tcs
dly_crate_ecl : (15:0)
wr_20_3e(5)
I14
bcres_lemo
dly_crate_ttc : (15:0)
wr_20_3e(4)
I16
bcres_ttc
==> Signal Merger
Crate Delay with pulse shaping
ORBIT_X
nclk40
D
CLK
CLR
Q
Common_lib
fd_behav
I93
BCNTRES
BCNTRES_TTC
I95
L1A_X
L1AX
I92
--simulated3jan06
sig
clr
clk
tim_chip_lib
pulse
I22
p_rise
p_fall
l1a_lemo
L1ACCEPT
l1a_from_ttc
I94
I102
l1a_ttc
EVCNTRES
evres_ttc
I96
I103
evcntres_ttc
to Signal Merger
bcres concurrently
with per_bgo()
PERIODIC SIGNALS
--simulated 11nov05
--23.2.06: bc_table_tim7
lock=1 BCtable output=0
to TP
VME regs
bgo_period : (15:0)
trig_period : (15:0)
max_bc_nr : (15:0)
cmd_reg : (15:0)
wr_20_3e(10:8) : (15:0)
en_bc_tab
vme_wr
vme_addr(12:1) : (19:1)
vdin : (15:0)
bcres2cntr
TTCREADY
ttc_rdy
I97
dly_l1a_tcs(7:0) : (15:0)
l1a_from_tcs
delay : (7:0)
I18
l1a_tcs_dlyed
--simulated 3nov05
from Signal Merger
wr_reg34_30 : (2:0)
bctab_addr : (11:0)
I21
lock_l1a
lock_bgo
bc_err_p
bcres_flag
per_bgo : (4:0)
l1a_bctable
bcres_bccntr
bc_tab_vme : (15:0)
last_max_bcnr : (15:0)
end_of_orbit
per_cntr_bgo : (15:0)
per_cntr_l1a : (15:0)
sim_bc_cntr : (15:0)
behavioral
behavioral


DIS_ROBUS
cmd_reg(10) : (15:0)
clk40
clr
D
Q
CLK
CLR
Common_lib
fd_behav
I2
NEN_RO_BUS_T
SIGNAL MERGER
==> RO-BUS
ro_rdrqst
nclk40
clr
RDRQST_T
RDRQST_T
I1
width = 3 (integer)
ro_strobe : (2:0)
d : (width-1:0)
q : (width-1:0)
STROB : (2:0)
STROB
nclk40
clr
clk
Common_lib
ofd_vec
I35
RO bus
width = 12 (integer)
robus : (11:0)
BX : (11:0)
BX
nclk40
clr
I34
STROBE(1) =0 in both working modes
==> Precision removed OUTFF
run_ff to status register
LEDs
l1a_to_led
L1A_LED
L1A_LED
I31
ttc_err_led
TTC_ERR
TTC_ERR
I32
eb2
2
-- Front Panel Signals
l1a_pan <= l1a_r(9);
bcres_pan <= bcres_r(9);
reset_pan <= reset_r(9);
l1a_pan
bcres_pan
reset_pan

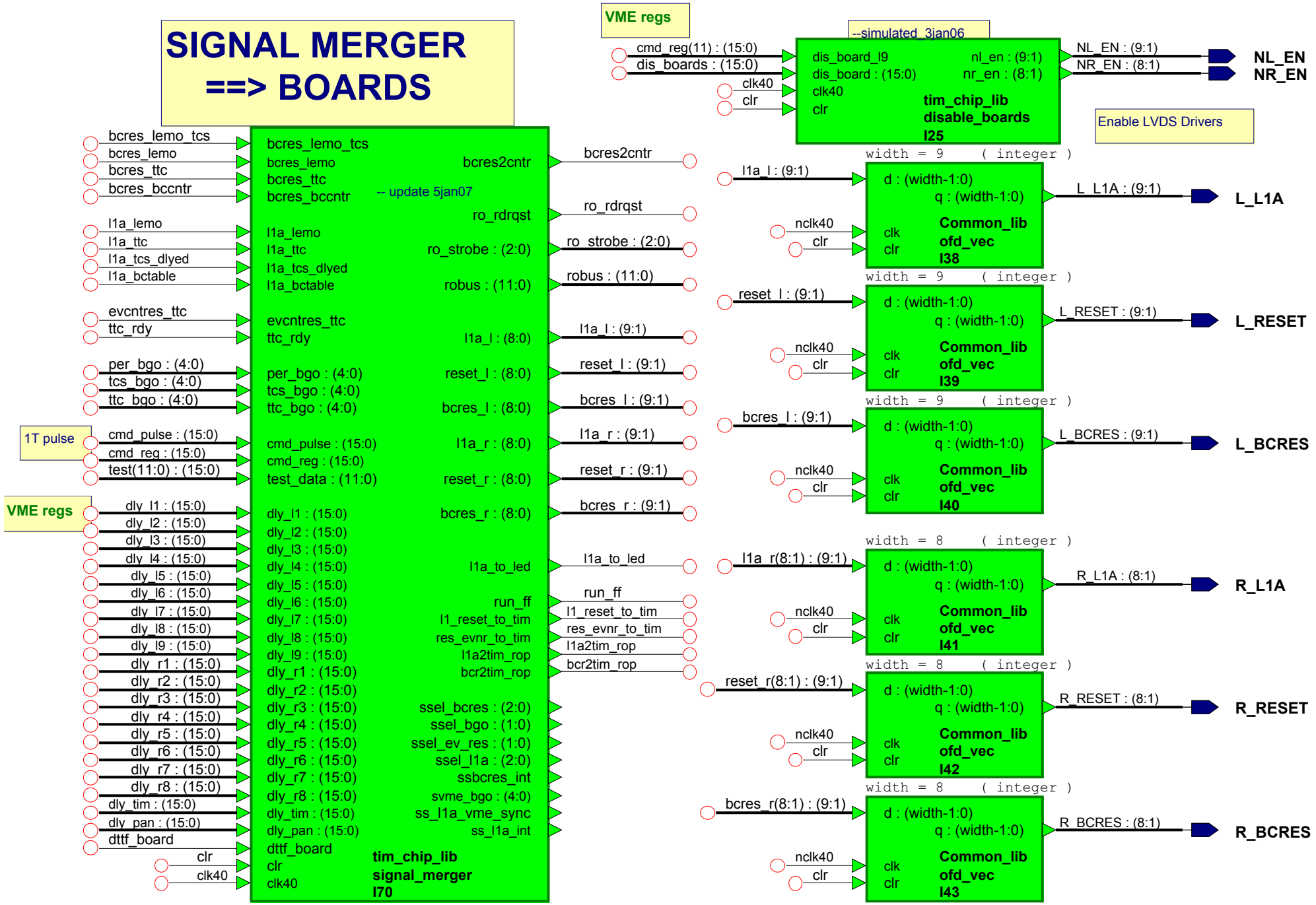
```
SIGNAL dly_r2           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r3           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r4           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r5           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r6           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r7           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_r8           : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_tcs_ecl      : std_logic_vector(15 DOWNTO 0)
SIGNAL dly_tim          : std_logic_vector(15 DOWNTO 0)
SIGNAL dtack            : std_logic
SIGNAL dttf_board       : std_logic
SIGNAL dttfmodee        : std_logic
SIGNAL dummy_fdl_tcs    : std_logic
SIGNAL en_bc_tab        : std_logic
SIGNAL en_ch_link       : std_logic
SIGNAL en_vdoo          : std_logic
SIGNAL end_of_orbit     : std_logic
SIGNAL evcntres_ttc     : std_logic
SIGNAL evres_ttc        : std_logic
SIGNAL fdl2tim          : std_logic_vector(7 DOWNTO 0)
SIGNAL gnd_1            : std_logic
SIGNAL ground           : std_logic
SIGNAL gtfe2tim         : std_logic
SIGNAL gtfe_ready       : std_logic
SIGNAL gts              : std_ulogic
SIGNAL high             : std_logic
SIGNAL irq              : std_logic
SIGNAL junk             : std_logic
SIGNAL l1_reset_to_tim  : std_logic
SIGNAL l1a2tim_rop      : std_logic
SIGNAL l1a_bctable      : std_logic
SIGNAL l1a_err          : std_logic
SIGNAL l1a_errors       : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_from_tcs     : std_logic
SIGNAL l1a_from_ttc     : std_logic
SIGNAL l1a_l            : std_logic_vector(9 DOWNTO 1)
SIGNAL l1a_lemo         : std_logic
SIGNAL l1a_pan          : std_logic
SIGNAL l1a_r            : std_logic_vector(9 DOWNTO 1)
SIGNAL l1a_tcs_dlyed    : std_logic
SIGNAL l1a_to_led       : std_logic
SIGNAL l1a_ttc          : std_logic
SIGNAL last_max_bcnr    : std_logic_vector(15 DOWNTO 0)
SIGNAL lock_bgo         : std_logic
SIGNAL lock_l1a         : std_logic
SIGNAL lock_with_clk    : std_ulogic
SIGNAL max_bc_nr        : std_logic_vector(15 DOWNTO 0)
SIGNAL nclk40           : std_logic
SIGNAL nreset_ttc       : std_logic
SIGNAL per_bgo          : std_logic_vector(4 DOWNTO 0)
SIGNAL rd_00_1e         : std_logic_vector(15 DOWNTO 0)
SIGNAL rd_20_3e         : std_logic_vector(15 DOWNTO 0)
SIGNAL rd_40_5e         : std_logic_vector(15 DOWNTO 0)
SIGNAL rd_60_6e         : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_bc_tab        : std_logic
SIGNAL res_evnr_to_tim  : std_logic
SIGNAL reset_l          : std_logic_vector(9 DOWNTO 1)
SIGNAL reset_pan        : std_logic
SIGNAL reset_r          : std_logic_vector(9 DOWNTO 1)
SIGNAL ro_cmd_reg       : std_logic_vector(15 DOWNTO 0)
SIGNAL ro_rdrqst        : std_logic
SIGNAL ro_strobe        : std_logic_vector(2 DOWNTO 0)
SIGNAL robus            : std_logic_vector(11 DOWNTO 0)
SIGNAL rodat            : std_logic_vector(27 DOWNTO 0)
SIGNAL rop_error        : std_logic
```




VME INTERFACE
OBUF for nberr,ndtack
NDTACK_TIM
NBERR_TIM
NIRQ_FR_TIM
eb11
11
-- inverter to get='1' at begin
NDTACK_TIM <= not dtack;
NBERR_TIM <= not berr;
NIRQ_FR_TIM <= not irq;
dtack
berr
irq
Common_lib
fd_behav
I55
behavioral
gnd_1
clk40
clr
DTTF_MODE
nclk40
I108
dttfmodee
I111
dttf_board
vme_en1
vme_en2
and
I57
vme_en
EN_TIM
I109
vme_en2
I91
I112
vme_en3
WR_TIM
I110
vme_wr
vme_en3
vme_enn
I71
I105
en_vdoo
inv
I79
dis_vdoo
ADDR
ADDR : (19:1)
width = 19 (integer)
d : (width-1:0)
q : (width-1:0)
clk
fd_vec
I7
vme_addr : (19:1)
vme_adresse : (19:0)
VDATA
VDATA : (15:0)
eb1
1
-- eb1 1
-- For simulation only
vme_adresse <= vme_addr & '0';
IOBUF:
T= 1: IO=Z, O=X vme writing or inactive
T= 0: IO=I, O=I vme read
g4: FOR i IN 0 TO 15 GENERATE
5
VDATA(i) : (15:0)
unisim
IOBUF
I59
IO
T
I
O
dis_vdoo
vdoo(i) : (15:0)
vdii(i) : (15:0)
unisim
FD
I15
I17
clk40
vdout(i) : (15:0)
vdin(i) : (15:0)
Frame Declarations
vdoo : (15:0)
vdii : (15:0)
vdin : (15:0)
vdout : (15:0)
vme_wr
clk40
BIDIRECTIONAL
VME DATA BUS


--simulated 27feb06
vme_addr : (19:1)
vme_en
vme_wr
dttf_board
dtack
berr
clk40
clr
--sim12.3.07
vme_addr : (19:1)
vme_en
vme_wr
dttf_board
dtack
berr
clk
clr
wr_00_1e : (15:0)
rd_00_1e : (15:0)
wr_20_3e : (15:0)
rd_20_3e : (15:0)
wr_40_4e : (7:0)
rd_40_5e : (15:0)
rd_60_6e : (7:0)
rd_bc_tab
en_bc_tab
vme_wr_pls
s_debug : (7:0)
tim_chip_lib
vme_decoder_tim
l48
behavioral
vdin : (15:0)
wr_00_1e : (15:0)
rd_00_1e : (15:0)
wr_20_3e : (15:0)
rd_20_3e : (15:0)
wr_40_4e : (7:0)
rd_40_5e : (15:0)
rd_60_6e : (7:0)
rd_bc_tab
en_bc_tab
clk40
clr
0001=gt crate
b=tim6u_V2, 0=card#, 3=tim_chip,1=chip#
eb33
chip_idh <= X"0001";
chip_idl <= X"b031";
chip_versh <= X"0000";
chip_versl <= X"1016";
day_month <= X"2603";
yyear <= X"2007";
chip_idh : (15:0)
chip_idl : (15:0)
chip_versh : (15:0)
chip_versl : (15:0)
day_month : (15:0)
yyear : (15:0)
sm_status : (15:0)
status_reg : (15:0)
ttcrx_errors : (15:0)
l1a_errors : (15:0)
bc_errors : (15:0)
last_max_bcnr : (15:0)
bc_tab_vme : (15:0)
rop_error
rop_fifo_empty
rop_fifo_warn
tim_status : (3:0)
eb44
status_reg(15) <= junk; --or of unused signals
status_reg(14) <= rop_error; -- ropFIFO overflow
status_reg(13) <= rop_fifo_warn;
status_reg(12) <= rop_fifo_empty;
status_reg(11) <= tim_status(3); --for TCS
status_reg(10) <= tim_status(2);
status_reg(9) <= tim_status(1);
status_reg(8) <= tim_status(0);
status_reg(7) <= en_ch_link; --set in ro_cmd_reg
status_reg(6) <= run_ff; -- RUN flipflop
status_reg(5) <= l1a_err; -- bad_l1a_ttc
status_reg(4) <= bcr_err; -- bad max bcnr
status_reg(3) <= bcres_flag; -- active external bcres
status_reg(2) <= ttcrx_err; --stored sin+db bit err
status_reg(1) <= ttcrx_dberr;
status_reg(0) <= ttc_rdy;
status_reg : (15:0)
vdin : (15:0)
wr_00_1e : (15:0)
rd_00_1e : (15:0)
wr_20_3e : (15:0)
rd_20_3e : (15:0)
wr_40_4e : (7:0)
rd_40_5e : (15:0)
rd_60_6e : (7:0)
rd_bc_tab
clk
clr
chip_idh : (15:0)
chip_idl : (15:0)
chip_versh : (15:0)
chip_versl : (15:0)
day_month : (15:0)
yyear : (15:0)
sm_status : (15:0)
status_reg : (15:0)
ttcrx_errors : (15:0)
l1a_errors : (15:0)
bc_errors : (15:0)
last_max_bcnr : (15:0)
bc_tab_vme : (15:0)
tim_chip_lib
tim_vme_reg_v1016
l49
vdout : (15:0)
dly_l1 : (15:0)
dly_l2 : (15:0)
dly_l3 : (15:0)
dly_l4 : (15:0)
dly_l5 : (15:0)
dly_l6 : (15:0)
dly_l7 : (15:0)
dly_l8 : (15:0)
dly_l9 : (15:0)
dly_r1 : (15:0)
dly_r2 : (15:0)
dly_r3 : (15:0)
dly_r4 : (15:0)
dly_r5 : (15:0)
dly_r6 : (15:0)
dly_r7 : (15:0)
dly_r8 : (15:0)
dly_pan : (15:0)
dly_tim : (15:0)
free_2e : (15:0)
dis_boards : (15:0)
dly_crate_ttc : (15:0)
dly_crate_ecl : (15:0)
dly_tcs_ecl : (15:0)
trig_period : (15:0)
bgo_period : (15:0)
max_bc_nr : (15:0)
cmd_pulse : (15:0)
cmd_reg : (15:0)
ro_cmd_reg : (15:0)
dly_l1a_tcs : (15:0)
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
testmask4 : (15:0)
test : (15:0)
vdout : (15:0)
dly_l1 : (15:0)
dly_l2 : (15:0)
dly_l3 : (15:0)
dly_l4 : (15:0)
dly_l5 : (15:0)
dly_l6 : (15:0)
dly_l7 : (15:0)
dly_l8 : (15:0)
dly_l9 : (15:0)
dly_r1 : (15:0)
dly_r2 : (15:0)
dly_r3 : (15:0)
dly_r4 : (15:0)
dly_r5 : (15:0)
dly_r6 : (15:0)
dly_r7 : (15:0)
dly_r8 : (15:0)
dly_pan : (15:0)
dly_tim : (15:0)
dis_boards : (15:0)
dly_crate_ttc : (15:0)
dly_crate_ecl : (15:0)
dly_tcs_ecl : (15:0)
trig_period : (15:0)
bgo_period : (15:0)
max_bc_nr : (15:0)
cmd_pulse : (15:0)
cmd_reg : (15:0)
ro_cmd_reg : (15:0)
dly_l1a_tcs : (15:0)
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
testmask4 : (15:0)
test : (15:0)
CMD_PULSE...1TICK
15 ------
14 -------
13 MONRQST_VME (not used)
12 SEND_TESTDATA
11 L1A_VME
10 l1a_vme_sync
9 DO_TEST_EN_VME
8 DO_PRIV_GAP_VME
7 DO_PRIV_ORBIT_VME
6 RES_ORBIT_VME
5 START_RUN_VME
4 STOP_RUN_VME
3 EVCNT_RES_VME
2 L1RES_VME
1 HARD_RES_VME
0 BCRES_VME

SIGNAL MERGER ==> BOARDS



```
SIGNAL rop_fifo_empty   : std_logic
SIGNAL rop_fifo_warn    : std_logic
SIGNAL rst              : STD_ULOGIC
SIGNAL run_ff           : std_logic
SIGNAL sinerr_str       : std_logic
SIGNAL sm_status        : std_logic_vector(15 DOWNTO 0)
SIGNAL status_reg       : std_logic_vector(15 DOWNTO 0)
SIGNAL tcs2tim          : std_logic_vector(7 DOWNTO 0)
SIGNAL tcs_bgo          : std_logic_vector(4 DOWNTO 0)
SIGNAL test             : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask1        : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask2        : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask3        : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask4        : std_logic_vector(15 DOWNTO 0)
SIGNAL tim2fdl          : std_logic_vector(7 DOWNTO 0)
SIGNAL tim2gtfe         : std_logic
SIGNAL tim2tcs          : std_logic_vector(7 DOWNTO 0)
SIGNAL tim_status       : std_logic_vector(3 DOWNTO 0)
SIGNAL tp_inc_bcerr     : std_logic
SIGNAL tp_inc_ttcrx_err : std_logic
SIGNAL tpp1             : std_logic
SIGNAL tpp2             : std_logic
SIGNAL tpp3             : std_logic
SIGNAL tpp4             : std_logic
SIGNAL trig_period      : std_logic_vector(15 DOWNTO 0)
SIGNAL ttc_bgo          : std_logic_vector(4 DOWNTO 0)
SIGNAL ttc_err_led      : std_logic
SIGNAL ttc_rdy          : std_logic
SIGNAL ttcrx_dberr      : std_logic
SIGNAL ttcrx_err        : std_logic
SIGNAL ttcrx_errors     : std_logic_vector(15 DOWNTO 0)
SIGNAL unused           : std_logic_vector(15 DOWNTO 0)
SIGNAL unused_a         : std_logic_vector(15 DOWNTO 0)
SIGNAL vdii             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vdin             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vdoo             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vdout            : std_logic_vector(15 DOWNTO 0)
SIGNAL vme_addr         : std_logic_VECTOR(19 DOWNTO 1)
SIGNAL vme_adresse      : std_logic_vector(19 DOWNTO 0)
SIGNAL vme_en           : std_logic
SIGNAL vme_en1          : std_logic
SIGNAL vme_en2          : std_logic
SIGNAL vme_en3          : std_logic
SIGNAL vme_enn          : std_logic
SIGNAL vme_wr           : std_logic
SIGNAL wr_00_1e         : std_logic_vector(15 DOWNTO 0)
SIGNAL wr_20_3e         : std_logic_vector(15 DOWNTO 0)
SIGNAL wr_40_4e         : std_logic_vector(7 DOWNTO 0)
SIGNAL yyear            : std_logic_vector(15 DOWNTO 0)
```

INFO page

```
 tim_chip versions:
V1016: 26.3.07: vme_reg: read-mux with elsif, ..50=tim_status, ..52=sm_status,
                readback cmd_pulse_reg, rop changed,
V1015: 24.1.07:  Precision:  FrontEnd_2004 Option selected --> seems to work better
                 testmask4(9) ..rd_20_3e(12)=read status_reg
                 tim_vme_reg_v1015, new status_reg bits
V1014: 23.1.07:  tim_vme_regs without CASE code; table code used to get correct multiplexer
V1013: 19.1.07: vme_en...with old circuit from V1010
V1012: 16.1.07: RESET_TIM as low active expected ==> no inverter ==> nreset_ttc
V1011: 2.1.07:  Version for GT: special delays for TCS board!!
        BCRES_FLAG, ev_res by vme_cmd_pulse again,
        tim_status: without L1A_ttc&tcs comparison
-----------------------------------------
tim_chip_v7 versions:
V1010: 23.11.06: new circuit for TIM_LOCKED
V1009: 12.10.06 : tp3, tp4 changed
                  ev_res selection simplified,
V1008:  20.09.06: send robus, BRES, L1A ... with inverted clk40
V1007:  21.04.06: reset_ttcrx inverted==> low active RESET_B
----------------------------
V1006: tim_chip version is deleted!!
```

ROCMD_REG
15-12: not used
11: RO_LINK_ON
10-9: not used
8: EN_BC_CHECK
7: EN_TTC_CHECK
6-0: not used

COMMAND_REG
15-14: TIMSTATUS: 00=disconn,10=rdy
01=busy, 11=disconn
13: not used
12: not used
11: DIS_BOARD_L9
10: DIS_RO_BUS
9-8: SEL_EVRES: 00=vme, 01=ttc,
10=bgo, 11=inhibit
7-6:SEL_BGO: 00=vme, 01=ttc
10=periodic, 11=tcs
5-4: SEL_BCRES: 000=vme, 001=ttc
010=lemo, 011=periodic
others=inhibit
3-0: SEL_L1A: 000=vme, 001=ttc
010=lemo, 011=periodic
100=tcs, others=inhibit

```
-- Assign debug output signals
s_debug(0) <= or_wdtck;
s_debug(1) <= dtck_wff;
s_debug(2) <= or_rdtck;
s_debug(3) <= dtck_rff;
s_debug(4) <= dtck_rff2;
s_debug(5) <= vme_reg;
s_debug(6) <= vme_rd;
s_debug(7) <= addr_60_6e;
```

INFO page

TEST_T1

bcres_pan
l1a_bctable
evcntres_ttc
bcres2cntr

ORBITX
BCNTRES_TTC
l1a_from_tcs
vme_en

tp_inc_bcerr
bcres_lemo_tcs
reset_r(3) : (9:1)
reset_r(2) : (9:1)

reset_r(1) : (9:1)
bcres_r(3) : (9:1)
bcres_r(2) : (9:1)
bcres_r(1) : (9:1)

TEST_T2

l1a_pan
l1a_lemo
l1a_ttc
bcres_bccntr

bit 15

bcres_lemo
bcres_ttc
l1a_tcs_dlyed
vme_wr

bit 11

l1_reset_to_tim
tp_inc_ttcrx_err
l1a_l(3) : (9:1)
l1a_l(2) : (9:1)

bit 7

l1a_l(1) : (9:1)
l1a_r(3) : (9:1)
l1a_r(2) : (9:1)
l1a_r(1) : (9:1)

bit 3

V1011: new

TEST_T3

reset_pan
ttc_rdy
tcs2tim(7) : (7:0)
l1a_to_led

tcs2tim(7) = l1a_tcs //original pulse

dtack
wr_40_4e(2) : (7:0)
wr_20_3e(1) : (15:0)
wr_00_1e(0) : (15:0)

end_of_orbit
robus(6) : (11:0)
robus(5) : (11:0)
robus(4) : (11:0)

robus(3) : (11:0)
robus(2) : (11:0)
robus(1) : (11:0)
robus(0) : (11:0)

TEST_T4

clk40
dttf_board
nreset_ttc
l1a_bctable

bit 15

bit 11

rd_60_6e(3) : (7:0)
rd_40_5e(2) : (15:0)
rd_20_3e(12) : (15:0)
rd_00_1e(0) : (15:0)

lock_bgo
lock_l1a
en_bc_tab
ro_rdrqst

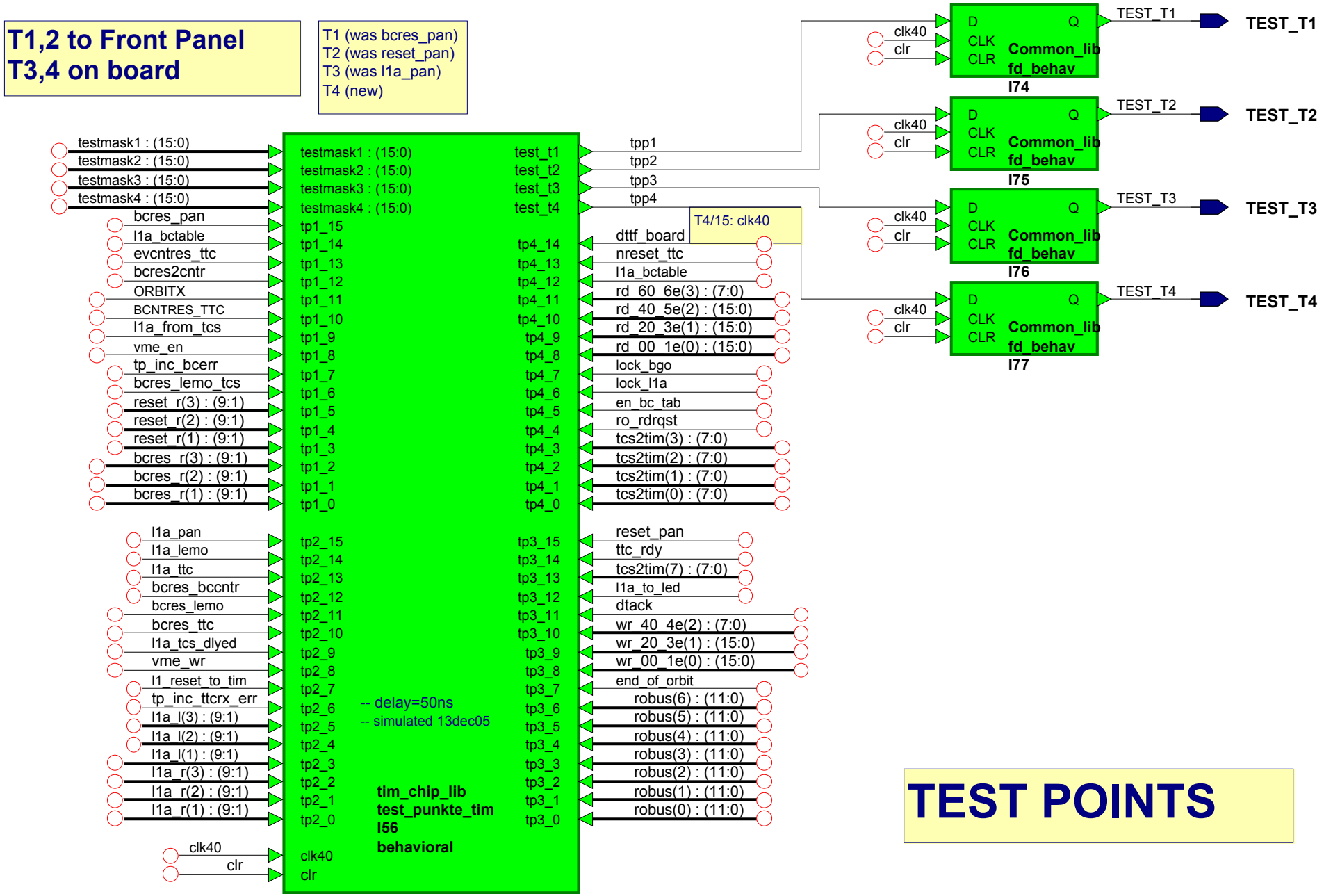
bit 7

tcs2tim(3) : (7:0)
tcs2tim(2) : (7:0)
tcs2tim(1) : (7:0)
tcs2tim(0) : (7:0)

bit 3

L1Reset clears error flags for TIM_status, not VME regs and err counters

```
-- robus 6: STOP_RUN
-- robus 5: START_RUN
-- robus 4: RES_ORBITNR
-- robus 3: HARD_RES
-- robus 2: PRIVATE_ORBIT
-- robus 1: PRIVATE_GAP
-- robus 0: TEST_EN
```


T1,2 to Front Panel
T3,4 on board
T1 (was bcres_pan)
T2 (was reset_pan)
T3 (was l1a_pan)
T4 (new)
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
testmask4 : (15:0)
bcres_pan
l1a_bctable
evcntres_ttc
bcres2cntr
ORBITX
BCNTRES_TTC
l1a_from_tcs
vme_en
tp_inc_bcerr
bcres_lemo_tcs
reset_r(3) : (9:1)
reset_r(2) : (9:1)
reset_r(1) : (9:1)
bcres_r(3) : (9:1)
bcres_r(2) : (9:1)
bcres_r(1) : (9:1)
l1a_pan
l1a_lemo
l1a_ttc
bcres_bccntr
bcres_lemo
bcres_ttc
l1a_tcs_dlyed
vme_wr
l1_reset_to_tim
tp_inc_ttcrx_err
l1a_l(3) : (9:1)
l1a_l(2) : (9:1)
l1a_l(1) : (9:1)
l1a_r(3) : (9:1)
l1a_r(2) : (9:1)
l1a_r(1) : (9:1)
clk40
clr
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
testmask4 : (15:0)
tp1_15
tp1_14
tp1_13
tp1_12
tp1_11
tp1_10
tp1_9
tp1_8
tp1_7
tp1_6
tp1_5
tp1_4
tp1_3
tp1_2
tp1_1
tp1_0
tp2_15
tp2_14
tp2_13
tp2_12
tp2_11
tp2_10
tp2_9
tp2_8
tp2_7
tp2_6
tp2_5
tp2_4
tp2_3
tp2_2
tp2_1
tp2_0
clk40
clr
-- delay=50ns
-- simulated 13dec05
tim_chip_lib
test_punkte_tim
I56
behavioral
test_t1
test_t2
test_t3
test_t4
tp4_14
tp4_13
tp4_12
tp4_11
tp4_10
tp4_9
tp4_8
tp4_7
tp4_6
tp4_5
tp4_4
tp4_3
tp4_2
tp4_1
tp4_0
tp3_15
tp3_14
tp3_13
tp3_12
tp3_11
tp3_10
tp3_9
tp3_8
tp3_7
tp3_6
tp3_5
tp3_4
tp3_3
tp3_2
tp3_1
tp3_0
tpp1
tpp2
tpp3
tpp4
T4/15: clk40
dttf_board
nreset_ttc
l1a_bctable
rd_60_6e(3) : (7:0)
rd_40_5e(2) : (15:0)
rd_20_3e(1) : (15:0)
rd_00_1e(0) : (15:0)
lock_bgo
lock_l1a
en_bc_tab
ro_rdrqst
tcs2tim(3) : (7:0)
tcs2tim(2) : (7:0)
tcs2tim(1) : (7:0)
tcs2tim(0) : (7:0)
reset_pan
ttc_rdy
tcs2tim(7) : (7:0)
l1a_to_led
dtack
wr_40_4e(2) : (7:0)
wr_20_3e(1) : (15:0)
wr_00_1e(0) : (15:0)
end_of_orbit
robus(6) : (11:0)
robus(5) : (11:0)
robus(4) : (11:0)
robus(3) : (11:0)
robus(2) : (11:0)
robus(1) : (11:0)
robus(0) : (11:0)
clk40
clr
D
CLK
CLR
Q
Common_lib
fd_behav
I74
I75
I76
I77
TEST_T1
TEST_T2
TEST_T3
TEST_T4
TEST_T1
TEST_T2
TEST_T3
TEST_T4
TEST POINTS