Declarations

Ports:

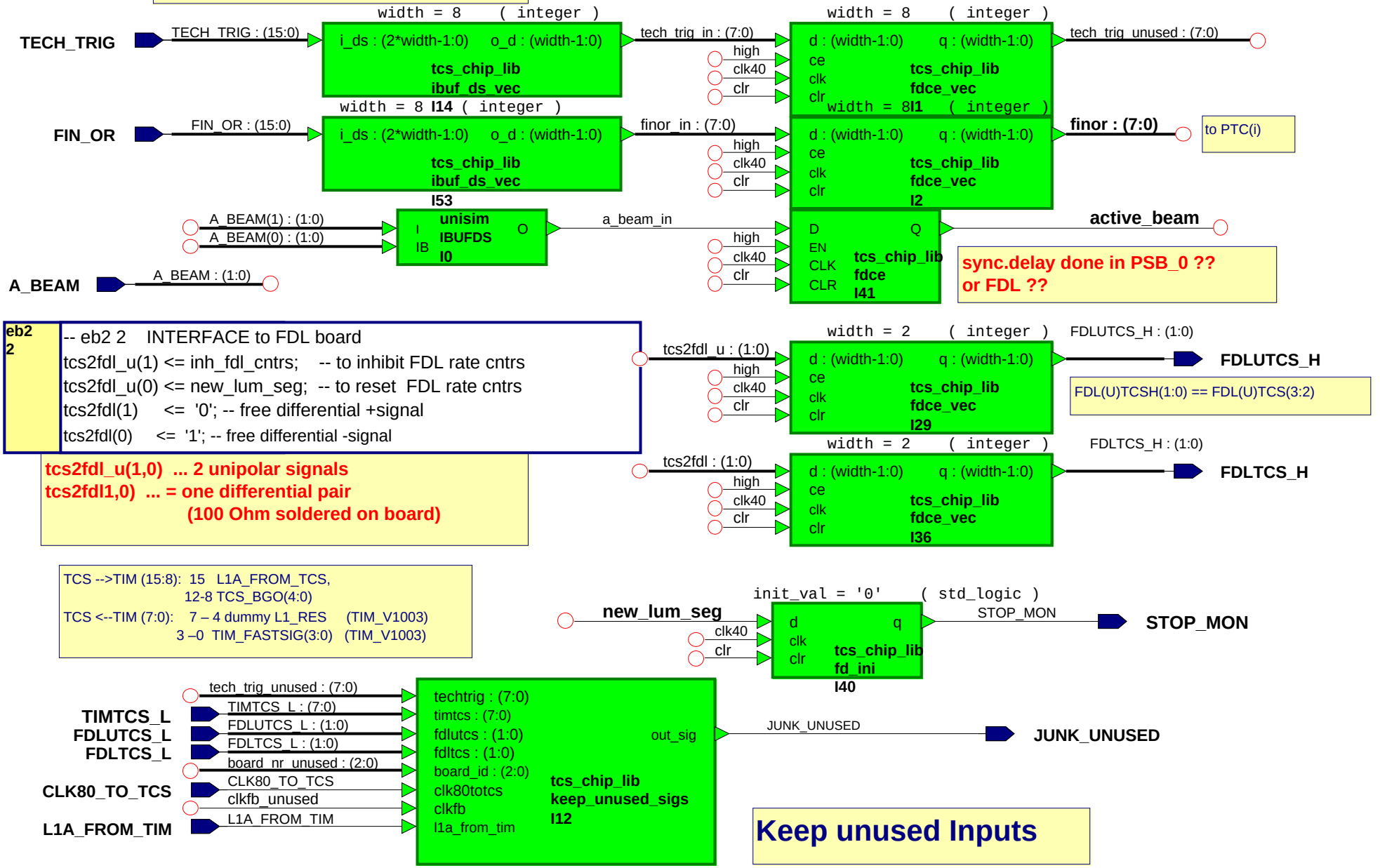
```
A_BEAM                : std_logic_vector(1 DOWNTO 0)
BCRES_FROM_TIM        : std_logic
CLK80_TO_TCS          : std_logic
CLK_FBIN_TCS          : std_logic
CLK_TO_TCS            : std_logic
EN_TCS                : std_logic
F3124                 : std_logic_vector(31 DOWNTO 0)
FASTIN                : std_logic_vector(81 DOWNTO 0)
FASTIN_CYC            : std_logic
FDLTCS_L              : std_logic_vector(1 DOWNTO 0)
FDLUTCS_L             : std_logic_vector(1 DOWNTO 0)
FIN_OR                : std_logic_vector(15 DOWNTO 0)
ID                    : std_logic_vector(2 DOWNTO 0)
INACTIVE              : std_logic
L1A_FROM_TIM          : std_logic
L1RES_FROM_TIM        : std_logic
RESET_TCS_CHIP        : std_logic
SW_DISPLAY            : std_logic
TECH_TRIG             : std_logic_vector(15 DOWNTO 0)
TIMTCS_L              : std_logic_vector(7 DOWNTO 0)
VA_I                  : std_logic_vector(19 DOWNTO 1)
WR_TCS                : std_logic
BCD0                  : std_logic_vector(3 DOWNTO 0)
BCD1                  : std_logic_vector(3 DOWNTO 0)
CLK_FBOUT_TCS         : std_logic
CLK_LOCKED_TCS        : std_logic
DAQ_BCD               : std_logic_vector(3 DOWNTO 0)
EVM_CLK               : std_logic
EVM_D                 : std_logic_vector(27 DOWNTO 0)
FDLTCS_H              : std_logic_vector(1 DOWNTO 0)
FDLUTCS_H             : std_logic_vector(1 DOWNTO 0)
GCLK0S                : std_ulogic
IRQ_X                 : std_logic
JUNK_UNUSED           : std_logic
LUM                   : std_logic_vector(3 DOWNTO 0)
MON_F3124             : std_logic_vector(31 DOWNTO 0)
NDTACK_TCS            : std_logic
NEN_BUSSW             : std_logic
NEN_EVMLINK           : std_logic
NEN_FASTSIGS          : std_logic
NEN_OUT_DAQ           : std_logic
NEN_OUT_PART          : std_logic
NL1A_TCS_LED          : std_logic
NL1A_TCS_MON          : std_logic
NSTATUS_LED           : std_logic_vector(2 DOWNTO 0)
OUT_DAQ0              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ1              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ2              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ3              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ4              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ5              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ6              : std_logic_vector(3 DOWNTO 0)
OUT_DAQ7              : std_logic_vector(3 DOWNTO 0)
OUT_PART24            : std_logic_vector(3 DOWNTO 1)
OUT_PART25            : std_logic_vector(3 DOWNTO 1)
OUT_PART26            : std_logic_vector(3 DOWNTO 1)
OUT_PART27            : std_logic_vector(3 DOWNTO 1)
OUT_PART28            : std_logic_vector(3 DOWNTO 1)
OUT_PART29            : std_logic_vector(3 DOWNTO 1)
OUT_PART30            : std_logic_vector(3 DOWNTO 1)
OUT_PART31            : std_logic_vector(3 DOWNTO 1)
STOP_MON              : std_logic
TEST1_TCS             : std_logic
TEST2_TCS             : std_logic
```

Package List

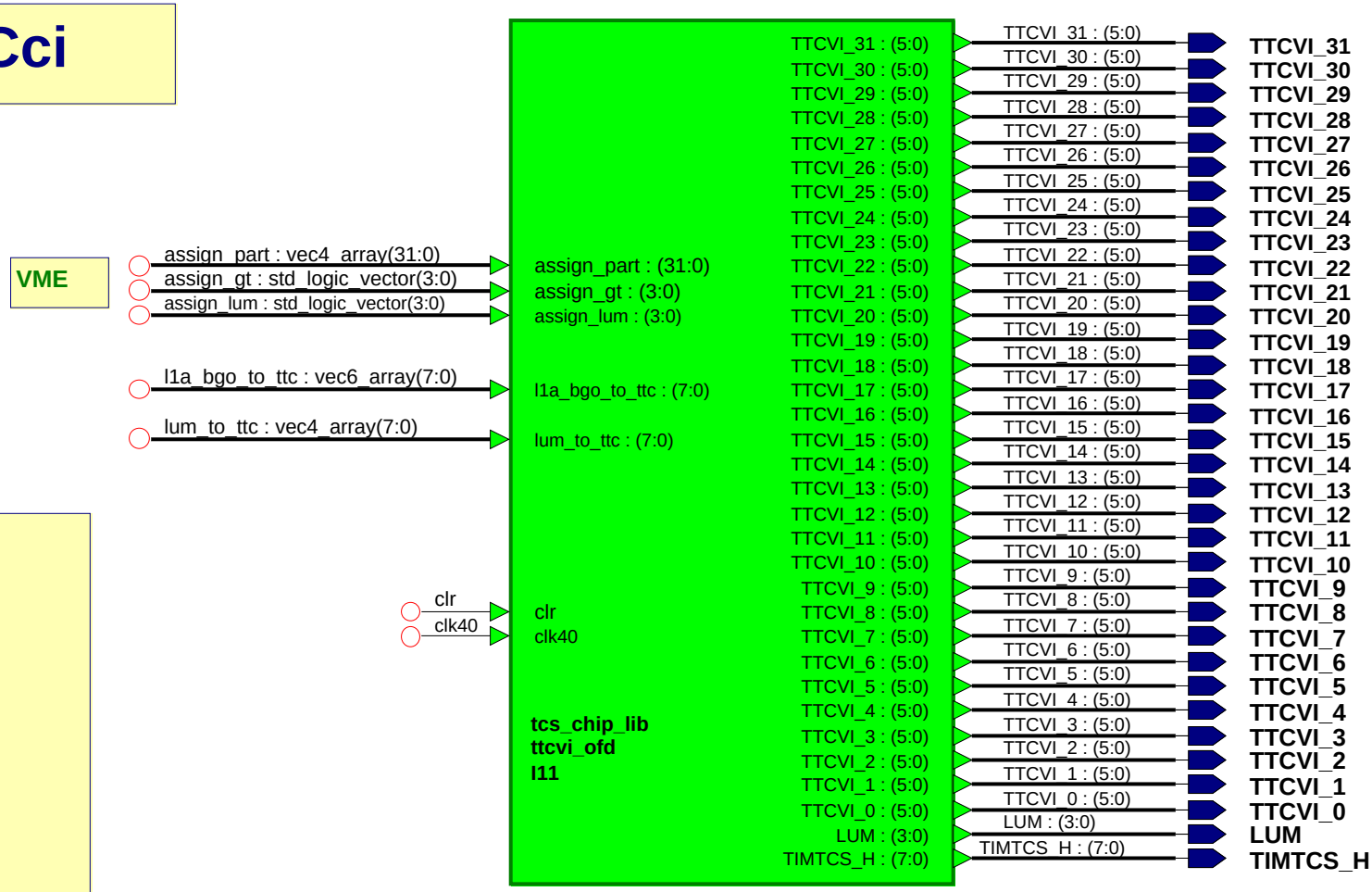
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
LIBRARY unisim;
USE unisim.VCOMPONENTS.all;
USE IEEE.VITAL_Timing.all;
LIBRARY STD;
USE STD.TEXTIO.all;
USE unisim.VPKG.all;
LIBRARY tcs_types;
USE tcs_types.tcs.all;
USE IEEE.VITAL_Primitives.all;
LIBRARY tcs_chip_lib;
USE tcs_chip_lib.all;
```

Vienna		Project:	tcsv2
Title:	TCS CHIP	**Initial values defined in tcs_types.tcs_init_val_pkg.vhd**	
Path:	tcs_chip_lib/tcs_chip/struct		
Edited:	by taurok on 23 Mär 2010		

I/O FDL board


TECH_TRIG
TECH_TRIG : (15:0)
width = 8 (integer)
i_ds : (2*width-1:0) o_d : (width-1:0)
tcs_chip_lib
ibuf_ds_vec
tech_trig_in : (7:0)
high
clk40
clr
width = 8 (integer)
d : (width-1:0) q : (width-1:0)
ce
clk
clr
tcs_chip_lib
fdce_vec
tech_trig_unused : (7:0)
FIN_OR
FIN_OR : (15:0)
width = 8 I14 (integer)
i_ds : (2*width-1:0) o_d : (width-1:0)
tcs_chip_lib
ibuf_ds_vec
I53
finor_in : (7:0)
width = 8 I1 (integer)
d : (width-1:0) q : (width-1:0)
tcs_chip_lib
fdce_vec
I2
finor : (7:0)
to PTC(i)
A_BEAM(1) : (1:0)
A_BEAM(0) : (1:0)
I
IB
unisim
IBUFDS
O
I0
a_beam_in
D
EN
CLK
CLR
Q
tcs_chip_lib
fdce
I41
active_beam
sync.delay done in PSB_0 ??
or FDL ??
A_BEAM
A_BEAM : (1:0)
eb2
2
-- eb2 2 INTERFACE to FDL board
tcs2fdl_u(1) <= inh_fdl_cntrs; -- to inhibit FDL rate cntrs
tcs2fdl_u(0) <= new_lum_seg; -- to reset FDL rate cntrs
tcs2fdl(1) <= '0'; -- free differential +signal
tcs2fdl(0) <= '1'; -- free differential -signal
tcs2fdl_u(1,0) ... 2 unipolar signals
tcs2fdl1,0) ... = one differential pair
(100 Ohm soldered on board)
tcs2fdl_u : (1:0)
width = 2 (integer)
d : (width-1:0) q : (width-1:0)
tcs_chip_lib
fdce_vec
I29
FDLUTCS_H : (1:0)
FDLUTCS_H
FDL(U)TCSH(1:0) == FDL(U)TCS(3:2)
tcs2fdl : (1:0)
width = 2 (integer)
d : (width-1:0) q : (width-1:0)
tcs_chip_lib
fdce_vec
I36
FDLTCS_H : (1:0)
FDLTCS_H
TCS -->TIM (15:8): 15 L1A_FROM_TCS,
12-8 TCS_BGO(4:0)
TCS <--TIM (7:0): 7 – 4 dummy L1_RES (TIM_V1003)
3 –0 TIM_FASTSIG(3:0) (TIM_V1003)
new_lum_seg
init_val = '0' (std_logic)
d
clk
clr
q
tcs_chip_lib
fd_ini
I40
STOP_MON
STOP_MON
tech_trig_unused : (7:0)
TIMTCS_L
FDLUTCS_L
FDLTCS_L
board_nr_unused : (2:0)
CLK80_TO_TCS
clkfb_unused
L1A_FROM_TIM
techtrig : (7:0)
timtcs : (7:0)
fdlutcs : (1:0)
fdltcs : (1:0)
board_id : (2:0)
clk80totcs
clkfb
l1a_from_tim
out_sig
tcs_chip_lib
keep_unused_sigs
I12
JUNK_UNUSED
JUNK_UNUSED
Keep unused Inputs

OUTPUT to TTCci



BGO Codes

1 BC0
2 TE test enable
3 Private Gap
4 Private Orbit
5 Resync
6 HardRes
7 EC0 Event counter reset
8 OC0 Orbit counter reset
9 Start
A Stop
B Start of Gap
C ---
D WTE Warning TestEnable

Version History

```
            OLD VERSIONS   2007 - 2008
-- V001C: tim_signal_decoder: res_orbit_cntr simplified as in FDL chip
--            VME logic: vme_enn with vme_en1,2,3
--           Calibration cycle continues regardless of PTC_ready when started.
-- V001B: Finor, random and test trig's concurrently; ev_type from FinOR
--            finor and rndm trig's allowed as defined by valid_bc of bc-table
--            Dead-time cntr's incremented alternatively when either valid_bc =1 or when
--           active_beam =1 (BPTX detector)
-- V001A:  lost triggers: error corrected
-- V0019: lumi_cntr: ld_new_lumsegm...resets when a new value is loaded
--   New initial values: lum_segm_period=X"4000"=1,46s; trigger types..all assigned
-- V0018: ptc_cntrs: trig_cntrs...error removed
--     rop_bcr_delay ...zu get correct bcnr in event record
--     periodic_proc: 100Hz Generator added
-- V0017: new_lum_seg --> TCSM(stop_mon) to save&clear status counters
--    trigger:     Inhibit random trigger in invalid BCs(gaps, no collision)
--    PTC_SM:  resync2 --> res_evnr2 when in IDLE mode; required for HCAL, ECAL
--    bgo_ctrl:  inhibit L1A around BGo removed
-- V0016:  reset orbit counter by PTC0 : bgo_ctrl, tim_signal_decoder modified, requestFF
--             TCS-->FDL:  new_lum_seg --> FDLTCSH(0) and FDLUTCSH(0)
--                                freeze      ....not implemented
--      PTC_SM: resync0 --> init...and continue run
--     ROP: include 'tcs2daq' (=ptc_status) into record
--     'rndm_prescale_fact'....prescaler for random trigger
-- V0015:          ... TO BE USED in GLOBAL RUN Nov.2007
--                    BAD CODE problem is postponed to a later version.
--      PTC_SM:
--            Starts independently from input status.
--            PANIC BUTTON returns ptc_sm to IDLE status if 'done' bit is missing
--                 because the BC-table does not contain the bit for this BGo command.
--            ptc_clears_orbitnr = '1' ..optional reset of orbit counter
--            IDLE:stop_run_fsm_cld <= '1' ; ' =ignore old stop request
--             'hard_res' is possible when in out_of_sync status
```

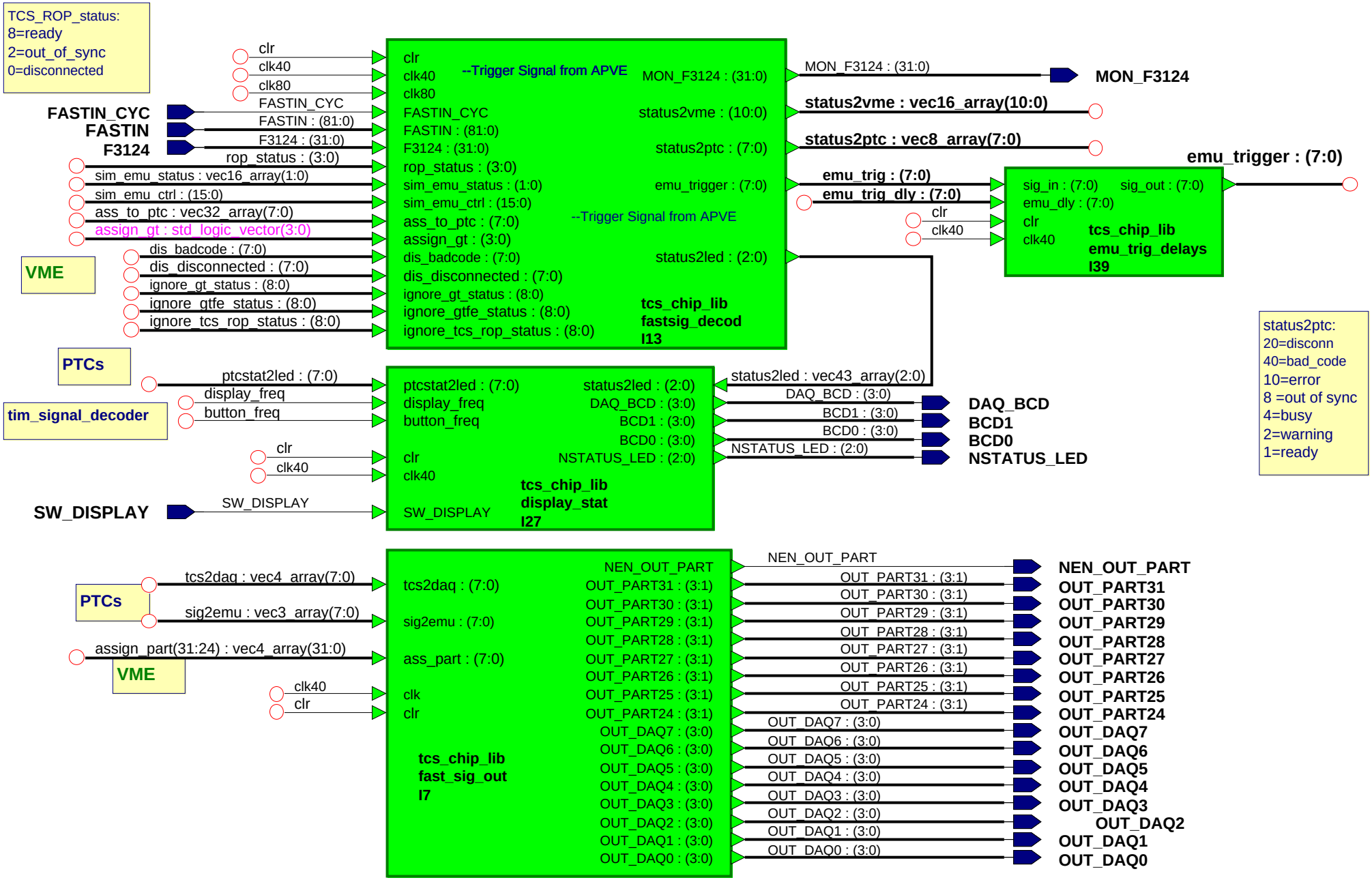
```
      OLD VERSIONS   until 2007
V0014: testmask0-7 bits added,   ... TO BE USED in GLOBAL RUN Nov.2007
V0013: trigger, bgo_ctrl, vme_decoder_tcs, vme registers_tcs: 'not' set between (...)
         vme_decoder_tcs:  dtck_wff delayed by 1 tick
         ptc_sm: After Hardres do a Resync procedure
V0012: bgo_ctrl: removed FF for Emu signals to add OUTFF in 'fast_sig_out' module'
          PTC_SM : resync from error possible, inc_res_cntr inserted
           States out_of_sync+error: --  sensible to 'disconnected' input.
                                              --  can return to busy when err/outsync disappear
V0011: PTC_SM : resync and hardres is possible from warn,ready,busy states
V0010: Evnr+TrigNr start with =1 as in GTFE, board_id =cc07
         Display unit
V000F: pipeline instead of roc state machine sends event records to GTFE
V000E: rop without CASE..--> same as V000D
V000D: test_mask8 bits, nen_evmlink
V000C: PTC-SM with resync,hardres; test_mask bits,
       EMU output corrected
      +/-2bx deadtime around Bgo commands
       new deadtime counter:  +/-2bx around BC0; StartofGap
V000B: Monitoring counters,
       PTC-SM without automatic resync; fsm_states register
V000A: fast_sig_decoder
V0009: fast_sig_decod, dtack for ptc_cmd_puls
V0008: first version,
```

```
TEST2_TCS                : std_logic
TIMTCS_H                 : std_logic_vector(7 DOWNTO 0)
TTCVI_0                  : std_logic_vector(5 DOWNTO 0)
TTCVI_1                  : std_logic_vector(5 DOWNTO 0)
TTCVI_10                 : std_logic_vector(5 DOWNTO 0)
TTCVI_11                 : std_logic_vector(5 DOWNTO 0)
TTCVI_12                 : std_logic_vector(5 DOWNTO 0)
TTCVI_13                 : std_logic_vector(5 DOWNTO 0)
TTCVI_14                 : std_logic_vector(5 DOWNTO 0)
TTCVI_15                 : std_logic_vector(5 DOWNTO 0)
TTCVI_16                 : std_logic_vector(5 DOWNTO 0)
TTCVI_17                 : std_logic_vector(5 DOWNTO 0)
TTCVI_18                 : std_logic_vector(5 DOWNTO 0)
TTCVI_19                 : std_logic_vector(5 DOWNTO 0)
TTCVI_2                  : std_logic_vector(5 DOWNTO 0)
TTCVI_20                 : std_logic_vector(5 DOWNTO 0)
TTCVI_21                 : std_logic_vector(5 DOWNTO 0)
TTCVI_22                 : std_logic_vector(5 DOWNTO 0)
TTCVI_23                 : std_logic_vector(5 DOWNTO 0)
TTCVI_24                 : std_logic_vector(5 DOWNTO 0)
TTCVI_25                 : std_logic_vector(5 DOWNTO 0)
TTCVI_26                 : std_logic_vector(5 DOWNTO 0)
TTCVI_27                 : std_logic_vector(5 DOWNTO 0)
TTCVI_28                 : std_logic_vector(5 DOWNTO 0)
TTCVI_29                 : std_logic_vector(5 DOWNTO 0)
TTCVI_3                  : std_logic_vector(5 DOWNTO 0)
TTCVI_30                 : std_logic_vector(5 DOWNTO 0)
TTCVI_31                 : std_logic_vector(5 DOWNTO 0)
TTCVI_4                  : std_logic_vector(5 DOWNTO 0)
TTCVI_5                  : std_logic_vector(5 DOWNTO 0)
TTCVI_6                  : std_logic_vector(5 DOWNTO 0)
TTCVI_7                  : std_logic_vector(5 DOWNTO 0)
TTCVI_8                  : std_logic_vector(5 DOWNTO 0)
TTCVI_9                  : std_logic_vector(5 DOWNTO 0)
VD_I                     : std_logic_vector(15 DOWNTO 0)
```

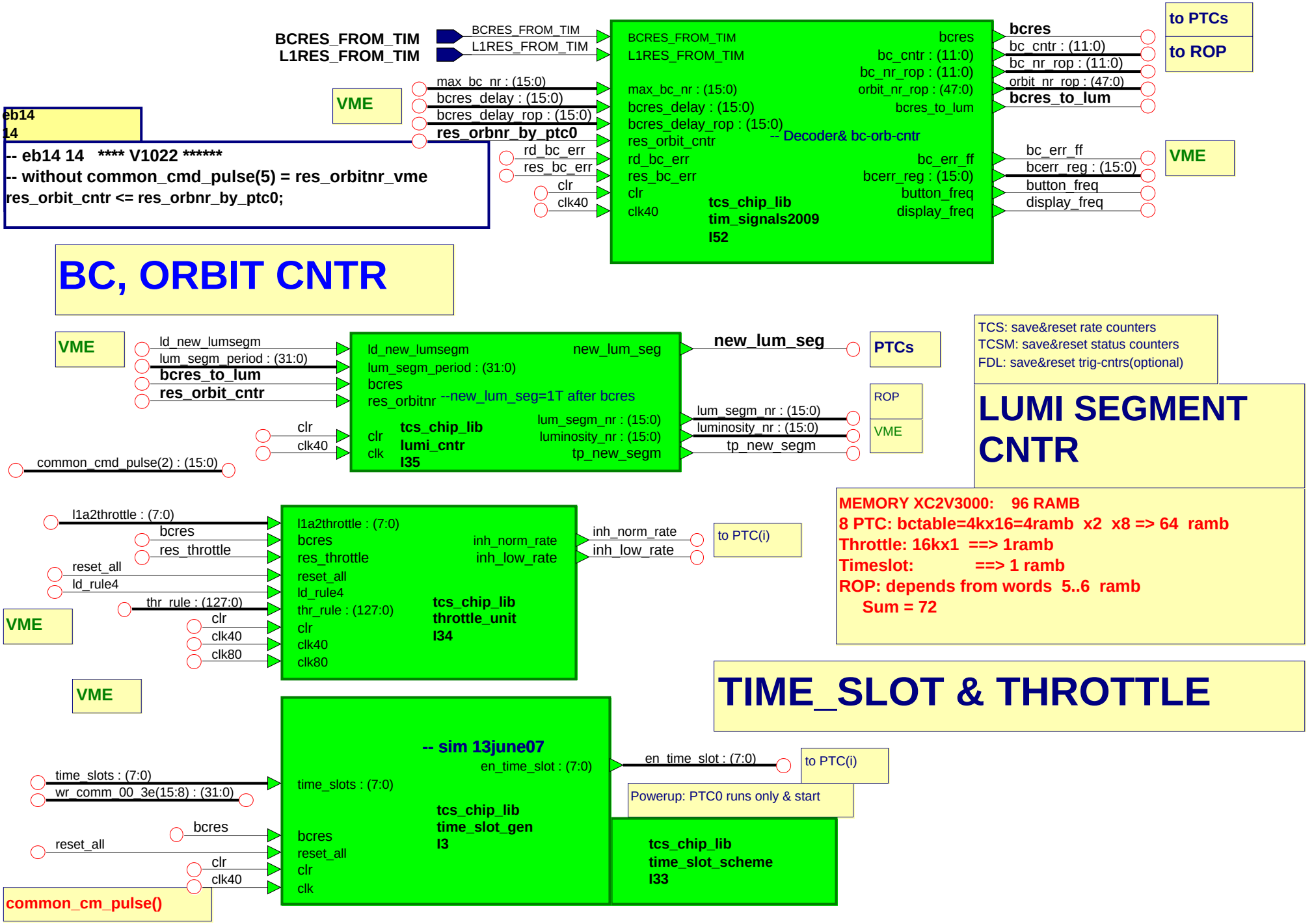
Diagram Signals:

```
SIGNAL CLK0                 : std_ulogic := '0'
SIGNAL CLK180               : std_ulogic := '0'
SIGNAL CLK2X                : std_ulogic := '0'
SIGNAL CLK2X180             : std_ulogic := '0'
SIGNAL CLKIN                : std_logic
SIGNAL a_beam_in            : std_logic
SIGNAL active_beam          : std_logic
SIGNAL ass_to_ptc           : vec32_array(7 DOWNTO 0)
SIGNAL assign_gt            : std_logic_vector(3 DOWNTO 0)
SIGNAL assign_lum           : std_logic_vector(3 DOWNTO 0)
SIGNAL assign_part          : vec4_array(31 DOWNTO 0)
SIGNAL bc_cntr              : std_logic_vector(11 downto 0)
SIGNAL bc_err_ff            : std_logic
SIGNAL bc_nr_rop            : std_logic_vector(11 DOWNTO 0)
SIGNAL bcerr_reg            : std_logic_vector(15 DOWNTO 0)
SIGNAL bcres                : std_logic
SIGNAL bcres_delay          : std_logic_vector(15 DOWNTO 0)
SIGNAL bcres_delay_rop      : std_logic_vector(15 DOWNTO 0)
SIGNAL bcres_to_lum         : std_logic
SIGNAL bgo_period_l         : vec16_array(7 DOWNTO 0)
SIGNAL bgo_period_s         : vec16_array(7 DOWNTO 0)
SIGNAL board_id             : std_logic_vector(15 DOWNTO 0)
SIGNAL board_nr_unused      : std_logic_vector(2 DOWNTO 0)
SIGNAL button_freq          : std_logic
SIGNAL clk40                : std_logic
SIGNAL clk80                : std_logic
SIGNAL clkfb_unused         : STD_ULOGIC
SIGNAL clr                  : std_logic
SIGNAL common_cmd_pulse     : std_logic_vector(15 DOWNTO 0)
SIGNAL common_status        : std_logic_vector(15 DOWNTO 0)
SIGNAL dcm_locked           : std_logic
```

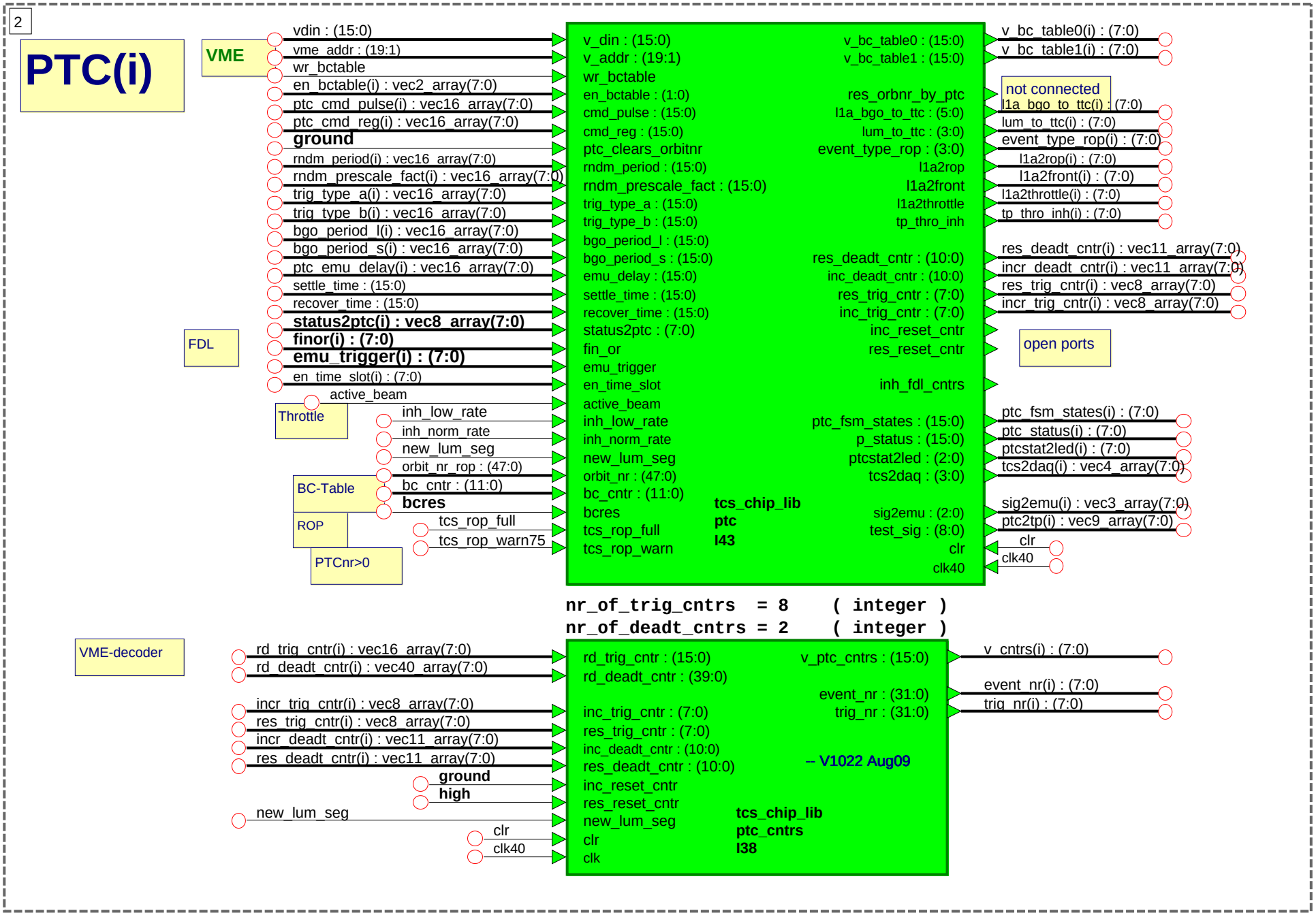
```
                    LAST VERSIONS
-- V1024: trigger :use 'active_bc_ff'  for counting nr. of 'FIN_ORs in invalid BC'
-- V1023:  ==>Decoding signals BCres, L1Res from TIM boards.
--  ==>  Emulator trigger signals added
--       new registers & deadtime cntrs, new "trigger_type"
--      Module ' emu_trig_delays' added,
--      Modules 'fastsig_decod', 'ptc', 'trigger', 'ptc_cntrs',
--                  'vme_decoder_tcs'  modified
-- V1022:  Updated ISE10.1, FPAdv82
--       common_cmd_pulse(5) = ' res_orbit_vme'  removed
--       All memories, fifo redone with ISE10.1
--       ptc_cntrs: Trigger & eventnr. return to 0 after overflow!!
--       ptc_cntrs: Accept trigger also at begin of luminosity segment.
--       trigger :  'inhibit fdl rate counters' 3bx before inhibiting the finor signal
-- V1021:  "trigger" : Inhibit Rate Counters on the FDL board
--                          during a calibration cycle. IO-pin:FDLTCS_H(1)
-- V1020:  "tim_signals2009" : bcnr_rop & orb_nr_rop & lum_seg_nr
--                switch concurrently.
-- V101F: "bgo_ctrl": state machine for HardRes and Resync logic
--           "calibr_sm": caltrig is sent immediately
--    vme_registers_tcs: Power-up values are taken from
--            tcs_types.tcs_init_val_pkg.vhd and are defined in
--           ... \tcs_chip\ucf_files\tcs_reg_list.xls
--   ptc_test point:  bgo_strobe added
-- V001E: "bgo_ctrl": long waiting time after HARDRES,
--            BC_table1(22):= 'end_of_calibration_cycle' -->
--           "calibr_sm": triggers are inhibited between
--           'test_en' and  'end_of_calibration_cycle' or after 255 bc.
--           trigger:  caltrig never inhibited by anyone!
-- V001D: error triggers ignore inhibit signal from state machine
```



IN/OUT to DET_PART'S, EMULATORS, DAQ_PART'S


BCRES_FROM_TIM
L1RES_FROM_TIM
BCRES_FROM_TIM
L1RES_FROM_TIM
VME
max_bc_nr : (15:0)
bcres_delay : (15:0)
bcres_delay_rop : (15:0)
res_orbnr_by_ptc0
rd_bc_err
res_bc_err
clr
clk40
BCRES_FROM_TIM
L1RES_FROM_TIM
max_bc_nr : (15:0)
bcres_delay : (15:0)
bcres_delay_rop : (15:0)
res_orbit_cntr
rd_bc_err
res_bc_err
clr
clk40
tcs_chip_lib
tim_signals2009
I52
-- Decoder& bc-orb-cntr
bcres
bc_cntr : (11:0)
bc_nr_rop : (11:0)
orbit_nr_rop : (47:0)
bcres_to_lum
bc_err_ff
bcerr_reg : (15:0)
button_freq
display_freq
bcres
bc_cntr : (11:0)
bc_nr_rop : (11:0)
orbit_nr_rop : (47:0)
bcres_to_lum
bc_err_ff
bcerr_reg : (15:0)
button_freq
display_freq
to PTCs
to ROP
VME
eb14
14
-- eb14 14 **** V1022 ******
-- without common_cmd_pulse(5) = res_orbitnr_vme
res_orbit_cntr <= res_orbnr_by_ptc0;
BC, ORBIT CNTR
VME
ld_new_lumsegm
lum_segm_period : (31:0)
bcres_to_lum
res_orbit_cntr
clr
clk40
common_cmd_pulse(2) : (15:0)
ld_new_lumsegm
lum_segm_period : (31:0)
bcres
res_orbitnr
--new_lum_seg=1T after bcres
clr
clk
tcs_chip_lib
lumi_cntr
I35
new_lum_seg
lum_segm_nr : (15:0)
luminosity_nr : (15:0)
tp_new_segm
new_lum_seg
PTCs
ROP
VME
lum_segm_nr : (15:0)
luminosity_nr : (15:0)
tp_new_segm
TCS: save&reset rate counters
TCSM: save&reset status counters
FDL: save&reset trig-cntrs(optional)
LUMI SEGMENT CNTR
MEMORY XC2V3000: 96 RAMB
8 PTC: bctable=4kx16=4ramb x2 x8 => 64 ramb
Throttle: 16kx1 ==> 1ramb
Timeslot: ==> 1 ramb
ROP: depends from words 5..6 ramb
Sum = 72
l1a2throttle : (7:0)
bcres
res_throttle
reset_all
ld_rule4
thr_rule : (127:0)
clr
clk40
clk80
VME
l1a2throttle : (7:0)
bcres
res_throttle
reset_all
ld_rule4
thr_rule : (127:0)
clr
clk40
clk80
tcs_chip_lib
throttle_unit
I34
inh_norm_rate
inh_low_rate
inh_norm_rate
inh_low_rate
to PTC(i)
VME
TIME_SLOT & THROTTLE
time_slots : (7:0)
wr_comm_00_3e(15:8) : (31:0)
bcres
reset_all
clr
clk40
common_cm_pulse()
-- sim 13june07
time_slots : (7:0)
bcres
reset_all
clr
clk
tcs_chip_lib
time_slot_gen
I3
en_time_slot : (7:0)
en_time_slot : (7:0)
to PTC(i)
Powerup: PTC0 runs only & start
tcs_chip_lib
time_slot_scheme
I33

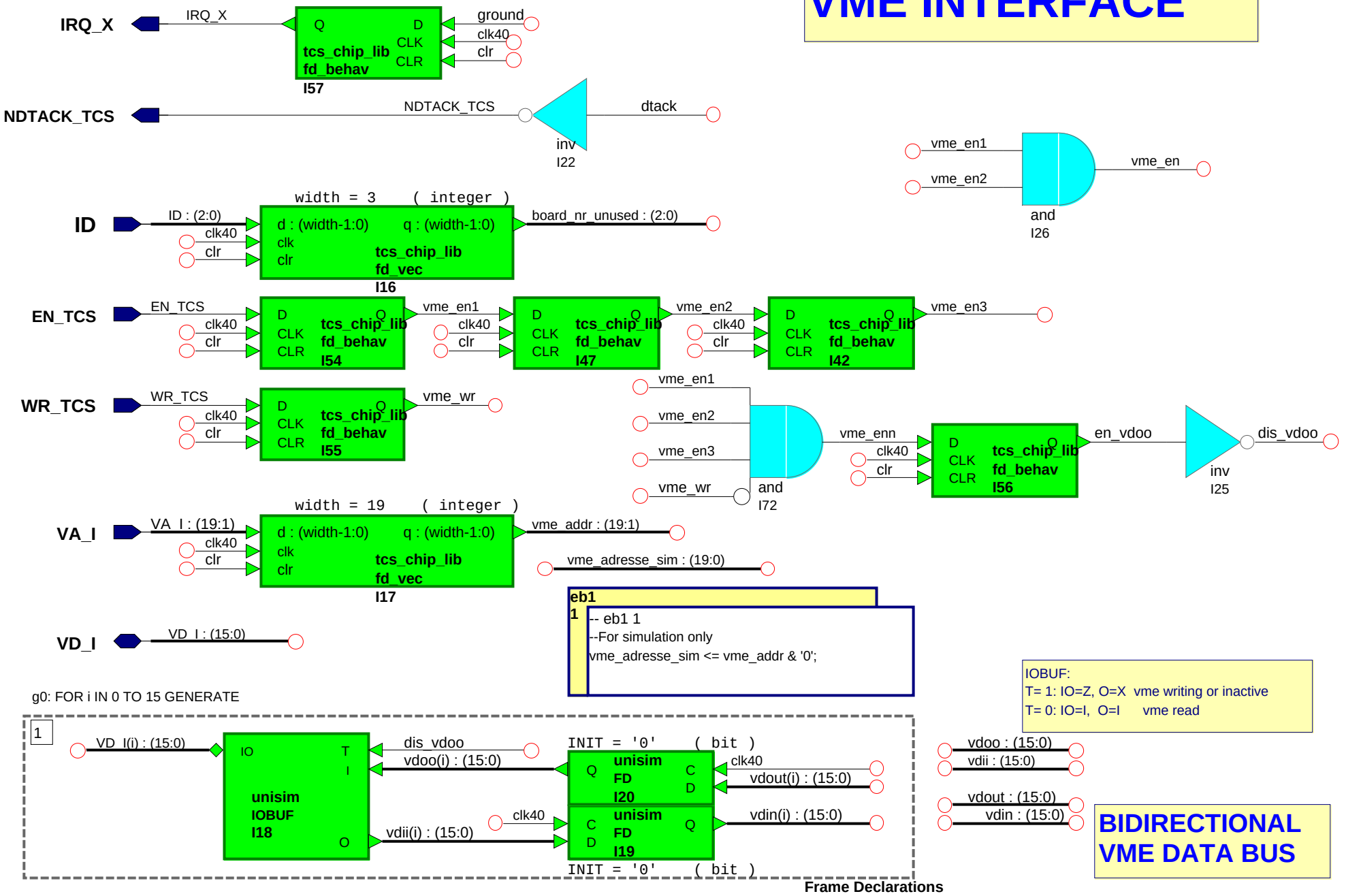
PTC1_7: FOR i IN 1 TO 7 GENERATE



Frame Declarations

```
SIGNAL dcm_locked            : std_logic
SIGNAL dis_badcode           : std_logic_vector(7 DOWNTO 0)
SIGNAL dis_disconnected      : std_logic_vector(7 DOWNTO 0)
SIGNAL dis_vdoo              : std_logic
SIGNAL disable_io            : std_logic_vector(3 DOWNTO 0)
SIGNAL display_freq          : std_logic
SIGNAL dout                  : std_logic
SIGNAL dtack                 : std_logic
SIGNAL emu_trig              : std_logic_vector(7 DOWNTO 0)
SIGNAL emu_trig_dly          : vec16_array(7 DOWNTO 0)
SIGNAL emu_trigger           : std_logic_vector(7 DOWNTO 0)
SIGNAL en_bctable            : vec2_array(7 DOWNTO 0)
SIGNAL en_time_slot          : std_logic_vector(7 DOWNTO 0)
SIGNAL en_vdoo               : std_logic
SIGNAL event_nr              : vec32_array(7 DOWNTO 0)
SIGNAL event_type_rop        : vec4_array(7 DOWNTO 0)
SIGNAL finor                 : std_logic_vector(7 DOWNTO 0)
SIGNAL finor_in              : std_logic_vector(7 DOWNTO 0)
SIGNAL gnd_2                 : std_logic_vector(1 DOWNTO 0)
SIGNAL ground                : std_logic
SIGNAL gsr                   : STD_ULOGIC
SIGNAL gts                   : std_ulogic
SIGNAL high                  : std_logic
SIGNAL ignore_gt_status      : std_logic_vector(8 DOWNTO 0)
SIGNAL ignore_gtfe_status    : std_logic_vector(8 DOWNTO 0)
SIGNAL ignore_tcs_rop_status : std_logic_vector(8 DOWNTO 0)
SIGNAL inc_reset_cntr        : std_logic
SIGNAL incr_deadt_cntr       : vec11_array(7 DOWNTO 0)
SIGNAL incr_trig_cntr        : vec8_array(7 DOWNTO 0)
SIGNAL inh_fdl_cntrs         : std_logic
SIGNAL inh_low_rate          : std_logic
SIGNAL inh_norm_rate         : std_logic
SIGNAL l1a2front             : std_logic_vector(7 DOWNTO 0)
SIGNAL l1a2rop               : std_logic_vector(7 DOWNTO 0)
SIGNAL l1a2throttle          : std_logic_vector(7 DOWNTO 0)
SIGNAL l1a_bgo_to_ttc        : vec6_array(7 DOWNTO 0)
SIGNAL ld_new_lumsegm        : std_logic
SIGNAL ld_rule4              : std_logic
SIGNAL lum_segm_nr           : std_logic_vector(15 DOWNTO 0)
SIGNAL lum_segm_period       : std_logic_vector(31 DOWNTO 0)
SIGNAL lum_to_ttc            : vec4_array(7 DOWNTO 0)
SIGNAL luminosity_nr         : std_logic_vector(15 DOWNTO 0)
SIGNAL max_bc_nr             : std_logic_vector(15 downto 0)
SIGNAL nclk40                : std_logic
SIGNAL nclk80                : std_logic
SIGNAL new_lum_seg           : std_logic
SIGNAL orbit_nr_rop          : std_logic_vector(47 DOWNTO 0)
SIGNAL part_run_nr           : vec32_array(7 DOWNTO 0)
SIGNAL ptc0_clears_orbitnr   : std_logic
SIGNAL ptc2tp                : vec9_array(7 DOWNTO 0)
SIGNAL ptc2tp0               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp1               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp2               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp3               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp4               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp5               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp6               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc2tp7               : std_logic_vector(8 DOWNTO 0)
SIGNAL ptc_cmd_pulse         : vec16_array(7 DOWNTO 0)
SIGNAL ptc_cmd_reg           : vec16_array(7 DOWNTO 0)
SIGNAL ptc_emu_delay         : vec16_array(7 DOWNTO 0)
SIGNAL ptc_fsm_states        : vec16_array(7 DOWNTO 0)
SIGNAL ptc_status            : vec16_array(7 DOWNTO 0)
SIGNAL ptcstat2led           : vec3_array(7 DOWNTO 0)
SIGNAL rd_bc_err             : std_logic
SIGNAL rd_comm_3e            : std_logic
SIGNAL rd_comm_40_6e         : std_logic_vector(23 downto 0)
```

VME INTERFACE



Frame Declarations

VME registers

eb5
5

```
-- eb5 5  --COMMON_STATUS
common_status(15) <= '0';
common_status(14) <= tcs_rop_full;
common_status(13) <= tcs_rop_warn75;
common_status(12) <= tcs_rop_warn50;
common_status(11) <= bc_err_ff;
common_status(10) <= tcs_rop_empty;
common_status(9)   <=  '0';
common_status(8)   <=  '0';
common_status(7 downto 0)   <=  X"00";
```

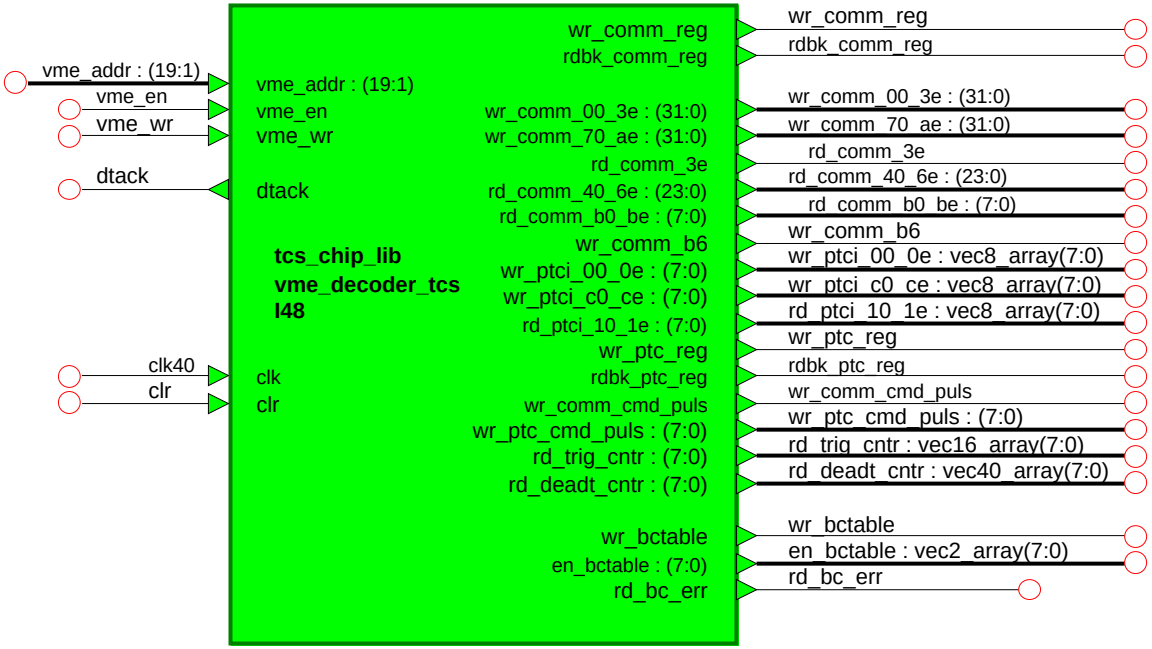
tcs_rop_full
tcs_rop_warn75
bc_err_ff
tcs_rop_empty

common_cmd_pulse : (15:0)

res_bc_err
res_throttle
reset_all

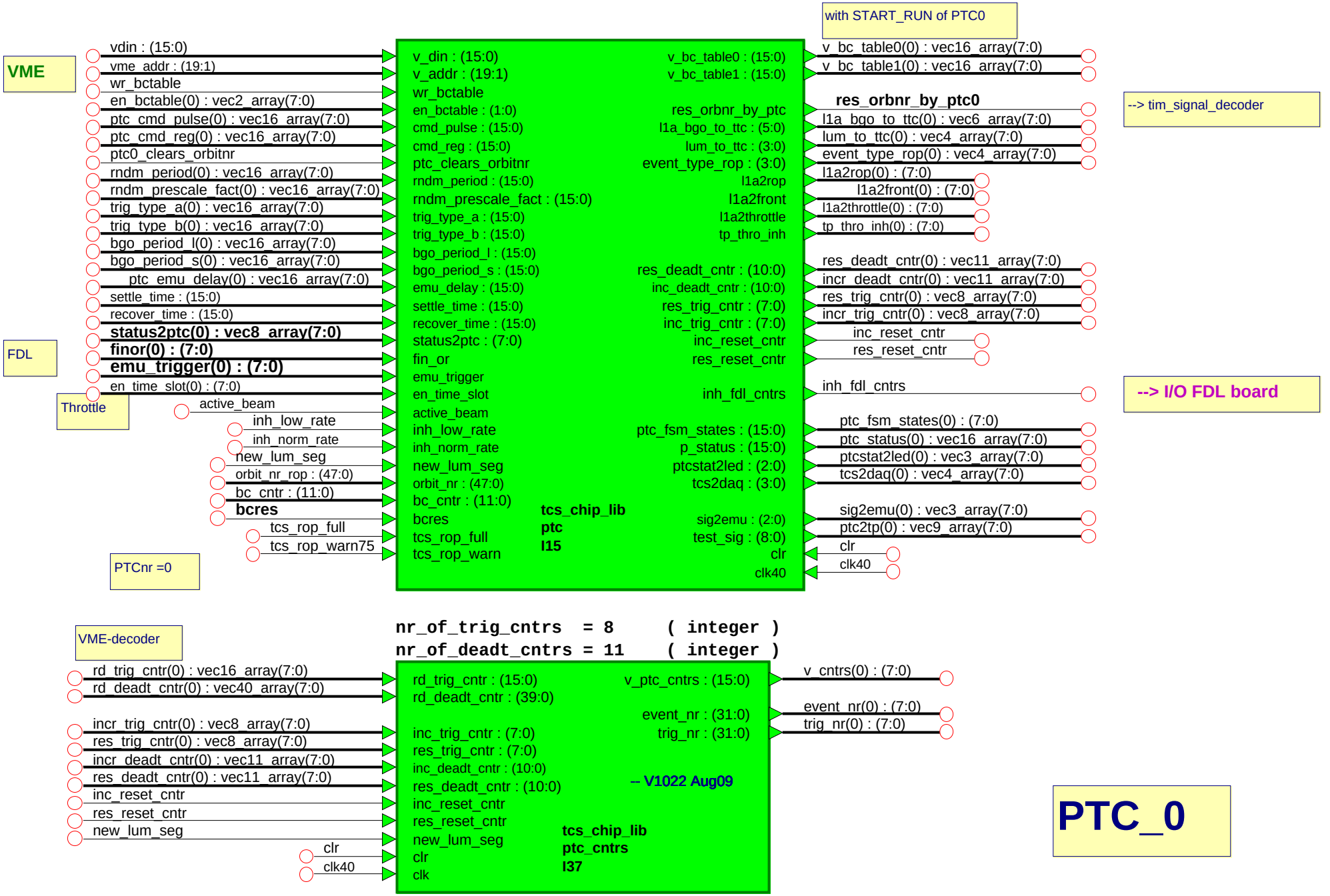
eb16
16

```
-- eb16 16    --COMMON_CMD_PULSE
res_bc_err  <= common_cmd_pulse(4)
                  or common_cmd_pulse(3) ;
reset_all      <= common_cmd_pulse(3);
res_throttle <= common_cmd_pulse(2);
--not used:
--res_trignr  <= common_cmd_pulse(0);
```

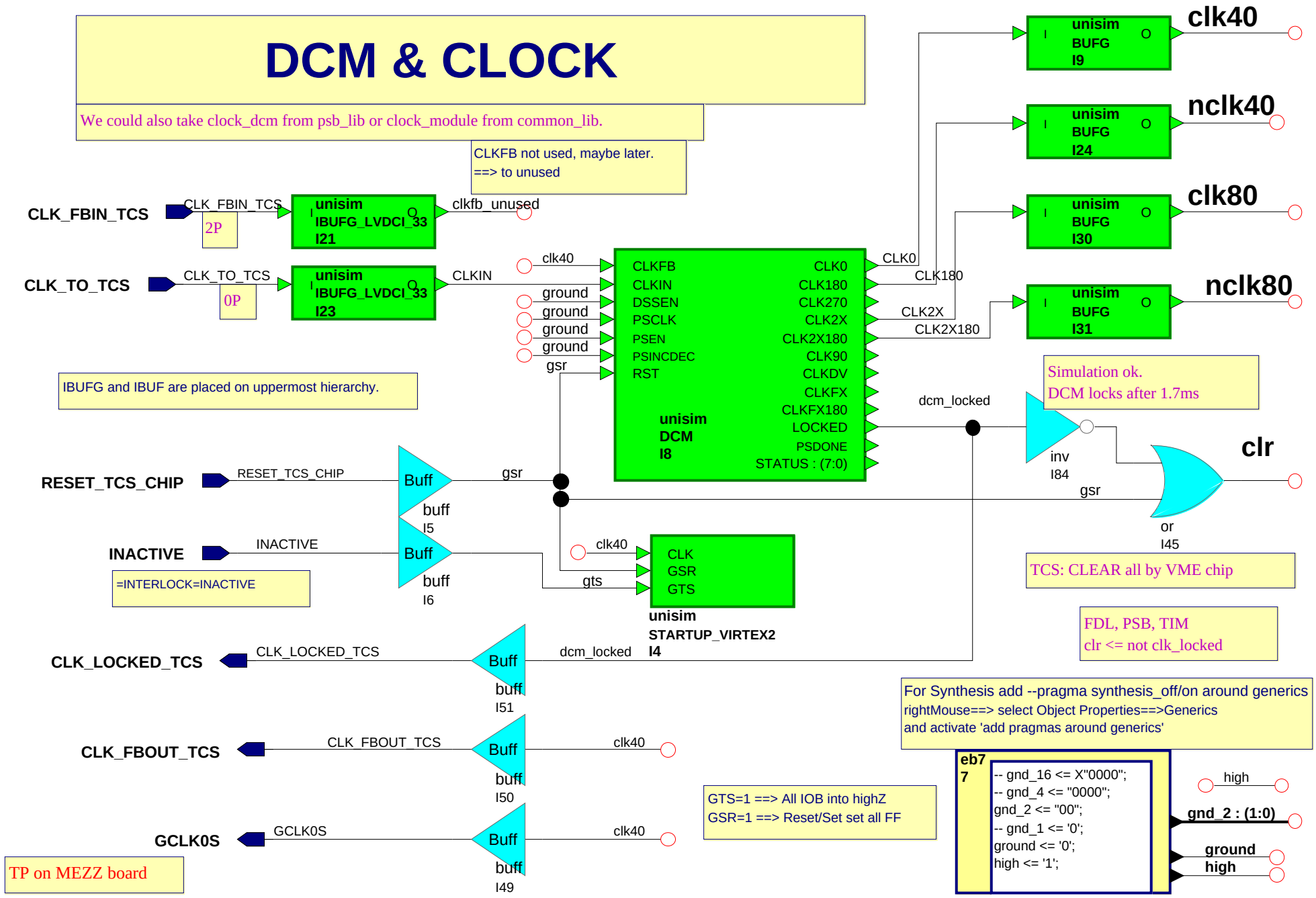


PTC_i w/r regs

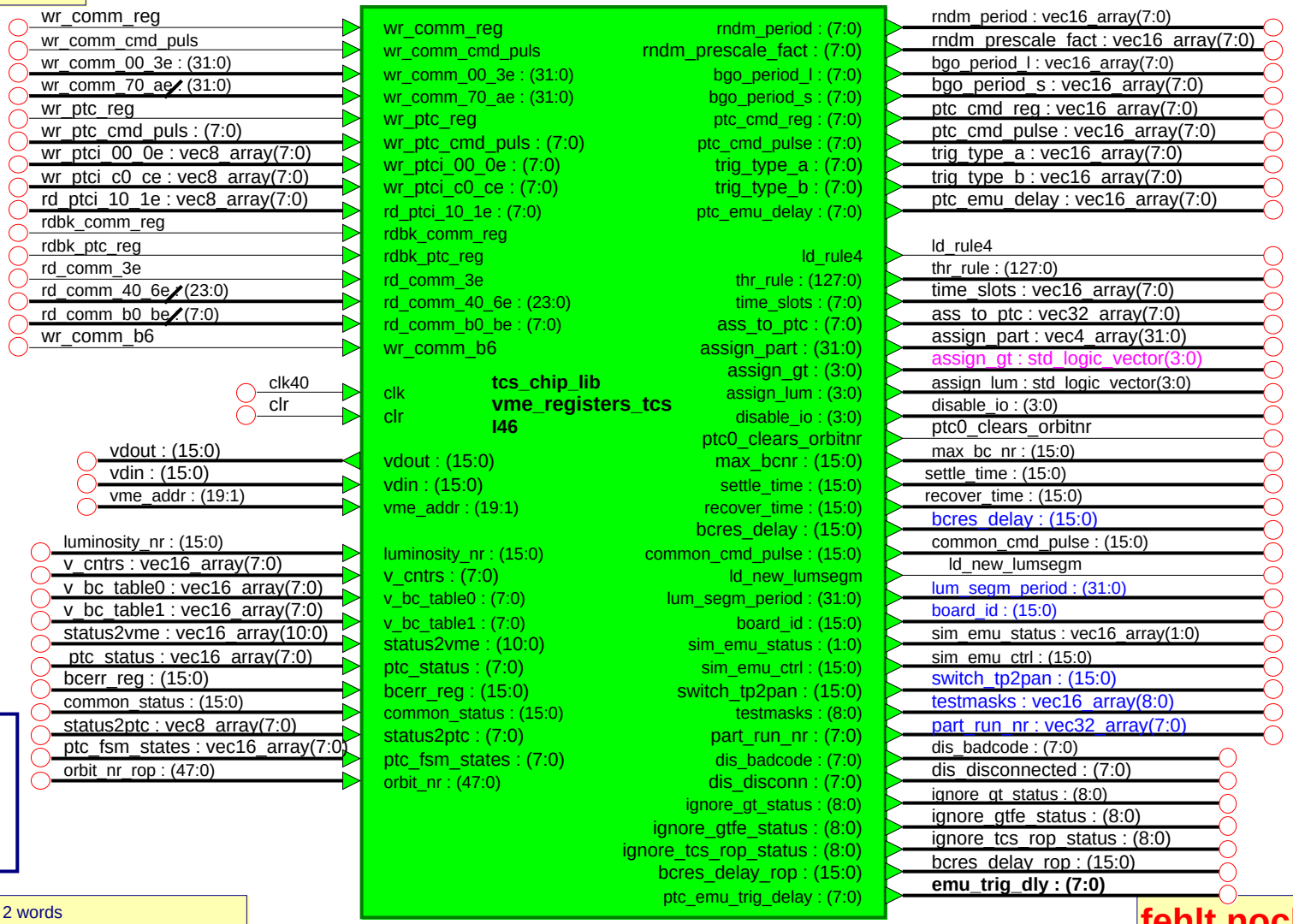
Common w/r regs


with START_RUN of PTC0
VME
vdin : (15:0)
vme_addr : (19:1)
wr_bctable
en_bctable(0) : vec2_array(7:0)
ptc_cmd_pulse(0) : vec16_array(7:0)
ptc_cmd_reg(0) : vec16_array(7:0)
ptc0_clears_orbitnr
rndm_period(0) : vec16_array(7:0)
rndm_prescale_fact(0) : vec16_array(7:0)
trig_type_a(0) : vec16_array(7:0)
trig_type_b(0) : vec16_array(7:0)
bgo_period_l(0) : vec16_array(7:0)
bgo_period_s(0) : vec16_array(7:0)
ptc_emu_delay(0) : vec16_array(7:0)
settle_time : (15:0)
recover_time : (15:0)
status2ptc(0) : vec8_array(7:0)
finor(0) : (7:0)
emu_trigger(0) : (7:0)
en_time_slot(0) : (7:0)
FDL
Throttle
active_beam
inh_low_rate
inh_norm_rate
new_lum_seg
orbit_nr_rop : (47:0)
bc_cntr : (11:0)
bcres
tcs_rop_full
tcs_rop_warn75
PTCnr =0
v_din : (15:0)
v_addr : (19:1)
wr_bctable
en_bctable : (1:0)
cmd_pulse : (15:0)
cmd_reg : (15:0)
ptc_clears_orbitnr
rndm_period : (15:0)
rndm_prescale_fact : (15:0)
trig_type_a : (15:0)
trig_type_b : (15:0)
bgo_period_l : (15:0)
bgo_period_s : (15:0)
emu_delay : (15:0)
settle_time : (15:0)
recover_time : (15:0)
status2ptc : (7:0)
fin_or
emu_trigger
en_time_slot
active_beam
inh_low_rate
inh_norm_rate
new_lum_seg
orbit_nr : (47:0)
bc_cntr : (11:0)
bcres
tcs_rop_full
tcs_rop_warn
tcs_chip_lib
ptc
l15
v_bc_table0 : (15:0)
v_bc_table1 : (15:0)
res_orbnr_by_ptc
l1a_bgo_to_ttc : (5:0)
lum_to_ttc : (3:0)
event_type_rop : (3:0)
l1a2rop
l1a2front
l1a2throttle
tp_thro_inh
res_deadt_cntr : (10:0)
inc_deadt_cntr : (10:0)
res_trig_cntr : (7:0)
inc_trig_cntr : (7:0)
inc_reset_cntr
res_reset_cntr
inh_fdl_cntrs
ptc_fsm_states : (15:0)
p_status : (15:0)
ptcstat2led : (2:0)
tcs2daq : (3:0)
sig2emu : (2:0)
test_sig : (8:0)
clr
clk40
v_bc_table0(0) : vec16_array(7:0)
v_bc_table1(0) : vec16_array(7:0)
res_orbnr_by_ptc0
l1a_bgo_to_ttc(0) : vec6_array(7:0)
lum_to_ttc(0) : vec4_array(7:0)
event_type_rop(0) : vec4_array(7:0)
l1a2rop(0) : (7:0)
l1a2front(0) : (7:0)
l1a2throttle(0) : (7:0)
tp_thro_inh(0) : (7:0)
res_deadt_cntr(0) : vec11_array(7:0)
incr_deadt_cntr(0) : vec11_array(7:0)
res_trig_cntr(0) : vec8_array(7:0)
incr_trig_cntr(0) : vec8_array(7:0)
inc_reset_cntr
res_reset_cntr
inh_fdl_cntrs
ptc_fsm_states(0) : (7:0)
ptc_status(0) : vec16_array(7:0)
ptcstat2led(0) : vec3_array(7:0)
tcs2daq(0) : vec4_array(7:0)
sig2emu(0) : vec3_array(7:0)
ptc2tp(0) : vec9_array(7:0)
clr
clk40
--> tim_signal_decoder
--> I/O FDL board
nr_of_trig_cntrs = 8 (integer)
nr_of_deadt_cntrs = 11 (integer)
VME-decoder
rd_trig_cntr(0) : vec16_array(7:0)
rd_deadt_cntr(0) : vec40_array(7:0)
incr_trig_cntr(0) : vec8_array(7:0)
res_trig_cntr(0) : vec8_array(7:0)
incr_deadt_cntr(0) : vec11_array(7:0)
res_deadt_cntr(0) : vec11_array(7:0)
inc_reset_cntr
res_reset_cntr
new_lum_seg
clr
clk40
rd_trig_cntr : (15:0)
rd_deadt_cntr : (39:0)
inc_trig_cntr : (7:0)
res_trig_cntr : (7:0)
inc_deadt_cntr : (10:0)
res_deadt_cntr : (10:0)
inc_reset_cntr
res_reset_cntr
new_lum_seg
clr
clk
tcs_chip_lib
ptc_cntrs
I37
v_ptc_cntrs : (15:0)
event_nr : (31:0)
trig_nr : (31:0)
-- V1022 Aug09
v_cntrs(0) : (7:0)
event_nr(0) : (7:0)
trig_nr(0) : (7:0)
PTC_0

```
    SIGNAL rd_comm_40_be          : std_logic_vector(23 DOWNTO 0)
    SIGNAL rd_comm_b0_be          : std_logic_vector(7 DOWNTO 0)
    SIGNAL rd_deadt_cntr          : vec40_array(7 DOWNTO 0)
    SIGNAL rd_ptci_10_1e          : vec8_array(7 DOWNTO 0)
    SIGNAL rd_trig_cntr           : vec16_array(7 DOWNTO 0)
    SIGNAL rdbk_comm_reg          : std_logic
    SIGNAL rdbk_ptc_reg           : std_logic
    SIGNAL recover_time           : std_logic_vector(15 DOWNTO 0)
    SIGNAL res_bc_err             : std_logic
    SIGNAL res_deadt_cntr         : vec11_array(7 DOWNTO 0)
    SIGNAL res_orbit_cntr         : std_logic
    SIGNAL res_orbnr_by_ptc0      : std_logic
    SIGNAL res_reset_cntr         : std_logic
    SIGNAL res_throttle           : std_logic
    SIGNAL res_trig_cntr          : vec8_array(7 DOWNTO 0)
    SIGNAL reset_all              : std_logic
    SIGNAL rndm_period            : vec16_array(7 DOWNTO 0)
    SIGNAL rndm_prescale_fact     : vec16_array(7 DOWNTO 0)
    SIGNAL rop_status             : std_logic_vector(3 DOWNTO 0)
    SIGNAL settle_time            : std_logic_vector(15 DOWNTO 0)
    SIGNAL sig2emu                : vec3_array(7 DOWNTO 0)
    SIGNAL sig2emu_tp0            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp1            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp2            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp3            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp4            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp5            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp6            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sig2emu_tp7            : std_logic_vector(2 DOWNTO 0)
    SIGNAL sim_emu_ctrl           : std_logic_vector(15 DOWNTO 0)
    SIGNAL sim_emu_status         : vec16_array(1 DOWNTO 0)
    SIGNAL status2led             : vec43_array(2 DOWNTO 0)
    SIGNAL status2ptc             : vec8_array(7 DOWNTO 0)
    SIGNAL status2vme             : vec16_array(10 DOWNTO 0)
    SIGNAL switch_tp2pan          : std_logic_vector(15 DOWNTO 0)
    SIGNAL tcs2daq                : vec4_array(7 DOWNTO 0)
    SIGNAL tcs2fdl                : std_logic_vector(1 DOWNTO 0)
    SIGNAL tcs2fdl_u              : std_logic_vector(1 DOWNTO 0)
    SIGNAL tcs_rop_empty          : std_logic
    SIGNAL tcs_rop_full           : std_logic
    SIGNAL tcs_rop_warn50         : std_logic
    SIGNAL tcs_rop_warn75         : std_logic
    SIGNAL tech_trig_in           : std_logic_vector(7 DOWNTO 0)
    SIGNAL tech_trig_unused       : std_logic_vector(7 DOWNTO 0)
    SIGNAL test_sig0              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig1              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig2              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig3              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig4              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig5              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig6              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig7              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_sig8              : std_logic_vector(15 DOWNTO 0)
    SIGNAL test_signal            : vec16_array(8 DOWNTO 0)
    SIGNAL testmasks              : vec16_array(8 DOWNTO 0)
    SIGNAL thr_rule               : std_logic_vector(127 DOWNTO 0)
    SIGNAL time_slots             : vec16_array(7 DOWNTO 0)
    SIGNAL tp_eor                 : std_logic
    SIGNAL tp_header              : std_logic_vector(3 DOWNTO 0)
    SIGNAL tp_new_segm            : std_logic
    SIGNAL tp_sel_word0           : std_logic
    SIGNAL tp_thro_inh            : std_logic_vector(7 DOWNTO 0)
    SIGNAL trig_nr                : vec32_array(7 DOWNTO 0)
    SIGNAL trig_type_a            : vec16_array(7 DOWNTO 0)
    SIGNAL trig_type_b            : vec16_array(7 DOWNTO 0)
    SIGNAL v_bc_table0            : vec16_array(7 DOWNTO 0)
    SIGNAL v_bc_table1            : vec16_array(7 DOWNTO 0)
```


DCM & CLOCK
We could also take clock_dcm from psb_lib or clock_module from common_lib.
CLKFB not used, maybe later.
==> to unused
CLK_FBIN_TCS
CLK_FBIN_TCS
2P
unisim
IBUFG_LVDCI_33
I21
clkfb_unused
CLK_TO_TCS
CLK_TO_TCS
0P
unisim
IBUFG_LVDCI_33
I23
CLKIN
clk40
ground
ground
ground
ground
gsr
CLKFB
CLKIN
DSSEN
PSCLK
PSEN
PSINCDEC
RST
unisim
DCM
I8
CLK0
CLK180
CLK270
CLK2X
CLK2X180
CLK90
CLKDV
CLKFX
CLKFX180
LOCKED
PSDONE
STATUS : (7:0)
CLK0
CLK180
CLK2X
CLK2X180
unisim
BUFG
I9
clk40
unisim
BUFG
I24
nclk40
unisim
BUFG
I30
clk80
unisim
BUFG
I31
nclk80
IBUFG and IBUF are placed on uppermost hierarchy.
dcm_locked
Simulation ok.
DCM locks after 1.7ms
inv
I84
gsr
or
I45
clr
TCS: CLEAR all by VME chip
RESET_TCS_CHIP
RESET_TCS_CHIP
Buff
buff
I5
gsr
INACTIVE
INACTIVE
Buff
buff
I6
=INTERLOCK=INACTIVE
clk40
gts
CLK
GSR
GTS
unisim
STARTUP_VIRTEX2
I4
FDL, PSB, TIM
clr <= not clk_locked
CLK_LOCKED_TCS
CLK_LOCKED_TCS
Buff
buff
I51
dcm_locked
For Synthesis add --pragma synthesis_off/on around generics
rightMouse==> select Object Properties==>Generics
and activate 'add pragmas around generics'
CLK_FBOUT_TCS
CLK_FBOUT_TCS
Buff
buff
I50
clk40
GTS=1 ==> All IOB into highZ
GSR=1 ==> Reset/Set set all FF
GCLK0S
GCLK0S
Buff
buff
I49
clk40
eb7
7
-- gnd_16 <= X"0000";
-- gnd_4 <= "0000";
gnd_2 <= "00";
-- gnd_1 <= '0';
ground <= '0';
high <= '1';
high
gnd_2 : (1:0)
ground
high
TP on MEZZ board

VME registers



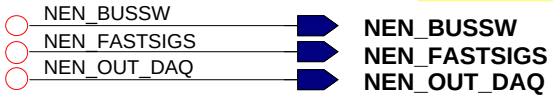
eb18 18

```
-- eb18 18
NEN_BUSSW <= disable_io(3);
-- automatic generation in tcs_rop:
-- NEN_EVM_LINK <= disable_io(2);
NEN_FASTSIGS <= disable_io(1);
NEN_OUT_DAQ <= disable_io(0);
```

RATE COUNTERS: 32 bits (12h/100kHz) --> 2 words
DEADTIME COUNTERS: 40 bits(7h/40MHz) -->48 --> 3 words+1free

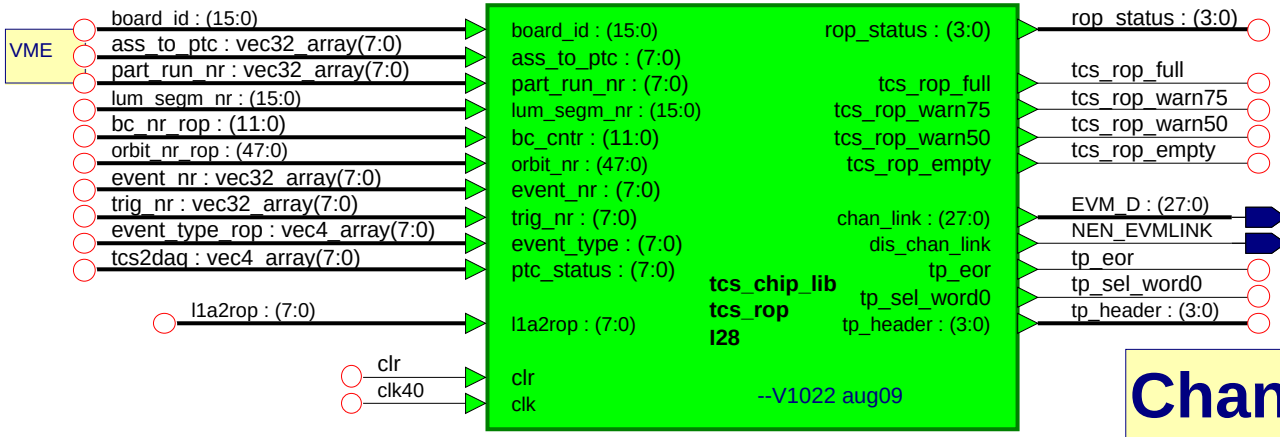
fehlt noch

w/r regs: load all into a RAM and read them back from it.



ROP

If L1A arrives then send a record.

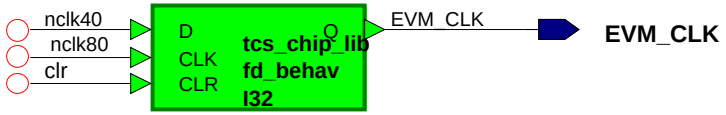


rop_status:
8=ready
2=out_of_sync
0=disconnected

EVM_D
NEN_EVMLINK

tp_eor ...end of record

Channel Link



EVM_CLK

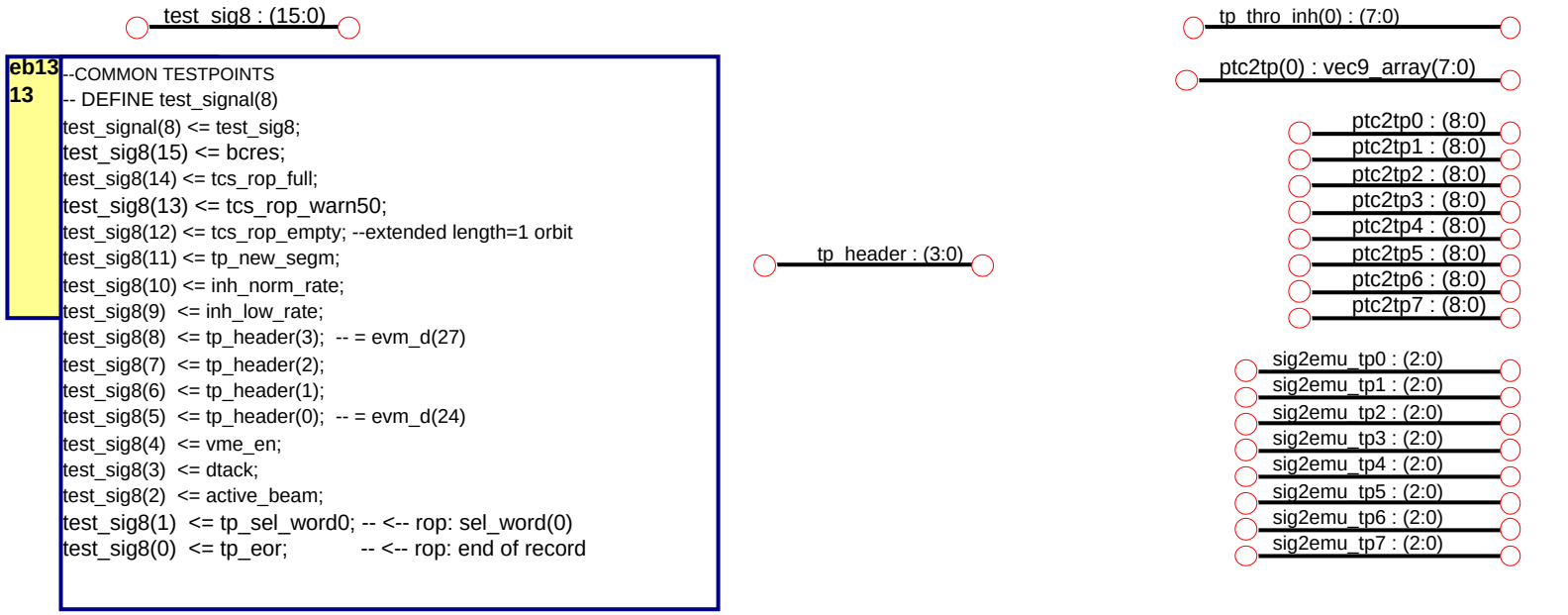
EVM_CLK = clk40 delayed by 6.2 ns to write safely into then Channel Link chip.

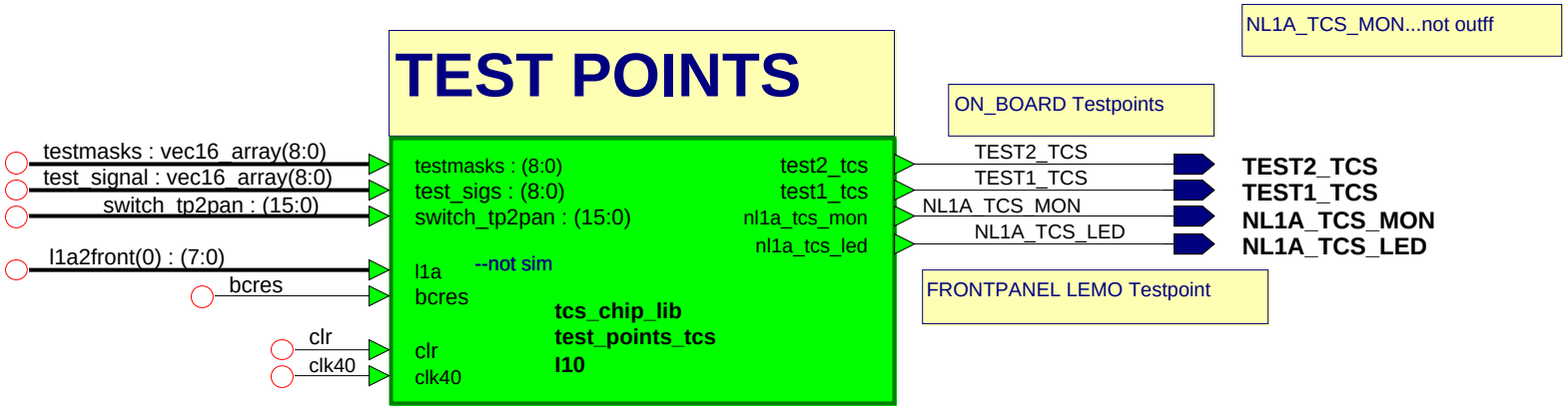
ROP runs without L1RESET from PTC0 and sends all events until FIFO is empty.
Inhibit L1As to return it to idle mode. StateMachine has been replaced by a Pipeline Logic.

```
SIGNAL v_cntrs              : vec16_array(7 DOWNTO 0)
SIGNAL vdii                 : std_logic_vector(15 DOWNTO 0)
SIGNAL vdin                 : std_logic_vector(15 DOWNTO 0)
SIGNAL vdoo                 : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout                : std_logic_vector(15 DOWNTO 0)
SIGNAL vme_addr             : std_logic_vector(19 DOWNTO 1)
SIGNAL vme_adresse_sim      : std_logic_vector(19 DOWNTO 0)
SIGNAL vme_en               : std_logic
SIGNAL vme_en1              : std_logic
SIGNAL vme_en2              : std_logic
SIGNAL vme_en3              : std_logic
SIGNAL vme_enn              : std_logic
SIGNAL vme_wr               : std_logic
SIGNAL wr_bctable           : std_logic
SIGNAL wr_comm_00_3e        : std_logic_vector(31 DOWNTO 0)
SIGNAL wr_comm_70_ae        : std_logic_vector(31 DOWNTO 0)
SIGNAL wr_comm_b6           : std_logic
SIGNAL wr_comm_cmd_puls     : std_logic
SIGNAL wr_comm_reg          : std_logic
SIGNAL wr_ptc_cmd_puls      : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_ptc_reg           : std_logic
SIGNAL wr_ptci_00_0e        : vec8_array(7 DOWNTO 0)
SIGNAL wr_ptci_c0_ce        : vec8_array(7 DOWNTO 0)
```

```
CLKDV_DIVIDE          = 2.0                    ( real       )
CLKFX_DIVIDE          = 1                      ( integer    )
CLKFX_MULTIPLY        = 4                      ( integer    )
CLKIN_DIVIDE_BY_2     = false                  ( boolean    )
CLKIN_PERIOD          = 10.0                   ( real       ) --non-simulatable
CLKOUT_PHASE_SHIFT    = "NONE"                 ( string     )
CLK_FEEDBACK          = "1X"                   ( string     )
DESKEW_ADJUST         = "SYSTEM_SYNCHRONOUS"   ( string     ) --non-simulatable
DFS_FREQUENCY_MODE    = "LOW"                  ( string     )
DLL_FREQUENCY_MODE    = "LOW"                  ( string     )
DSS_MODE              = "NONE"                 ( string     ) --non-simulatable
DUTY_CYCLE_CORRECTION = true                   ( boolean    )
FACTORY_JF            = X"C080"                ( bit_vector ) --non-simulatable
PHASE_SHIFT           = 0                      ( integer    )
SIM_MODE              = "SAFE"                 ( string     )
STARTUP_WAIT          = false                  ( boolean    ) --non-simulatable
```

COMMON TEST POINTS





PTCi TEST POINTS

test_sig0 : (15:0)

eb33

```
-- PTC 0  testpoints
-- DEFINE test_signal(0)
test_signal(0) <= test_sig0;
sig2emu_tp0 <= sig2emu(0);
ptc2tp0 <= ptc2tp(0);
test_sig0(15) <= l1a2front(0);
test_sig0(14) <= en_time_slot(0);
test_sig0(13) <= ptc2tp0(8); -- bgo_strobe
test_sig0(12) <= sig2emu_tp0(2); --bcr
test_sig0(11) <= sig2emu_tp0(1); --resync
test_sig0(10) <= sig2emu_tp0(0); --l1a
test_sig0(9)  <= tp_thro_inh(0);
test_sig0(8)  <= finor(0);      -- from FDL
test_sig0(7)  <= ptc2tp0(7); -- low_rate
test_sig0(6)  <= ptc2tp0(6); -- norm_rate
test_sig0(5)  <= ptc2tp0(5); -- random_trig
test_sig0(4)  <= ptc2tp0(4); -- test_trig
test_sig0(3)  <= ptc2tp0(3); -- cal_trig
test_sig0(2)  <= ptc2tp0(2); -- inh_l1a_test
test_sig0(1)  <= ptc2tp0(1); -- inh_l1a_cal
test_sig0(0)  <= ptc2tp0(0); -- inh_l1a_priv
```

test_sig1 : (15:0)

eb44

```
-- PTC1  testpoints
-- DEFINE test_signal(1)
test_signal(1) <= test_sig1;
sig2emu_tp1 <= sig2emu(1);
ptc2tp1 <= ptc2tp(1);
test_sig1(15) <= l1a2front(1);
test_sig1(14) <= en_time_slot(1);
test_sig1(13) <= ptc2tp1(8);
test_sig1(12) <= sig2emu_tp1(2);
test_sig1(11) <= sig2emu_tp1(1);
test_sig1(10) <= sig2emu_tp1(0);
test_sig1(9)  <= tp_thro_inh(1);
test_sig1(8)  <= finor(1);
test_sig1(7)  <= ptc2tp1(7);
test_sig1(6)  <= ptc2tp1(6);
test_sig1(5)  <= ptc2tp1(5);
test_sig1(4)  <= ptc2tp1(4);
test_sig1(3)  <= ptc2tp1(3);
test_sig1(2)  <= ptc2tp1(2);
test_sig1(1)  <= ptc2tp1(1);
test_sig1(0)  <= ptc2tp1(0);
```

test_sig2 : (15:0)

eb88

```
-- PTC 2  testpoints
-- DEFINE test_signal(2)
test_signal(2) <= test_sig2;
sig2emu_tp2 <= sig2emu(2);
ptc2tp2 <= ptc2tp(2);
test_sig2(15) <= l1a2front(2);
test_sig2(14) <= en_time_slot(2);
test_sig2(13) <= ptc2tp2(8);
test_sig2(12) <= sig2emu_tp2(2);
test_sig2(11) <= sig2emu_tp2(1);
test_sig2(10) <= sig2emu_tp2(0);
test_sig2(9)  <= tp_thro_inh(2);
test_sig2(8)  <= finor(2);
test_sig2(7)  <= ptc2tp2(7);
test_sig2(6)  <= ptc2tp2(6);
test_sig2(5)  <= ptc2tp2(5);
test_sig2(4)  <= ptc2tp2(4);
test_sig2(3)  <= ptc2tp2(3);
test_sig2(2)  <= ptc2tp2(2);
test_sig2(1)  <= ptc2tp2(1);
test_sig2(0)  <= ptc2tp2(0);
```

test_sig3 : (15:0)

eb99

```
-- PTC 3  testpoints
-- DEFINE test_signal(3)
test_signal(3) <= test_sig3;
sig2emu_tp3 <= sig2emu(3);
ptc2tp3 <= ptc2tp(3);
test_sig3(15) <= l1a2front(3);
test_sig3(14) <= en_time_slot(3);
test_sig3(13) <= ptc2tp3(8);
test_sig3(12) <= sig2emu_tp3(2);
test_sig3(11) <= sig2emu_tp3(1);
test_sig3(10) <= sig2emu_tp3(0);
test_sig3(9)  <= tp_thro_inh(3);
test_sig3(8)  <= finor(3);
test_sig3(7)  <= ptc2tp3(7);
test_sig3(6)  <= ptc2tp3(6);
test_sig3(5)  <= ptc2tp3(5);
test_sig3(4)  <= ptc2tp3(4);
test_sig3(3)  <= ptc2tp3(3);
test_sig3(2)  <= ptc2tp3(2);
test_sig3(1)  <= ptc2tp3(1);
test_sig3(0)  <= ptc2tp3(0);
```

test_sig4 : (15:0)

eb66

```
-- PTC 4  testpoints
-- DEFINE test_signal(4)
test_signal(4) <= test_sig4;
sig2emu_tp4 <= sig2emu(4);
ptc2tp4 <= ptc2tp(4);
test_sig4(15) <= l1a2front(4);
test_sig4(14) <= en_time_slot(4);
test_sig4(13) <= ptc2tp4(8);
test_sig4(12) <= sig2emu_tp4(2);
test_sig4(11) <= sig2emu_tp4(1);
test_sig4(10) <= sig2emu_tp4(0);
test_sig4(9)  <= tp_thro_inh(4);
test_sig4(8)  <= finor(4);
test_sig4(7)  <= ptc2tp4(7);
test_sig4(6)  <= ptc2tp4(6);
test_sig4(5)  <= ptc2tp4(5);
test_sig4(4)  <= ptc2tp4(4);
test_sig4(3)  <= ptc2tp4(3);
test_sig4(2)  <= ptc2tp4(2);
test_sig4(1)  <= ptc2tp4(1);
test_sig4(0)  <= ptc2tp4(0);
```

test_sig5 : (15:0)

eb1010

```
-- PTC 5  testpoints
-- DEFINE test_signal(5)
test_signal(5) <= test_sig5;
sig2emu_tp5 <= sig2emu(5);
ptc2tp5 <= ptc2tp(5);
test_sig5(15) <= l1a2front(5);
test_sig5(14) <= en_time_slot(5);
test_sig5(13) <= ptc2tp5(8);
test_sig5(12) <= sig2emu_tp5(2);
test_sig5(11) <= sig2emu_tp5(1);
test_sig5(10) <= sig2emu_tp5(0);
test_sig5(9)  <= tp_thro_inh(5);
test_sig5(8)  <= finor(5);
test_sig5(7)  <= ptc2tp5(7);
test_sig5(6)  <= ptc2tp5(6);
test_sig5(5)  <= ptc2tp5(5);
test_sig5(4)  <= ptc2tp5(4);
test_sig5(3)  <= ptc2tp5(3);
test_sig5(2)  <= ptc2tp5(2);
test_sig5(1)  <= ptc2tp5(1);
test_sig5(0)  <= ptc2tp5(0);
```

test_sig6 : (15:0)

eb1111

```
-- PTC 6  testpoints
-- DEFINE test_signal(6)
test_signal(6) <= test_sig6;
sig2emu_tp6 <= sig2emu(6);
ptc2tp6 <= ptc2tp(6);
test_sig6(15) <= l1a2front(6);
test_sig6(14) <= en_time_slot(6);
test_sig6(13) <= ptc2tp6(8);
test_sig6(12) <= sig2emu_tp6(2);
test_sig6(11) <= sig2emu_tp6(1);
test_sig6(10) <= sig2emu_tp6(0);
test_sig6(9)  <= tp_thro_inh(6);
test_sig6(8)  <= finor(6);
test_sig6(7)  <= ptc2tp6(7);
test_sig6(6)  <= ptc2tp6(6);
test_sig6(5)  <= ptc2tp6(5);
test_sig6(4)  <= ptc2tp6(4);
test_sig6(3)  <= ptc2tp6(3);
test_sig6(2)  <= ptc2tp6(2);
test_sig6(1)  <= ptc2tp6(1);
test_sig6(0)  <= ptc2tp6(0);
```

test_sig7 : (15:0)

eb1212

```
-- PTC 7  testpoints
-- DEFINE test_signal(7)
test_signal(7) <= test_sig7;
sig2emu_tp7 <= sig2emu(7);
ptc2tp7 <= ptc2tp(7);
test_sig7(15) <= l1a2front(7);
test_sig7(14) <= en_time_slot(7);
test_sig7(13) <= ptc2tp7(8);
test_sig7(12) <= sig2emu_tp7(2); --bcr
test_sig7(11) <= sig2emu_tp7(1); --resync
test_sig7(10) <= sig2emu_tp7(0); --l1a
test_sig7(9)  <= tp_thro_inh(7);
test_sig7(8)  <= finor(7);     -- from FDL
test_sig7(7)  <= ptc2tp7(7); -- low_rate
test_sig7(6)  <= ptc2tp7(6); -- norm_rate
test_sig7(5)  <= ptc2tp7(5); -- random_trig
test_sig7(4)  <= ptc2tp7(4); -- test_trig
test_sig7(3)  <= ptc2tp7(3); -- cal_trig
test_sig7(2)  <= ptc2tp7(2); -- inh_l1a_test
test_sig7(1)  <= ptc2tp7(1); -- inh_l1a_cal
test_sig7(0)  <= ptc2tp7(0); -- inh_l1a_priv
```

Declarations

Ports:

```
active_beam         : std_logic
bc_cntr             : std_logic_vector(11 downto 0)
bcres               : std_logic
bgo_period_l        : std_logic_vector(15 DOWNTO 0)
bgo_period_s        : std_logic_vector(15 DOWNTO 0)
clk40               : std_logic
clr                 : std_logic
cmd_pulse           : std_logic_vector(15 DOWNTO 0)
cmd_reg             : std_logic_vector(15 DOWNTO 0)
emu_delay           : std_logic_vector( 15 DOWNTO 0 )
emu_trigger         : std_logic
en_bctable          : std_logic_vector( 1 DOWNTO 0 )
en_time_slot        : std_logic
fin_or              : std_logic
inh_low_rate        : std_logic
inh_norm_rate       : std_logic
new_lum_seg         : std_logic
orbit_nr            : std_logic_vector(47 DOWNTO 0)
ptc_clears_orbitnr  : std_logic
recover_time        : std_logic_vector( 15 DOWNTO 0 )
rndm_period         : std_logic_vector(15 DOWNTO 0)
rndm_prescale_fact  : std_logic_vector(15 DOWNTO 0)
settle_time         : std_logic_vector( 15 DOWNTO 0 )
status2ptc          : std_logic_vector(7 DOWNTO 0)
tcs_rop_full        : std_logic
tcs_rop_warn        : std_logic
trig_type_a         : std_logic_vector(15 DOWNTO 0)
trig_type_b         : std_logic_vector(15 DOWNTO 0)
v_addr              : std_logic_vector(19 DOWNTO 1)
v_din               : std_logic_vector( 15 DOWNTO 0 )
wr_bctable          : std_logic
event_type_rop      : std_logic_vector(3 DOWNTO 0)
inc_deadt_cntr      : std_logic_vector(10 DOWNTO 0)
inc_reset_cntr      : std_logic
inc_trig_cntr       : std_logic_vector(7 DOWNTO 0 )
inh_fdl_cntrs       : std_logic
l1a2front           : std_logic
l1a2rop             : std_logic
l1a2throttle        : std_logic
l1a_bgo_to_ttc      : std_logic_vector(5 DOWNTO 0)
lum_to_ttc          : std_logic_vector(3 DOWNTO 0)
p_status            : std_logic_vector(15 DOWNTO 0)
ptc_fsm_states      : std_logic_vector(15 DOWNTO 0)
ptcstat2led         : std_logic_vector(2 DOWNTO 0)
res_deadt_cntr      : std_logic_vector(10 DOWNTO 0)
res_orbnr_by_ptc    : std_logic
res_reset_cntr      : std_logic
res_trig_cntr       : std_logic_vector(7 DOWNTO 0 )
sig2emu             : std_logic_vector( 2 DOWNTO 0 )
tcs2daq             : std_logic_vector(3 DOWNTO 0)
test_sig            : std_logic_vector(8 DOWNTO 0)
tp_thro_inh         : std_logic
v_bc_table0         : std_logic_vector( 15 DOWNTO 0 )
v_bc_table1         : std_logic_vector( 15 DOWNTO 0 )
```

Diagram Signals:

```
SIGNAL bc_tab_p           : std_logic_vector(31 DOWNTO 0)
SIGNAL bgo                : std_logic_vector( 4 DOWNTO 0 )
SIGNAL cal_trig           : std_logic
SIGNAL deadtime2lum       : std_logic
SIGNAL do                 : std_logic_vector( 5 DOWNTO 0 )
SIGNAL do_bcres           : std_logic
SIGNAL do_calibr          : std_logic
SIGNAL do_priv_bgo        : std_logic
```

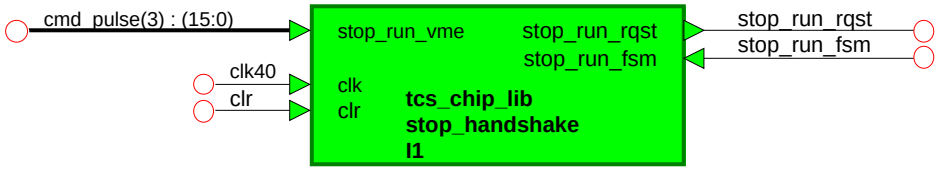
Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;

LIBRARY tcs_types;
USE tcs_types.tcs.all;
```

cmd_reg
15: dis_disconnected
14: dis_bad_code
13: IGNORE_GTFE_STATUS
12: dis_finor
11: IGNORE_GT_STATUS
10: ALLOW_TEST_TRIGGER
9: use_valid_bc
8: DO NOT SEND EVENT RECORDS
(old name: run_without_daq)
7: freeze_if_bad_bcnr
6: freeze_if_error
5: freeze_if_out_of_sync
4: freeze_if_warning
3: freeze_if_bad_code
2: EN_ERR_TRIG
1: IGNORE_TCS_ROP_STATUS
0: en_rndm_trig

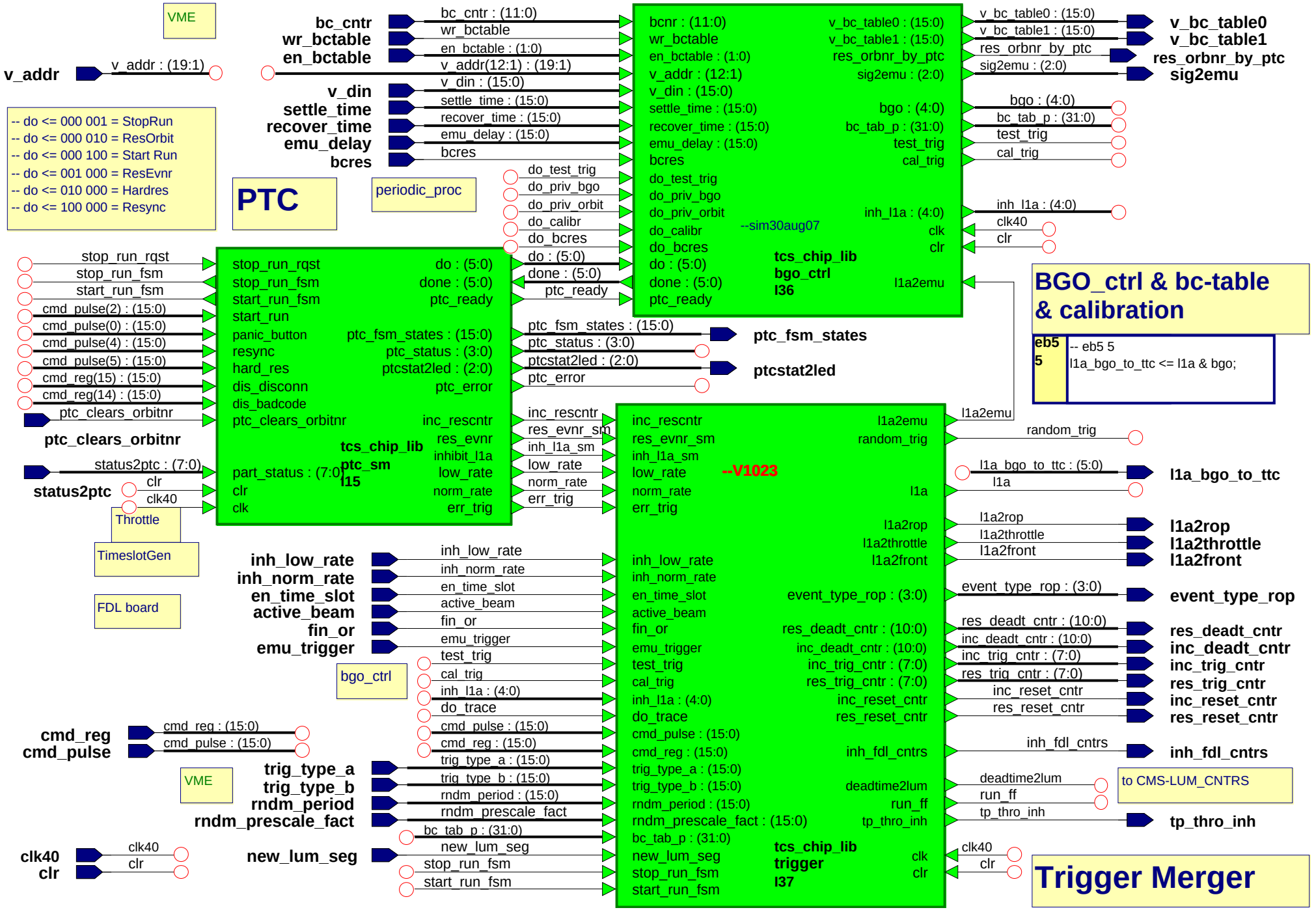
cmd_pulse
15:---
14: ---
13: ---
12:---
11: do_test_trig
10: do_priv_orbit
9: defrost_ptc
8: start_rndm_trig
7: do_traced_event
6: do_calibr_cycle
5: hard_reset
4: resynchronize
3: stop_run
2: start_run
1: start_ptc
0: reset_ptc...NOT USED



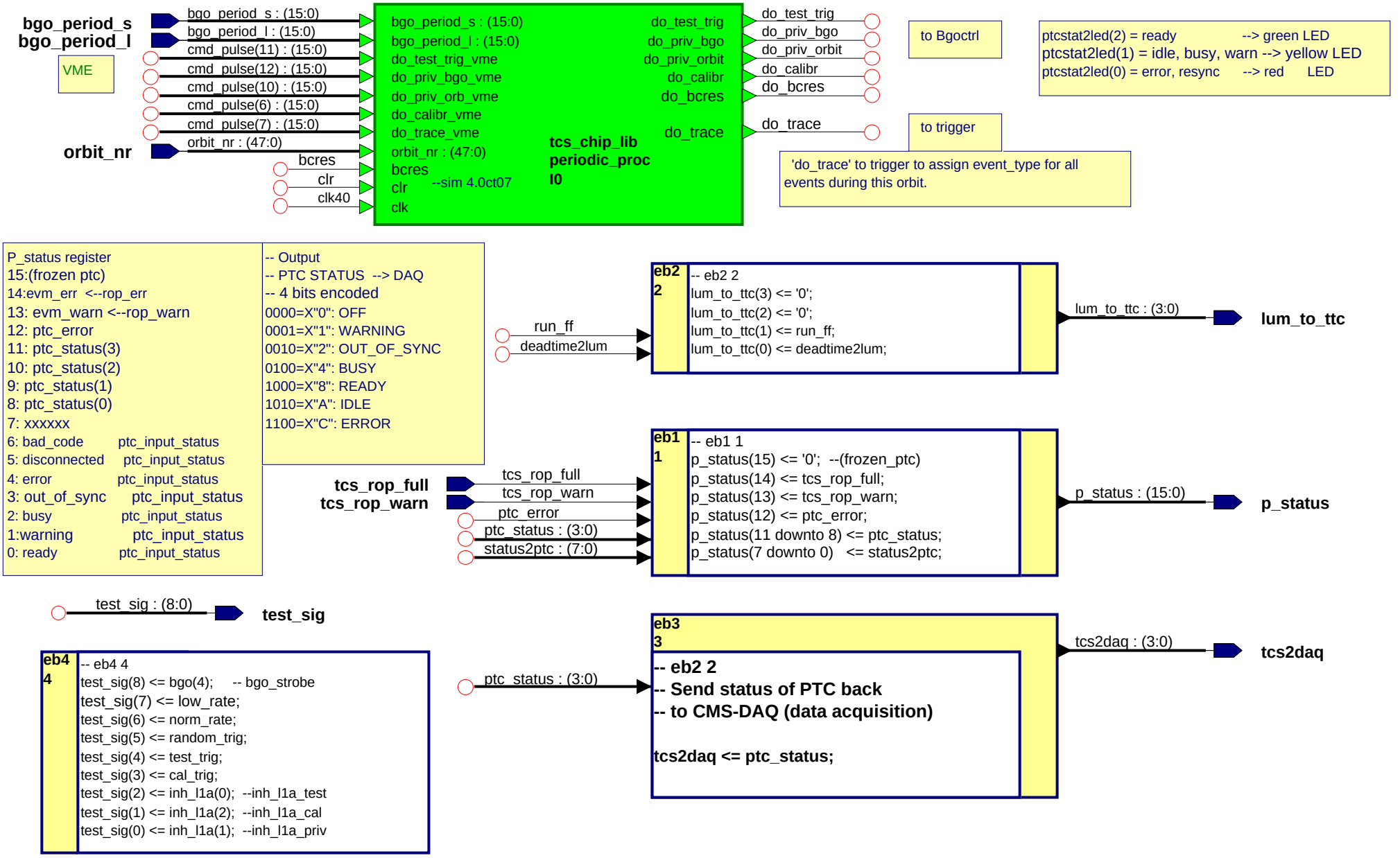
-- Input 'status2ptc'
-- PARTITION STATES
-- part_status :=decoded bits
bit 0: READY
bit 1: WARNING
bit 2: BUSY
bit 3: OUT_OF_SYNC
bit 4: ERROR
bit 5: DISCONNECTED
bit 6: BAD CODE
bit 7: ---free

status2ptc:
20=disconn
40=bad_code
10=error
8 =out of sync
4=busy
2=warning
1=ready

<company name>		Project:	tcsv2
		V0017: ptc_sm, trigger, bgo_ctrl ...modified	
Title:	<enter diagram title here>		
Path:	tcs_chip_lib/ptc/struct		
Edited:	by taurok on 30 Okt 2009		


VME
v_addr
v_addr : (19:1)
-- do <= 000 001 = StopRun
-- do <= 000 010 = ResOrbit
-- do <= 000 100 = Start Run
-- do <= 001 000 = ResEvnr
-- do <= 010 000 = Hardres
-- do <= 100 000 = Resync
bc_cntr
wr_bctable
en_bctable
v_din
settle_time
recover_time
emu_delay
bcres
PTC
periodic_proc
stop_run_rqst
stop_run_fsm
start_run_fsm
cmd_pulse(2) : (15:0)
cmd_pulse(0) : (15:0)
cmd_pulse(4) : (15:0)
cmd_pulse(5) : (15:0)
cmd_reg(15) : (15:0)
cmd_reg(14) : (15:0)
ptc_clears_orbitnr
status2ptc
clr
clk40
Throttle
TimeslotGen
FDL board
tcs_chip_lib
ptc_sm
l15
--sim30aug07
tcs_chip_lib
bgo_ctrl
l36
ptc_fsm_states
ptcstat2led
BGO_ctrl & bc-table & calibration
eb5 5
-- eb5 5
l1a_bgo_to_ttc <= l1a & bgo;
--V1023
inh_low_rate
inh_norm_rate
en_time_slot
active_beam
fin_or
emu_trigger
bgo_ctrl
cmd_reg
cmd_pulse
VME
trig_type_a
trig_type_b
rndm_period
rndm_prescale_fact
clk40
clr
new_lum_seg
tcs_chip_lib
trigger
l37
to CMS-LUM_CNTRS
Trigger Merger

```
SIGNAL do_priv_bgo        : std_logic
SIGNAL do_priv_orbit      : std_logic
SIGNAL do_test_trig       : std_logic
SIGNAL do_trace           : std_logic
SIGNAL done               : std_logic_vector( 5 DOWNTO 0 )
SIGNAL err_trig           : std_logic
SIGNAL inc_rescntr        : std_logic
SIGNAL inh_l1a            : std_logic_vector(4 DOWNTO 0)
SIGNAL inh_l1a_sm         : std_logic
SIGNAL l1a                : std_logic
SIGNAL l1a2emu            : std_logic
SIGNAL low_rate           : std_logic
SIGNAL norm_rate          : std_logic
SIGNAL ptc_error          : std_logic
SIGNAL ptc_ready          : std_logic
SIGNAL ptc_status         : std_logic_vector( 3 DOWNTO 0 )
SIGNAL random_trig        : std_logic
SIGNAL res_evnr_sm        : std_logic
SIGNAL run_ff             : std_logic
SIGNAL start_run_fsm      : std_logic
SIGNAL stop_run_fsm       : std_logic
SIGNAL stop_run_rqst      : std_logic
SIGNAL test_trig          : std_logic
```


bgo_period_s
bgo_period_l
VME
orbit_nr
bgo_period_s : (15:0)
bgo_period_l : (15:0)
cmd_pulse(11) : (15:0)
cmd_pulse(12) : (15:0)
cmd_pulse(10) : (15:0)
cmd_pulse(6) : (15:0)
cmd_pulse(7) : (15:0)
orbit_nr : (47:0)
bcres
clr
clk40
bgo_period_s : (15:0)
bgo_period_l : (15:0)
do_test_trig_vme
do_priv_bgo_vme
do_priv_orb_vme
do_calibr_vme
do_trace_vme
orbit_nr : (47:0)
bcres
clr
clk
--sim 4.0ct07
tcs_chip_lib
periodic_proc
I0
do_test_trig
do_priv_bgo
do_priv_orbit
do_calibr
do_bcres
do_trace
do_test_trig
do_priv_bgo
do_priv_orbit
do_calibr
do_bcres
do_trace
to Bgoctrl
to trigger
ptcstat2led(2) = ready --> green LED
ptcstat2led(1) = idle, busy, warn --> yellow LED
ptcstat2led(0) = error, resync --> red LED
'do_trace' to trigger to assign event_type for all events during this orbit.
P_status register
15:(frozen ptc)
14:evm_err <--rop_err
13: evm_warn <--rop_warn
12: ptc_error
11: ptc_status(3)
10: ptc_status(2)
9: ptc_status(1)
8: ptc_status(0)
7: xxxxxx
6: bad_code ptc_input_status
5: disconnected ptc_input_status
4: error ptc_input_status
3: out_of_sync ptc_input_status
2: busy ptc_input_status
1:warning ptc_input_status
0: ready ptc_input_status
-- Output
-- PTC STATUS --> DAQ
-- 4 bits encoded
0000=X"0": OFF
0001=X"1": WARNING
0010=X"2": OUT_OF_SYNC
0100=X"4": BUSY
1000=X"8": READY
1010=X"A": IDLE
1100=X"C": ERROR
run_ff
deadtime2lum
eb2
2
-- eb2 2
lum_to_ttc(3) <= '0';
lum_to_ttc(2) <= '0';
lum_to_ttc(1) <= run_ff;
lum_to_ttc(0) <= deadtime2lum;
lum_to_ttc : (3:0)
lum_to_ttc
tcs_rop_full
tcs_rop_warn
tcs_rop_full
tcs_rop_warn
ptc_error
ptc_status : (3:0)
status2ptc : (7:0)
eb1
1
-- eb1 1
p_status(15) <= '0'; --(frozen_ptc)
p_status(14) <= tcs_rop_full;
p_status(13) <= tcs_rop_warn;
p_status(12) <= ptc_error;
p_status(11 downto 8) <= ptc_status;
p_status(7 downto 0) <= status2ptc;
p_status : (15:0)
p_status
test_sig : (8:0)
test_sig
eb4
4
-- eb4 4
test_sig(8) <= bgo(4); -- bgo_strobe
test_sig(7) <= low_rate;
test_sig(6) <= norm_rate;
test_sig(5) <= random_trig;
test_sig(4) <= test_trig;
test_sig(3) <= cal_trig;
test_sig(2) <= inh_l1a(0); --inh_l1a_test
test_sig(1) <= inh_l1a(2); --inh_l1a_cal
test_sig(0) <= inh_l1a(1); --inh_l1a_priv
ptc_status : (3:0)
eb3
3
-- eb2 2
-- Send status of PTC back
-- to CMS-DAQ (data acquisition)
tcs2daq <= ptc_status;
tcs2daq : (3:0)
tcs2daq

Global Actions **Concurrent Statements**
Pre Actions:
Post Actions:

Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
```

Architecture Declarations

Signals Status

SIGNAL	MODE	DEFAULT	RESET	SCHEME
do	OUT	(OTHERS => '0')	(OTHERS => '0')	CLKD
err_trig	OUT	'0'	'0'	CLKD
inc_rescntr	OUT	'0'	'0'	CLKD
inhibit_l1a	OUT	'1'	'1'	CLKD
low_rate	OUT	'0'	'0'	CLKD
norm_rate	OUT	'0'	'0'	CLKD
ptc_error	OUT	'0'	'0'	CLKD
ptc_fsm_states	OUT	(OTHERS => '0')	(OTHERS => '0')	CLKD
ptc_ready	OUT	'0'	'0'	CLKD
ptc_status	OUT	X"4"	X"A"	CLKD
ptcstat2led	OUT	B"010"	B"010"	CLKD
res_evnr	OUT	'0'	'0'	CLKD
start_run_fsm	OUT	'0'	'0'	CLKD
stop_run_fsm	OUT	'0'	'0'	CLKD

State Register Statements

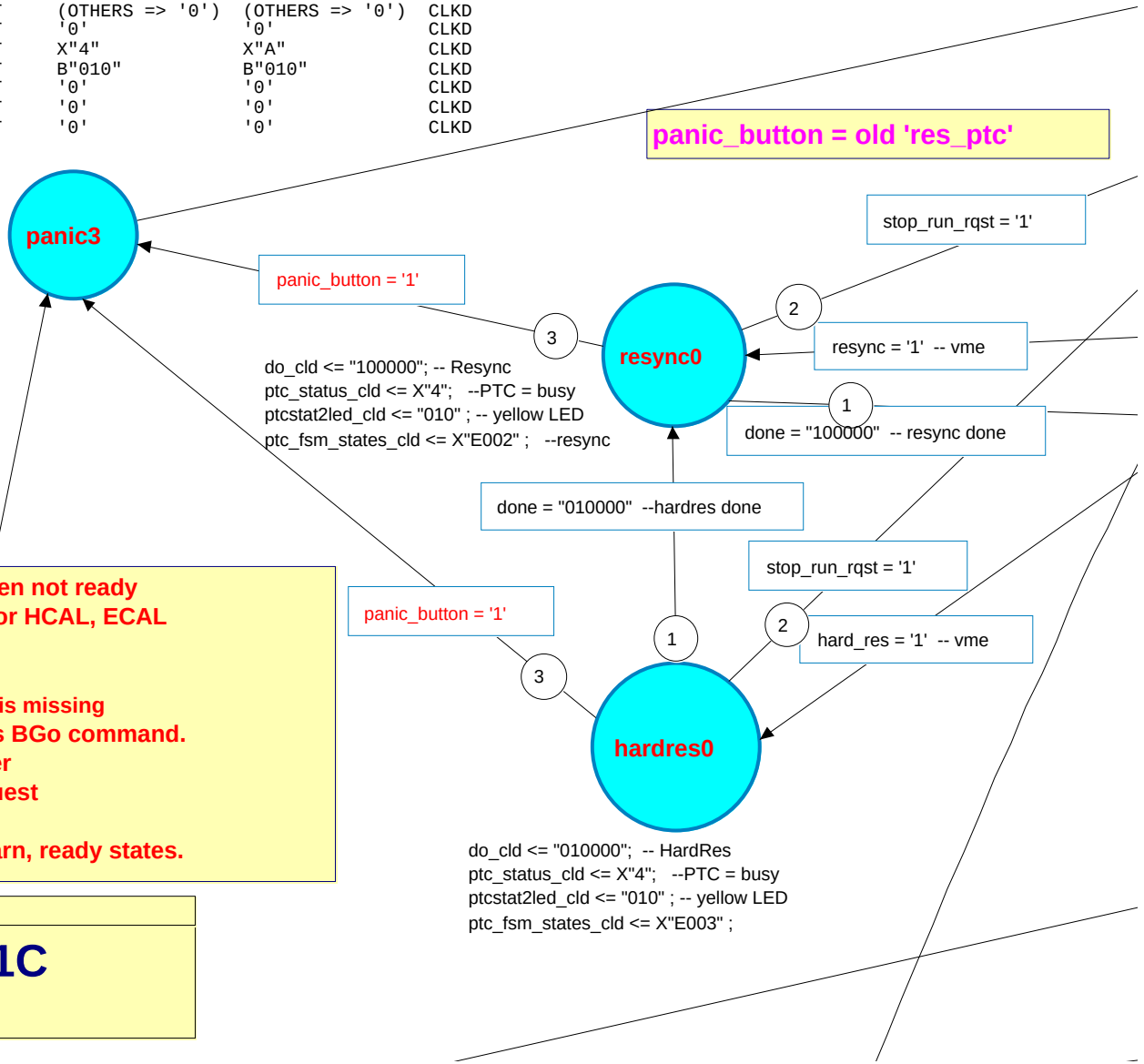
Process Declarations
Clocked Process:
Output Process:

Default values:
inhibit_l1a = '1'
ptc_status =X"4"=busy
ptcstat2led = "010" --yellow
low_rate = '0'
norm_rate = '0'

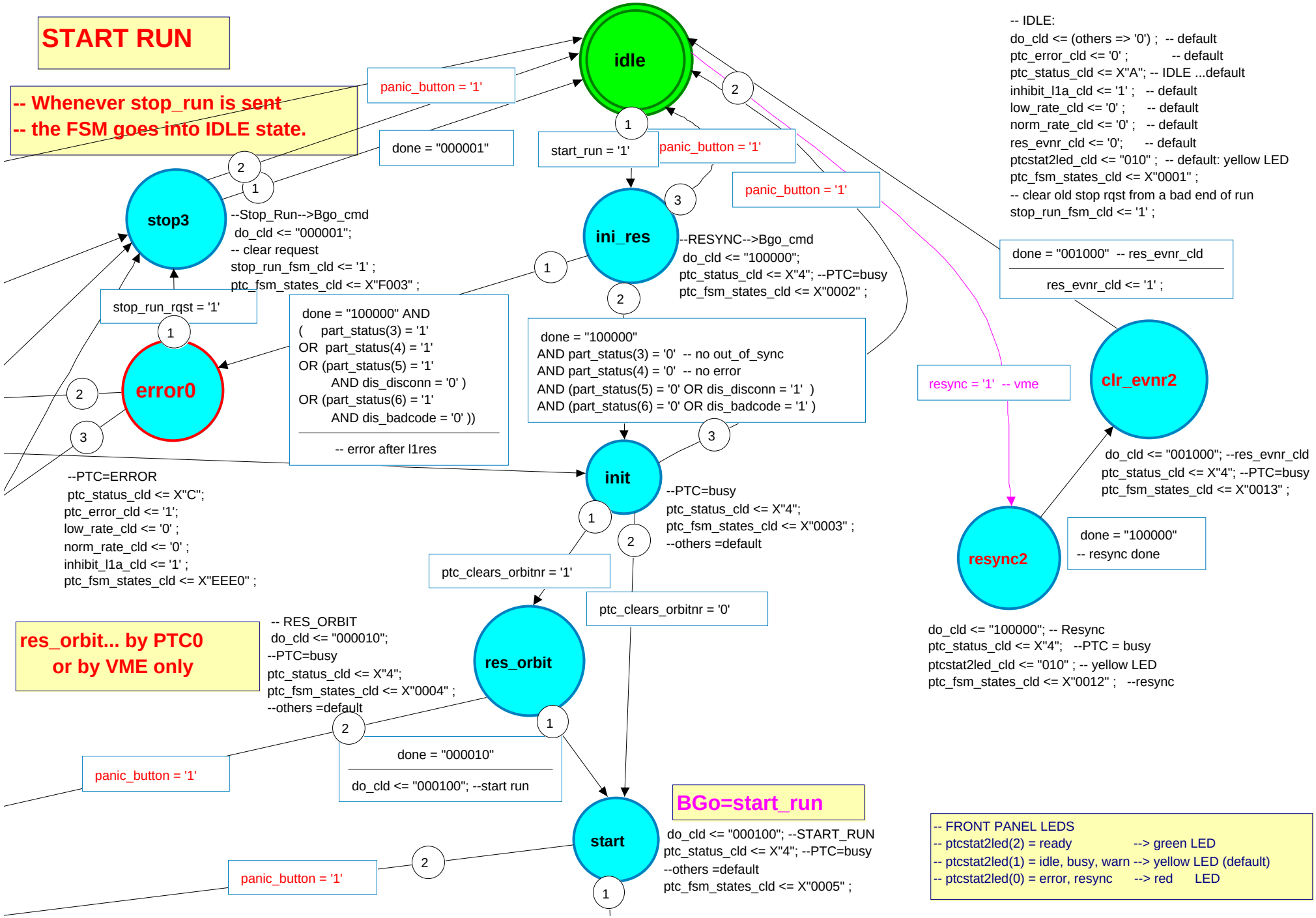
-- BAD CODE is ignored by FSM.

-- do() = long signal...reset by done()
-- do() as 1Tpulse: delete do command in states.

-- V001C: ptc_ready for bgo_ctrl added to suppress calcyc when not ready
-- V0017: resync2 --> res_evnr2 when in IDLE mode; required for HCAL, ECAL
-- V0016: resync0 --> init; send err_trig only during run
-- V0015: Start independently from input status.
-- PANIC BUTTON returns ptc_sm to IDLE status if 'done' bit is missing
-- because the BC-table does not contain the bit for this BGo command.
-- ptc_clears_orbitnr = '1' ..optional reset of orbit counter
-- IDLE:stop_run_fsm_cld <= '1' ; ' =ignore old stop request
-- 'hard_res' is possible when in out_of_sync status
-- V0011: resync_vme, hardres_vme possible when in busy, warn, ready states.



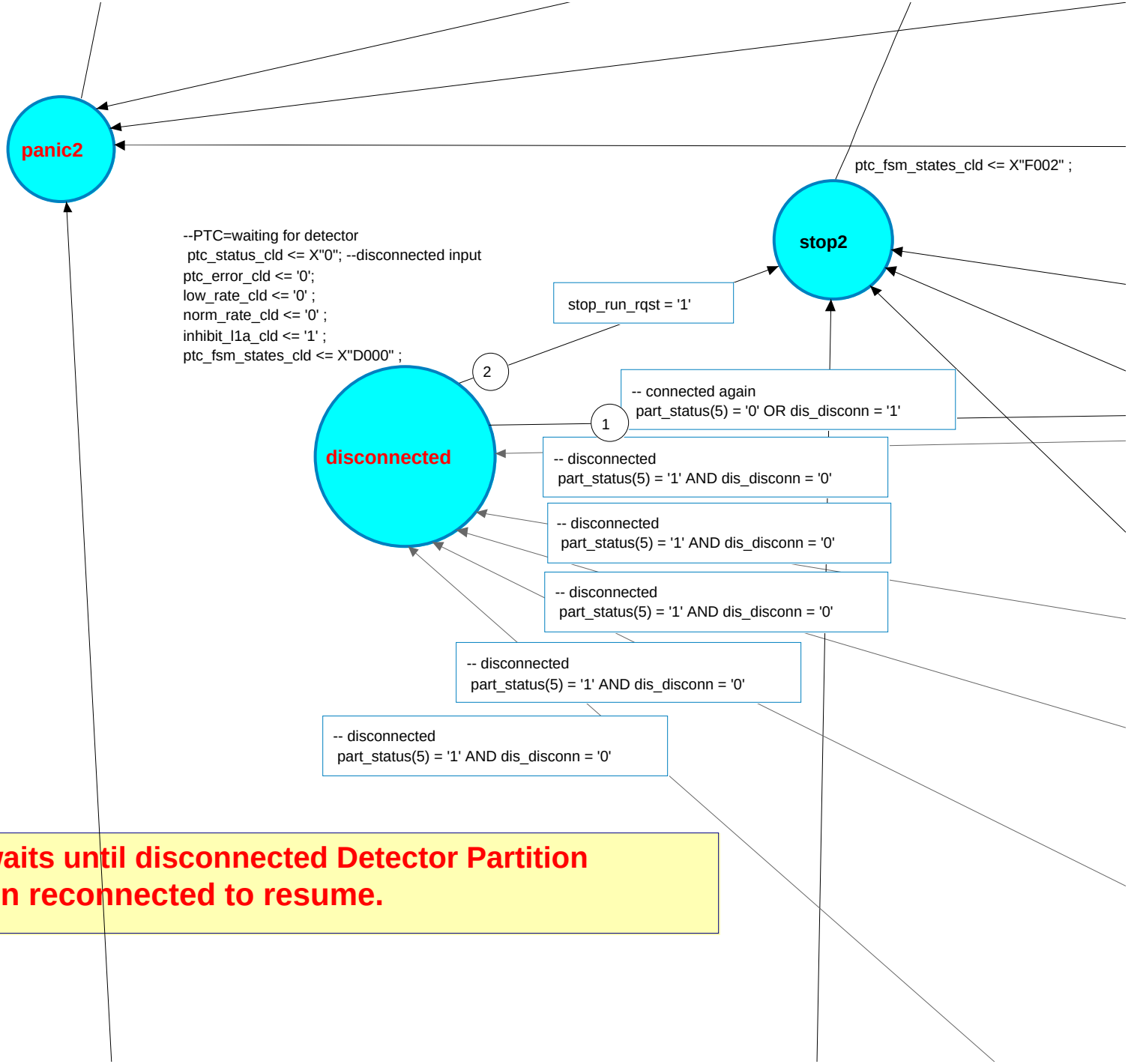
Vienna		Project:	tcsv2
Title:	PTC State Machine	**V001C**	
Path:	tcs_chip_lib/ptc_sm/fsm		
Edited:	by taurok on 31 Jul 2009		


START RUN
-- Whenever stop_run is sent
-- the FSM goes into IDLE state.
idle
panic_button = '1'
done = "000001"
start_run = '1'
panic_button = '1'
panic_button = '1'
stop3
--Stop_Run-->Bgo_cmd
do_cld <= "000001";
-- clear request
stop_run_fsm_cld <= '1' ;
ptc_fsm_states_cld <= X"F003" ;
stop_run_rqst = '1'
ini_res
--RESYNC-->Bgo_cmd
do_cld <= "100000";
ptc_status_cld <= X"4"; --PTC=busy
ptc_fsm_states_cld <= X"0002" ;
done = "100000" AND
(part_status(3) = '1'
OR part_status(4) = '1'
OR (part_status(5) = '1'
AND dis_disconn = '0')
OR (part_status(6) = '1'
AND dis_badcode = '0'))
-- error after l1res
error0
done = "100000"
AND part_status(3) = '0' -- no out_of_sync
AND part_status(4) = '0' -- no error
AND (part_status(5) = '0' OR dis_disconn = '1')
AND (part_status(6) = '0' OR dis_badcode = '1')
--PTC=ERROR
ptc_status_cld <= X"C";
ptc_error_cld <= '1';
low_rate_cld <= '0' ;
norm_rate_cld <= '0' ;
inhibit_l1a_cld <= '1' ;
ptc_fsm_states_cld <= X"EEE0" ;
init
--PTC=busy
ptc_status_cld <= X"4";
ptc_fsm_states_cld <= X"0003" ;
--others =default
ptc_clears_orbitnr = '1'
ptc_clears_orbitnr = '0'
res_orbit... by PTC0
or by VME only
-- RES_ORBIT
do_cld <= "000010";
--PTC=busy
ptc_status_cld <= X"4";
ptc_fsm_states_cld <= X"0004" ;
--others =default
res_orbit
done = "000010"
do_cld <= "000100"; --start run
panic_button = '1'
start
BGo=start_run
do_cld <= "000100"; --START_RUN
ptc_status_cld <= X"4"; --PTC=busy
--others =default
ptc_fsm_states_cld <= X"0005" ;
panic_button = '1'
-- IDLE:
do_cld <= (others => '0') ; -- default
ptc_error_cld <= '0' ; -- default
ptc_status_cld <= X"A"; -- IDLE ...default
inhibit_l1a_cld <= '1' ; -- default
low_rate_cld <= '0' ; -- default
norm_rate_cld <= '0' ; -- default
res_evnr_cld <= '0'; -- default
ptcstat2led_cld <= "010" ; -- default: yellow LED
ptc_fsm_states_cld <= X"0001" ;
-- clear old stop rqst from a bad end of run
stop_run_fsm_cld <= '1' ;
done = "001000" -- res_evnr_cld
res_evnr_cld <= '1' ;
resync = '1' -- vme
clr_evnr2
do_cld <= "001000"; --res_evnr_cld
ptc_status_cld <= X"4"; --PTC=busy
ptc_fsm_states_cld <= X"0013" ;
resync2
done = "100000"
-- resync done
do_cld <= "100000"; -- Resync
ptc_status_cld <= X"4"; --PTC = busy
ptcstat2led_cld <= "010" ; -- yellow LED
ptc_fsm_states_cld <= X"0012" ; --resync
-- FRONT PANEL LEDS
-- ptcstat2led(2) = ready --> green LED
-- ptcstat2led(1) = idle, busy, warn --> yellow LED (default)
-- ptcstat2led(0) = error, resync --> red LED

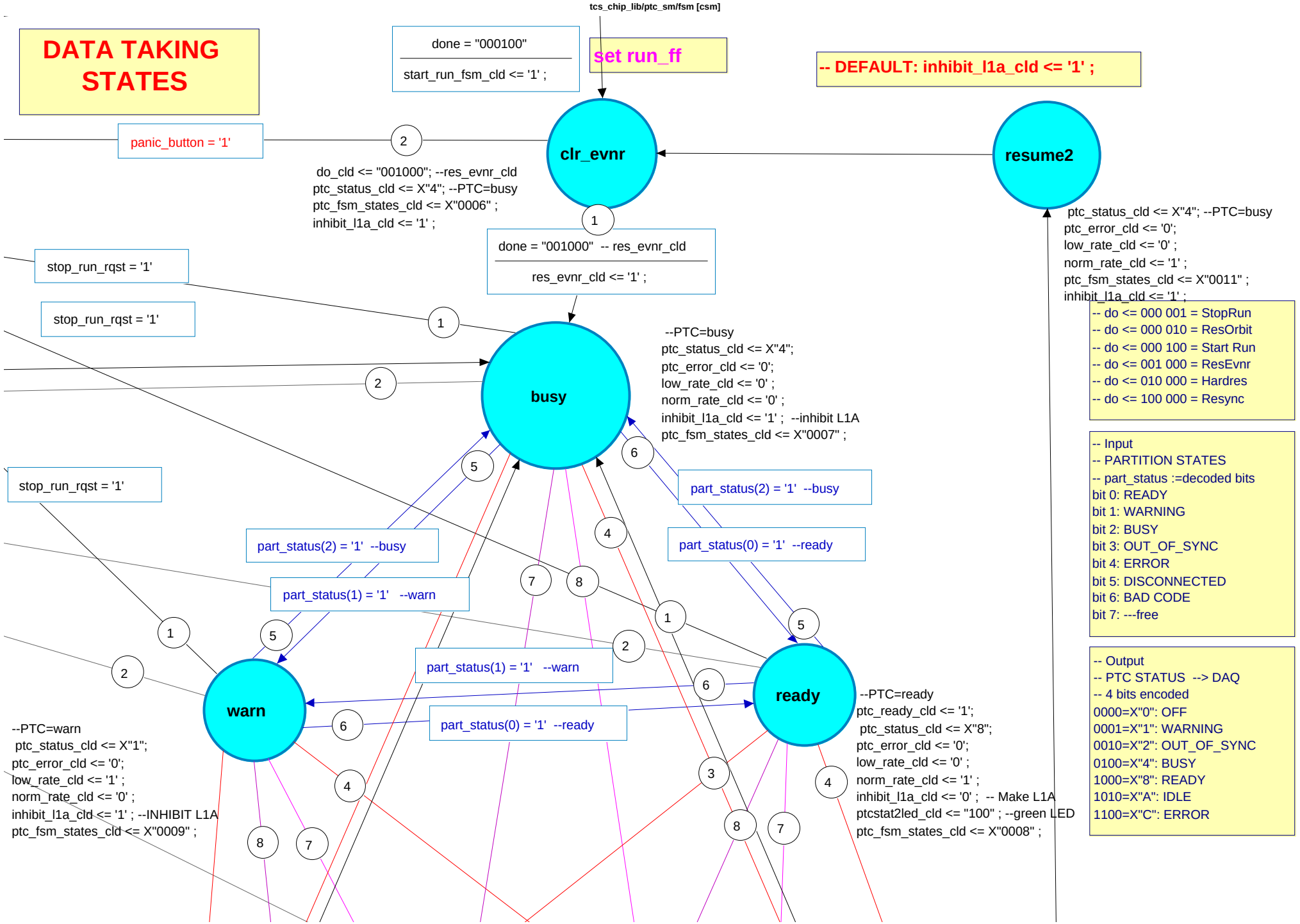
-- do <= 000 001 = StopRun
-- do <= 000 010 = ResOrbit
-- do <= 000 100 = Start Run
-- do <= 001 000 = ResEvnr
-- do <= 010 000 = Hardres
-- do <= 100 000 = Resync

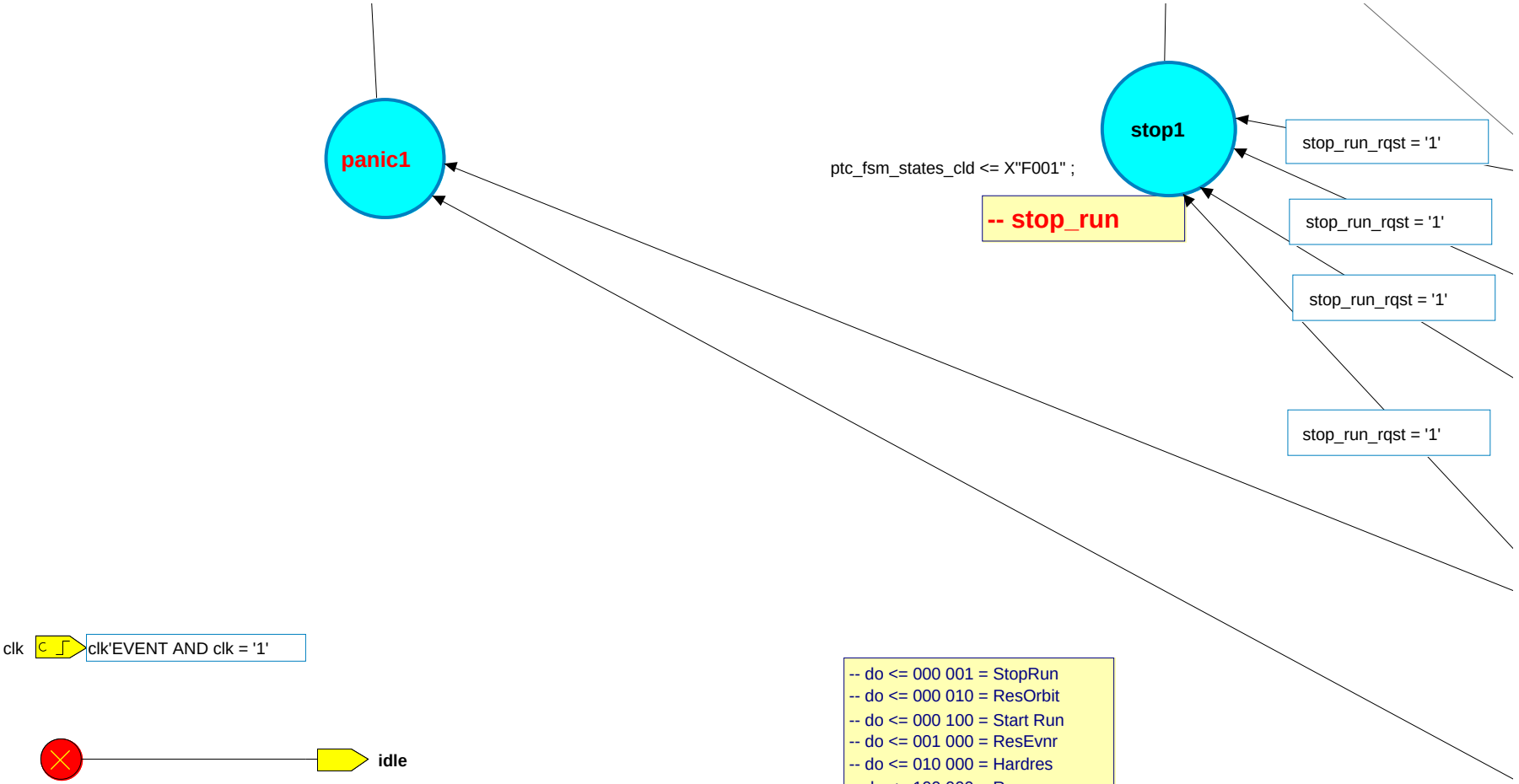
-- Input
-- PARTITION STATES
-- part_status :=decoded bits
bit 0: READY
bit 1: WARNING
bit 2: BUSY
bit 3: OUT_OF_SYNC
bit 4: ERROR
bit 5: DISCONNECTED
bit 6: BAD CODE
bit 7: ---free

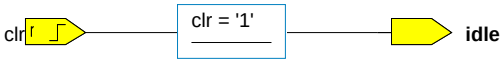
-- Output
-- PTC STATUS --> DAQ
-- 4 bits encoded
0000=X"0": OFF
0001=X"1": WARNING
0010=X"2": OUT_OF_SYNC
0100=X"4": BUSY
1000=X"8": READY
1010=X"A": IDLE
1100=X"C": ERROR



-- PTC waits until disconnected Detector Partition has been reconnected to resume.


DATA TAKING STATES
done = "000100"
start_run_fsm_cld <= '1' ;
set run_ff
-- DEFAULT: inhibit_l1a_cld <= '1' ;
panic_button = '1'
clr_evnr
resume2
do_cld <= "001000"; --res_evnr_cld
ptc_status_cld <= X"4"; --PTC=busy
ptc_fsm_states_cld <= X"0006" ;
inhibit_l1a_cld <= '1' ;
done = "001000" -- res_evnr_cld
res_evnr_cld <= '1' ;
ptc_status_cld <= X"4"; --PTC=busy
ptc_error_cld <= '0';
low_rate_cld <= '0' ;
norm_rate_cld <= '1' ;
ptc_fsm_states_cld <= X"0011" ;
inhibit_l1a_cld <= '1' ;
stop_run_rqst = '1'
stop_run_rqst = '1'
busy
--PTC=busy
ptc_status_cld <= X"4";
ptc_error_cld <= '0';
low_rate_cld <= '0' ;
norm_rate_cld <= '0' ;
inhibit_l1a_cld <= '1' ; --inhibit L1A
ptc_fsm_states_cld <= X"0007" ;
-- do <= 000 001 = StopRun
-- do <= 000 010 = ResOrbit
-- do <= 000 100 = Start Run
-- do <= 001 000 = ResEvnr
-- do <= 010 000 = Hardres
-- do <= 100 000 = Resync
stop_run_rqst = '1'
part_status(2) = '1' --busy
part_status(0) = '1' --ready
part_status(2) = '1' --busy
part_status(1) = '1' --warn
part_status(1) = '1' --warn
part_status(0) = '1' --ready
-- Input
-- PARTITION STATES
-- part_status :=decoded bits
bit 0: READY
bit 1: WARNING
bit 2: BUSY
bit 3: OUT_OF_SYNC
bit 4: ERROR
bit 5: DISCONNECTED
bit 6: BAD CODE
bit 7: ---free
warn
ready
--PTC=warn
ptc_status_cld <= X"1";
ptc_error_cld <= '0';
low_rate_cld <= '1' ;
norm_rate_cld <= '0' ;
inhibit_l1a_cld <= '1' ; --INHIBIT L1A
ptc_fsm_states_cld <= X"0009" ;
--PTC=ready
ptc_ready_cld <= '1';
ptc_status_cld <= X"8";
ptc_error_cld <= '0';
low_rate_cld <= '0' ;
norm_rate_cld <= '1' ;
inhibit_l1a_cld <= '0' ; -- Make L1A
ptcstat2led_cld <= "100" ; --green LED
ptc_fsm_states_cld <= X"0008" ;
-- Output
-- PTC STATUS --> DAQ
-- 4 bits encoded
0000=X"0": OFF
0001=X"1": WARNING
0010=X"2": OUT_OF_SYNC
0100=X"4": BUSY
1000=X"8": READY
1010=X"A": IDLE
1100=X"C": ERROR

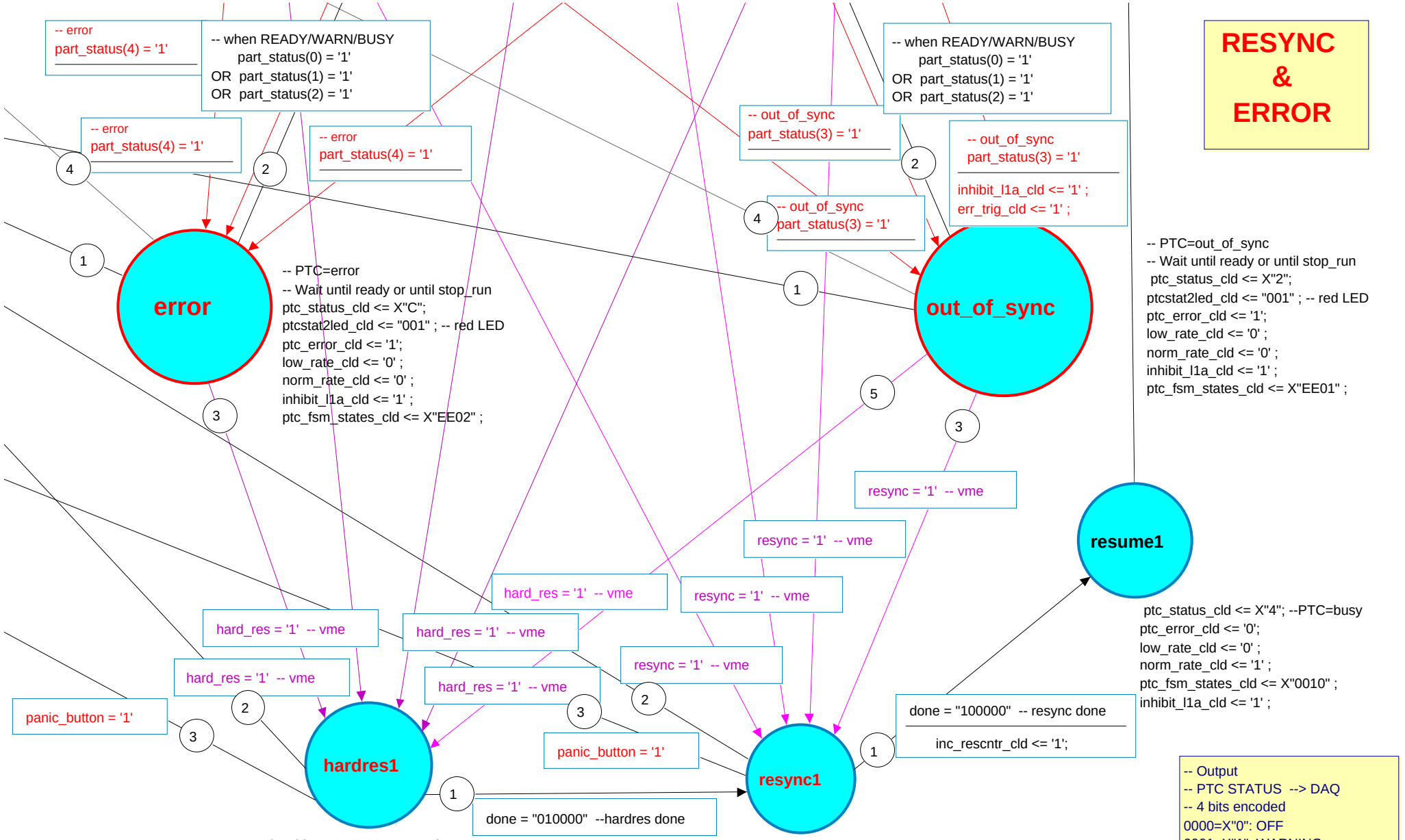


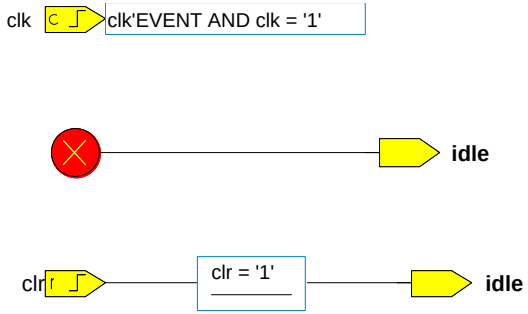



```
-- do <= 000 001 = StopRun
-- do <= 000 010 = ResOrbit
-- do <= 000 100 = Start Run
-- do <= 001 000 = ResEvnr
-- do <= 010 000 = Hardres
-- do <= 100 000 = Resync
```

```
-- Input
-- PARTITION STATES
-- part_status :=decoded bits
bit 0: READY
bit 1: WARNING
bit 2: BUSY
bit 3: OUT_OF_SYNC
bit 4: ERROR
bit 5: DISCONNECTED
bit 6: BAD CODE
bit 7: ---free
```

```
-- Output
-- PTC STATUS  --> DAQ
-- 4 bits encoded
0000=X"0": OFF
0001=X"1": WARNING
0010=X"2": OUT_OF_SYNC
0100=X"4": BUSY
1000=X"8": READY
1010=X"A": IDLE
1100=X"C": ERROR
```


RESYNC & ERROR
error
out_of_sync
resume1
hardres1
resync1
-- error
part_status(4) = '1'
-- when READY/WARN/BUSY
part_status(0) = '1'
OR part_status(1) = '1'
OR part_status(2) = '1'
-- out_of_sync
part_status(3) = '1'
inhibit_l1a_cld <= '1' ;
err_trig_cld <= '1' ;
-- PTC=error
-- Wait until ready or until stop_run
ptc_status_cld <= X"C";
ptcstat2led_cld <= "001" ; -- red LED
ptc_error_cld <= '1';
low_rate_cld <= '0' ;
norm_rate_cld <= '0' ;
inhibit_l1a_cld <= '1' ;
ptc_fsm_states_cld <= X"EE02" ;
-- PTC=out_of_sync
-- Wait until ready or until stop_run
ptc_status_cld <= X"2";
ptcstat2led_cld <= "001" ; -- red LED
ptc_error_cld <= '1';
low_rate_cld <= '0' ;
norm_rate_cld <= '0' ;
inhibit_l1a_cld <= '1' ;
ptc_fsm_states_cld <= X"EE01" ;
resync = '1' -- vme
hard_res = '1' -- vme
panic_button = '1'
done = "100000" -- resync done
inc_rescntr_cld <= '1';
ptc_status_cld <= X"4"; --PTC=busy
ptc_error_cld <= '0';
low_rate_cld <= '0' ;
norm_rate_cld <= '1' ;
ptc_fsm_states_cld <= X"0010" ;
inhibit_l1a_cld <= '1' ;
done = "010000" --hardres done
do_cld <= "010000"; -- HardRes
ptc_status_cld <= X"4"; --PTC = busy
ptcstat2led_cld <= "010" ; -- yellow LED
ptc_fsm_states_cld <= X"EE04" ;
inhibit_l1a_cld <= '1' ;
do_cld <= "100000"; -- Resync
ptc_status_cld <= X"4"; --PTC = busy
ptcstat2led_cld <= "010" ; -- yellow LED
ptc_fsm_states_cld <= X"EE03" ; --resync
inhibit_l1a_cld <= '1' ;
-- DEFAULT: inhibit_l1a_cld <= '1' ;
-- Output
-- PTC STATUS --> DAQ
-- 4 bits encoded
0000=X"0": OFF
0001=X"1": WARNING
0010=X"2": OUT_OF_SYNC
0100=X"4": BUSY
1000=X"8": READY
1010=X"A": IDLE
1100=X"C": ERROR


clk
C
clk'EVENT AND clk = '1'
idle
clr
r
clr = '1'
idle

Global Actions **Concurrent Statements** **Architecture Declarations**

Pre Actions:

Post Actions:

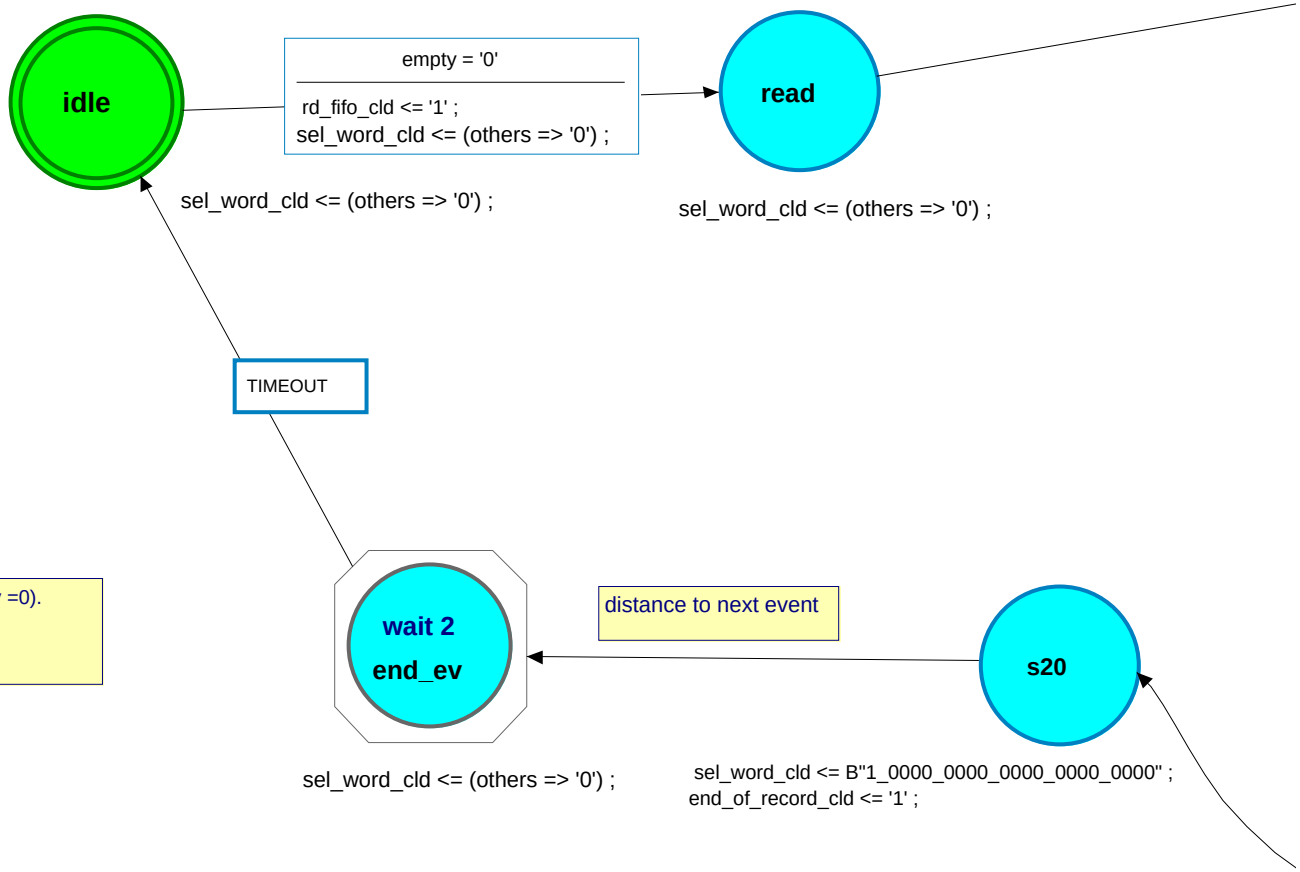
Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
```

Signals Status

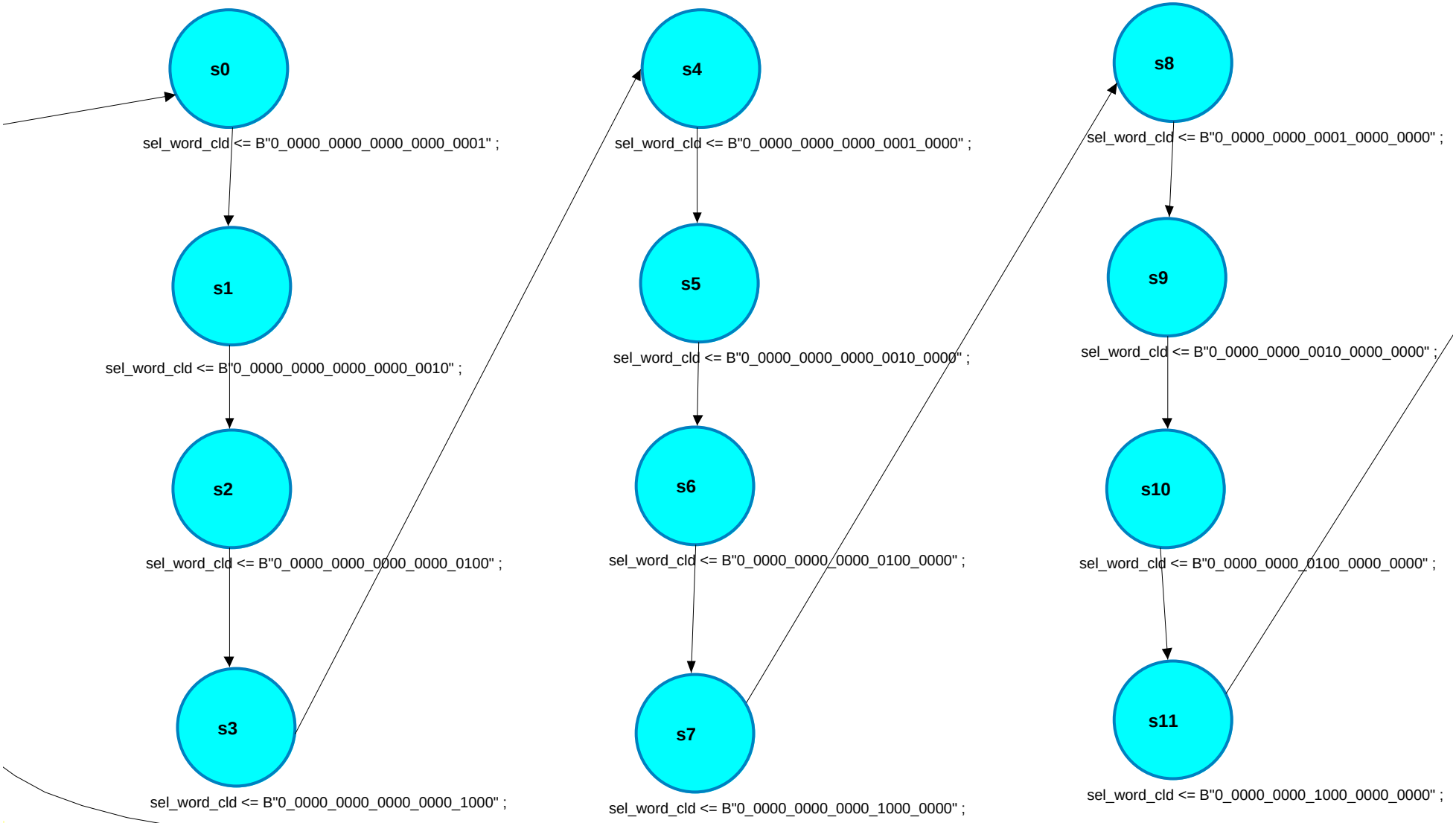
SIGNAL	MODE	DEFAULT	RESET	Process Declarations
end_of_record	OUT	'0'	'0'	Clocked Process: SCHEME
rd_fifo	OUT	'0'	'0'	CLKD
sel_word	OUT	(OTHERS => '0')	(OTHERS => '0')	CLKD
				CLKD

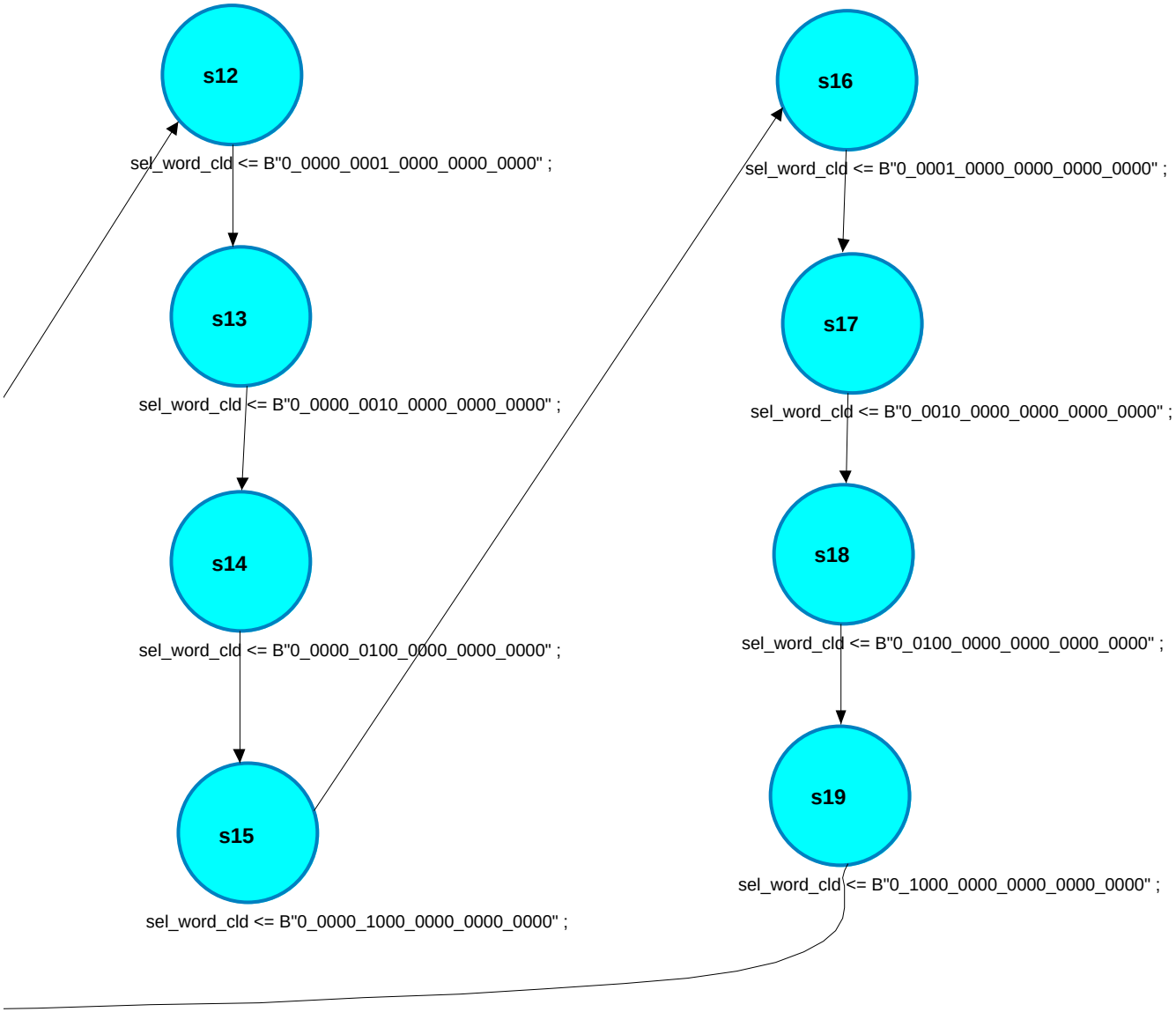
State Register Statements



ROC sends events as long as there are some in the FIFOs (empty =0).
ROC ignores fifo_full flag.
But not all are transferred.--> See ROP logic

<company name>		Project:	tcsv2
Title:	Readout Control ROC	<enter comments here>	
Path:	tcs_chip_lib/tcs_roc/fsm		
Edited:	by taurok on 31 Jul 2009		


s0
sel_word_cld <= B"0_0000_0000_0000_0000_0001" ;
s1
sel_word_cld <= B"0_0000_0000_0000_0000_0010" ;
s2
sel_word_cld <= B"0_0000_0000_0000_0000_0100" ;
s3
sel_word_cld <= B"0_0000_0000_0000_0000_1000" ;
s4
sel_word_cld <= B"0_0000_0000_0000_0001_0000" ;
s5
sel_word_cld <= B"0_0000_0000_0000_0010_0000" ;
s6
sel_word_cld <= B"0_0000_0000_0000_0100_0000" ;
s7
sel_word_cld <= B"0_0000_0000_0000_1000_0000" ;
s8
sel_word_cld <= B"0_0000_0000_0001_0000_0000" ;
s9
sel_word_cld <= B"0_0000_0000_0010_0000_0000" ;
s10
sel_word_cld <= B"0_0000_0000_0100_0000_0000" ;
s11
sel_word_cld <= B"0_0000_0000_1000_0000_0000" ;


s12
sel_word_cld <= B"0_0000_0001_0000_0000_0000" ;
s13
sel_word_cld <= B"0_0000_0010_0000_0000_0000" ;
s14
sel_word_cld <= B"0_0000_0100_0000_0000_0000" ;
s15
sel_word_cld <= B"0_0000_1000_0000_0000_0000" ;
s16
sel_word_cld <= B"0_0001_0000_0000_0000_0000" ;
s17
sel_word_cld <= B"0_0010_0000_0000_0000_0000" ;
s18
sel_word_cld <= B"0_0100_0000_0000_0000_0000" ;
s19
sel_word_cld <= B"0_1000_0000_0000_0000_0000" ;

Global Actions **Concurrent Statements** **Architecture Declarations** **State Register Statements** **Process Declarations**

Pre Actions:

Post Actions:

Clocked Process:

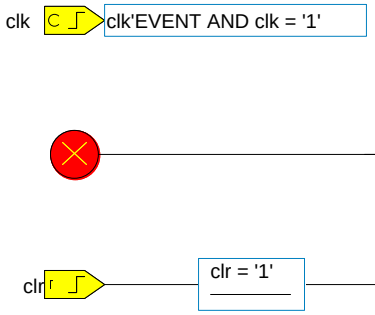
Output Process:

Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
```

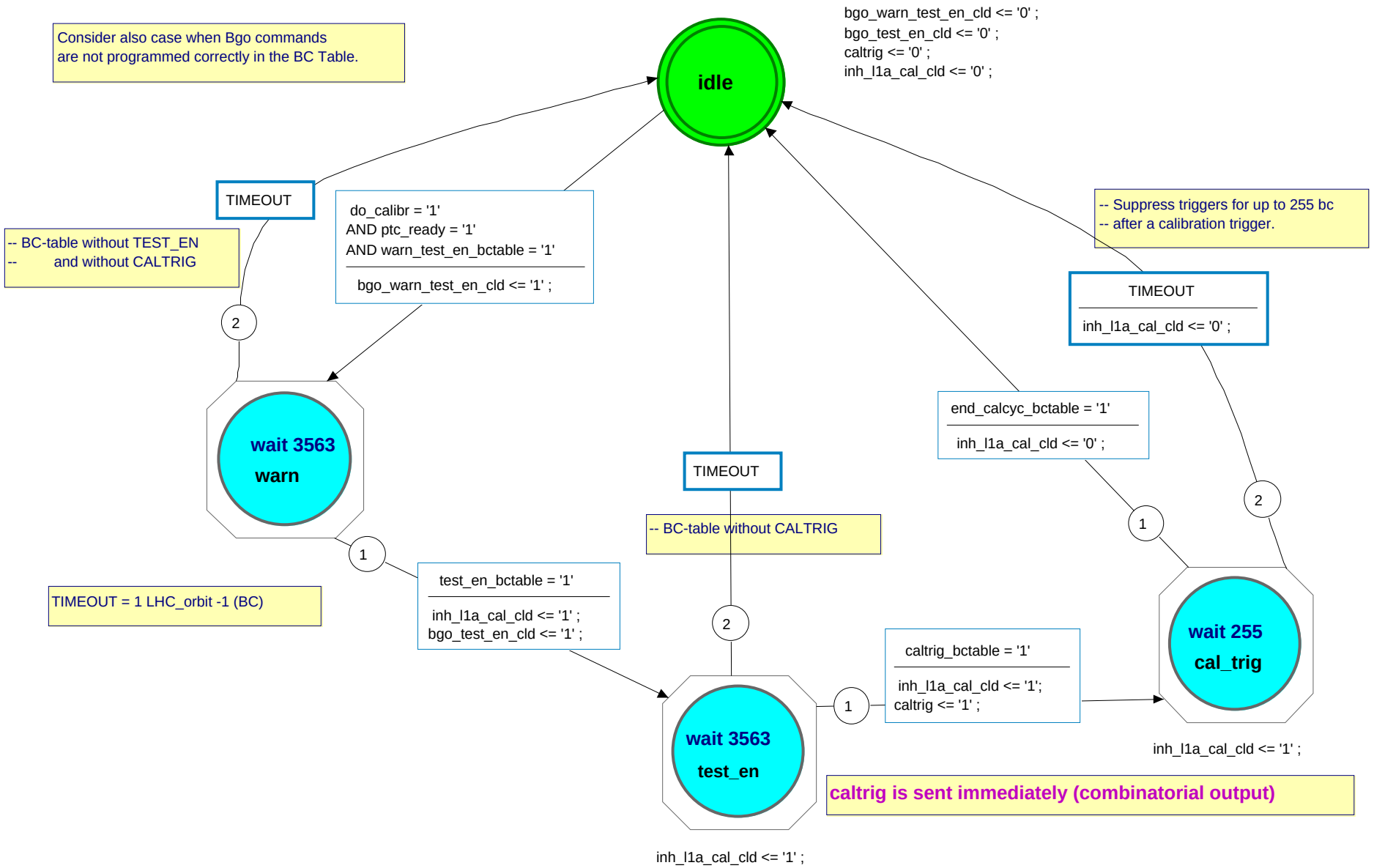
Signals Status

SIGNAL	MODE	DEFAULT	RESET	SCHEME
bgo_test_en	OUT	'0'	'0'	CLKD
bgo_warn_test_en	OUT	'0'	'0'	CLKD
caltrig	OUT	'0'		COMB
inh_l1a_cal	OUT	'0'	'0'	CLKD




```
-- V101F caltrig is sent immediately
-- V101E  March 2009
-- Correct BC-Table bits required!
-- Suppress triggers for up to 255 bc
-- after a calibration trigger to avoid
-- triggers generated by
-- 'after-pulses' from Lasers in ECAL.
```

Institut für Hochenergiephysik		Project:	tcsv2
Title:	Calibration cycle	Designed for tcs chip Version V001C	
Path:	tcs_chip_lib/calibr_sm/fsm		
Edited:	by taurok on 18 Aug 2009		


Consider also case when Bgo commands
are not programmed correctly in the BC Table.
idle
bgo_warn_test_en_cld <= '0' ;
bgo_test_en_cld <= '0' ;
caltrig <= '0' ;
inh_l1a_cal_cld <= '0' ;
TIMEOUT
-- BC-table without TEST_EN
-- and without CALTRIG
2
do_calibr = '1'
AND ptc_ready = '1'
AND warn_test_en_bctable = '1'
bgo_warn_test_en_cld <= '1' ;
-- Suppress triggers for up to 255 bc
-- after a calibration trigger.
TIMEOUT
inh_l1a_cal_cld <= '0' ;
wait 3563
warn
end_calcyc_bctable = '1'
inh_l1a_cal_cld <= '0' ;
TIMEOUT
-- BC-table without CALTRIG
1
2
TIMEOUT = 1 LHC_orbit -1 (BC)
test_en_bctable = '1'
inh_l1a_cal_cld <= '1' ;
bgo_test_en_cld <= '1' ;
2
caltrig_bctable = '1'
inh_l1a_cal_cld <= '1';
caltrig <= '1' ;
1
wait 255
cal_trig
inh_l1a_cal_cld <= '1' ;
wait 3563
test_en
caltrig is sent immediately (combinatorial output)
inh_l1a_cal_cld <= '1' ;

Global Actions
Pre Actions:
Post Actions:

Concurrent Statements

State Register Statements

Process Declarations
Clocked Process:
Output Process:

Signals Status

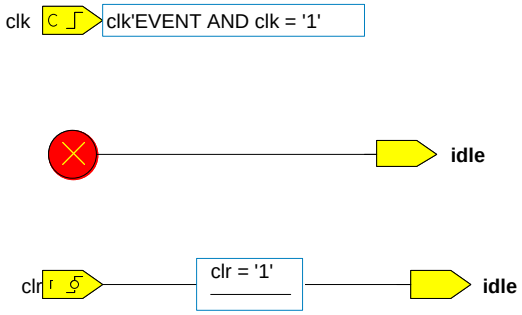
SIGNAL	MODE	DEFAULT	RESET	SCHEME
active_orbit	OUT	'0'	'0'	CLKD
done	OUT	'0'	'0'	CLKD
r_cntr	LOCAL		(others => '0')	CLKD
s_cntr	LOCAL		(others => '0')	CLKD

Package List

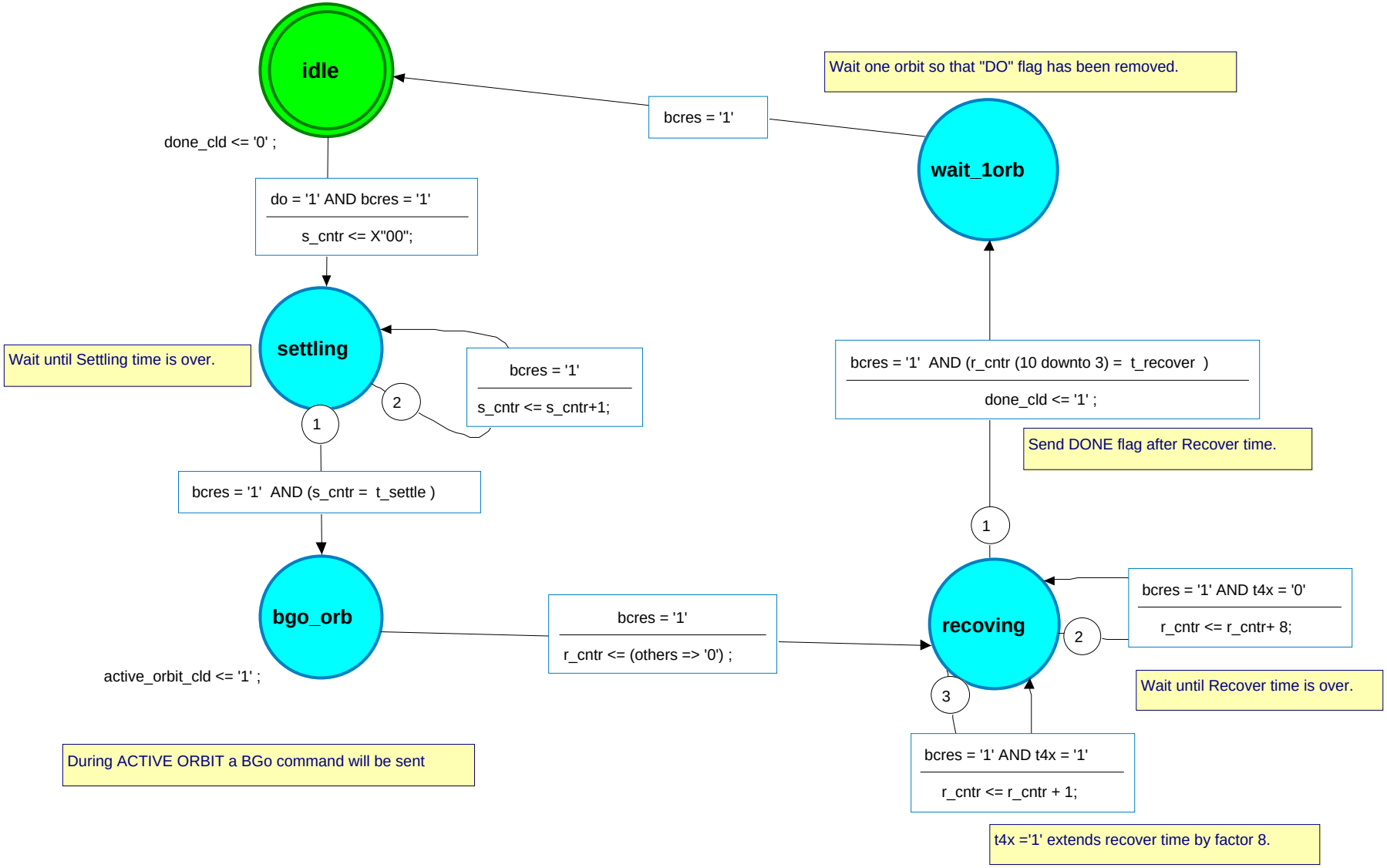
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all; -- ... decr. counters
```

Architecture Declarations

```
SIGNAL s_cntr : std_logic_vector(7 downto 0);
SIGNAL r_cntr : std_logic_vector(10 downto 0);
```



<company name>		Project:	tcsv2
Title:	<enter diagram title here>	<enter comments here>	
Path:	tcs_chip_lib/settle_recover_sm/fsm		
Edited:	by taurok on 31 Jul 2009		


idle
done_cld <= '0' ;
do = '1' AND bcres = '1'
s_cntr <= X"00";
settling
Wait until Settling time is over.
bcres = '1'
s_cntr <= s_cntr+1;
2
1
bcres = '1' AND (s_cntr = t_settle)
bgo_orb
active_orbit_cld <= '1' ;
bcres = '1'
r_cntr <= (others => '0') ;
During ACTIVE ORBIT a BGo command will be sent
bcres = '1'
Wait one orbit so that "DO" flag has been removed.
wait_1orb
bcres = '1' AND (r_cntr (10 downto 3) = t_recover)
done_cld <= '1' ;
Send DONE flag after Recover time.
1
recoving
bcres = '1' AND t4x = '0'
r_cntr <= r_cntr+ 8;
2
Wait until Recover time is over.
3
bcres = '1' AND t4x = '1'
r_cntr <= r_cntr + 1;
t4x ='1' extends recover time by factor 8.

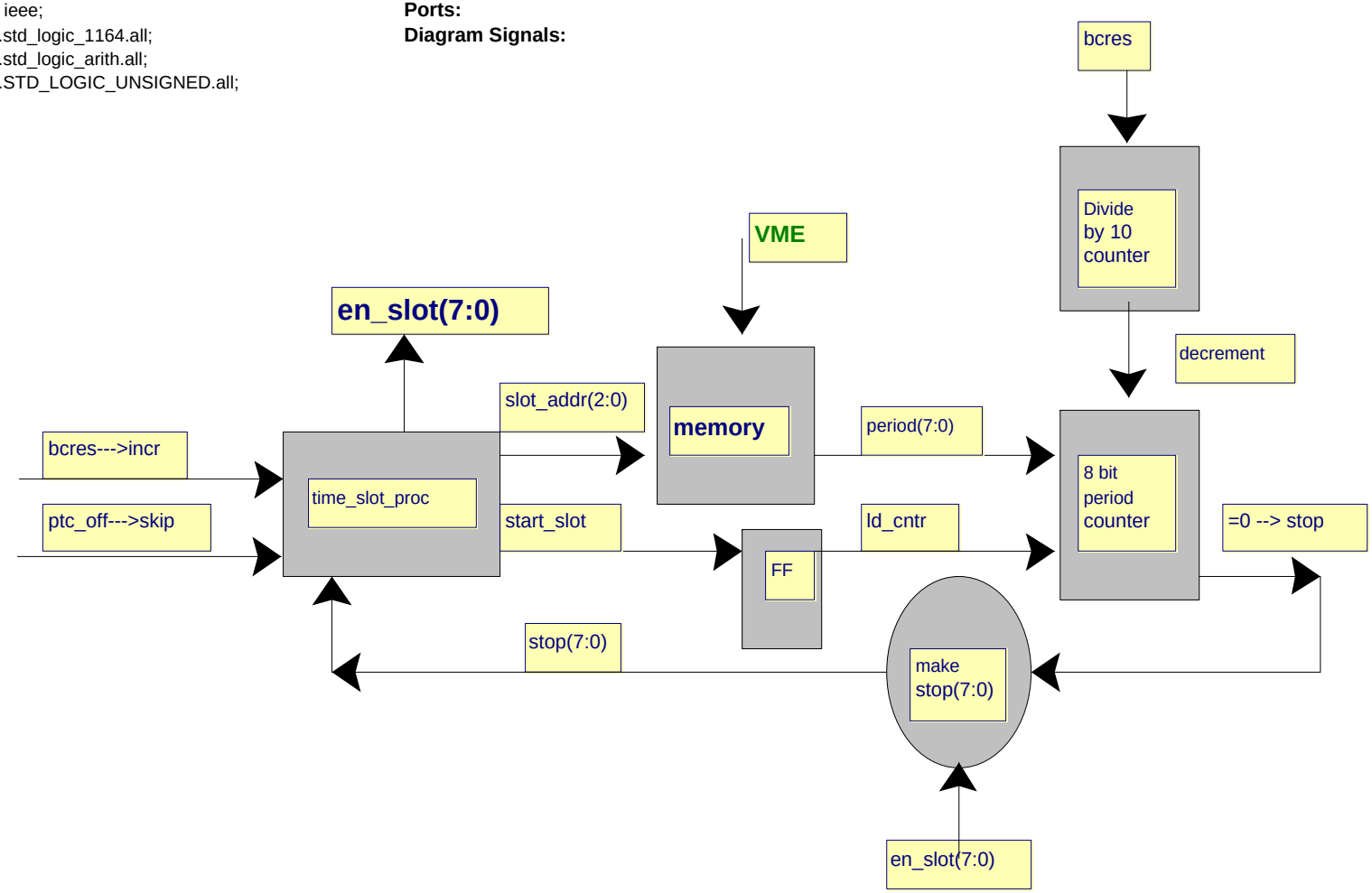
Package List

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;

Declarations

Ports:

Diagram Signals:



CONCEPT of TIME_SLOT_GENERATOR

NO FUNCTION by this module.

<company name>		Project:	tcs_chip
Title:	<enter diagram title here>	Shows the structure of the TIME_SLOT_GENERATOR	
Path:	tcs_chip_lib/time_slot_scheme/struct		
Edited:	by taurok on 30 Mär 2007		