Declarations

Ports:

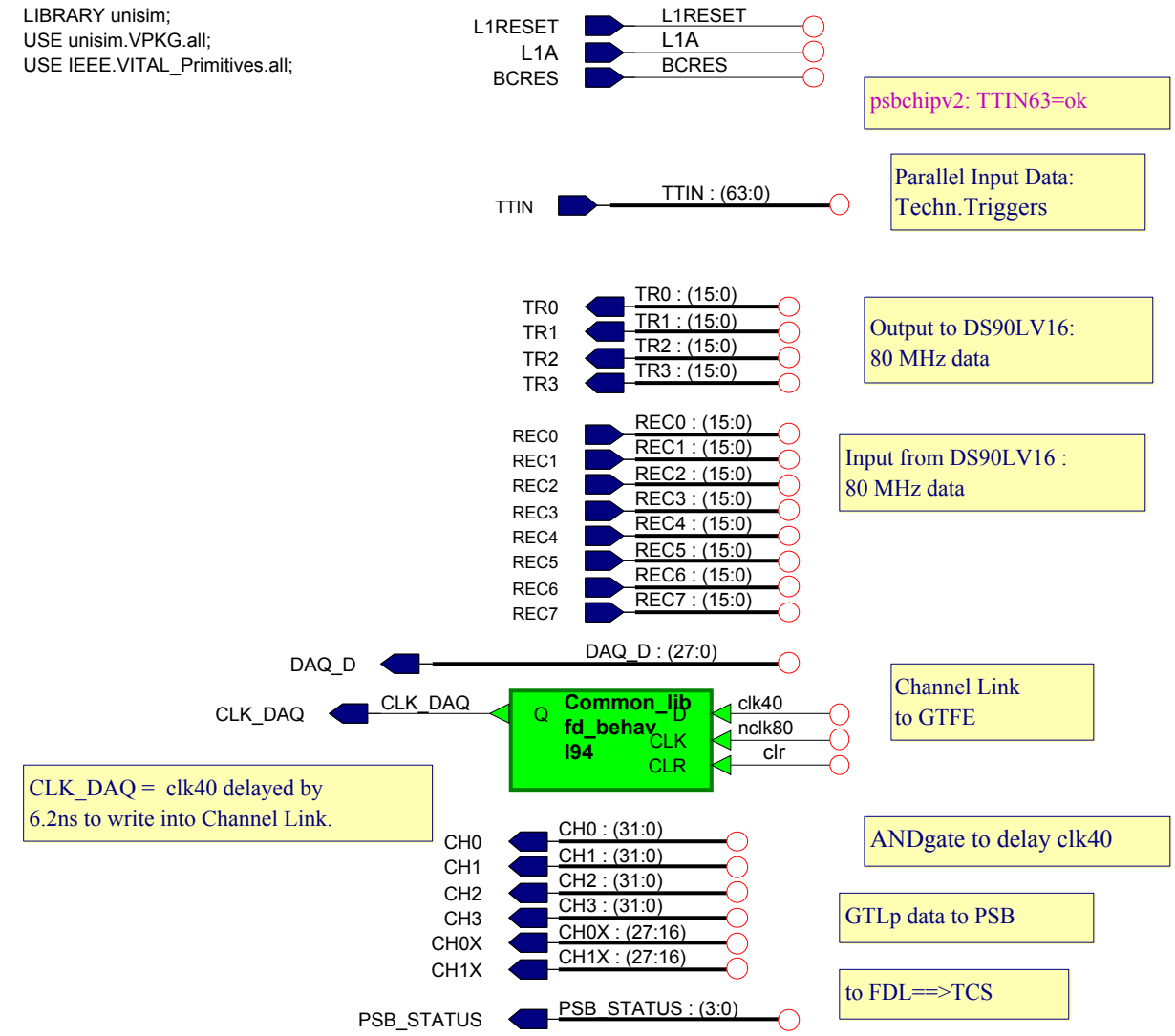
```
BCRES                  : std_logic
BX                     : std_logic_vector(11 DOWNTO 0)
CLK80_TO_PSB           : std_logic
CLK_FBIN_PSB           : std_logic
CLK_TO_PSB             : std_logic
EN_PSB                 : std_logic
EN_PSB_MEM             : std_logic
INACTIVE               : std_logic
L1A                    : std_logic
L1RESET                : std_logic
RDRQST                 : std_logic
REC0                   : std_logic_VECTOR(15 DOWNTO 0)
REC1                   : std_logic_VECTOR(15 DOWNTO 0)
REC2                   : std_logic_VECTOR(15 DOWNTO 0)
REC3                   : std_logic_VECTOR(15 DOWNTO 0)
REC4                   : std_logic_VECTOR(15 DOWNTO 0)
REC5                   : std_logic_VECTOR(15 DOWNTO 0)
REC6                   : std_logic_VECTOR(15 DOWNTO 0)
REC7                   : std_logic_VECTOR(15 DOWNTO 0)
RESET_DCM_PSB_CHIP     : std_logic
RESET_PSB_CHIP         : std_logic
STROB                  : std_logic_VECTOR(2 DOWNTO 0)
TTIN                   : std_logic_VECTOR(63 DOWNTO 0)
VADDR                  : std_logic_VECTOR(19 DOWNTO 1)
WR_PSB                 : std_logic
BCRES_PAN              : std_logic
CH0                    : std_logic_vector(31 DOWNTO 0)
CH0X                   : std_logic_vector(27 DOWNTO 16)
CH1                    : std_logic_vector(31 DOWNTO 0)
CH1X                   : std_logic_vector(27 DOWNTO 16)
CH2                    : std_logic_vector(31 DOWNTO 0)
CH3                    : std_logic_vector(31 DOWNTO 0)
CLK_DAQ                : std_logic
CLK_FBOUT_PSB          : std_logic
CLK_LOCKED_PSB         : std_logic
DAQ_D                  : std_logic_vector(27 DOWNTO 0)
ERR_LED                : std_logic
IRQ_FR_PSB             : std_logic
NBERR_PSB              : std_logic           := '1'
NDTACK_PSB             : std_logic REGISTER := '1'
PSB_STATUS             : std_logic_vector(3 DOWNTO 0)
PSB_TEST               : std_logic_vector(6 DOWNTO 0)
TR0                    : std_logic_VECTOR(15 DOWNTO 0)
TR1                    : std_logic_vector(15 DOWNTO 0)
TR2                    : std_logic_vector(15 DOWNTO 0)
TR3                    : std_logic_vector(15 DOWNTO 0)
VDATA                  : std_logic_vector(15 DOWNTO 0)
```

Diagram Signals:

```
SIGNAL BCRESx                : std_logic
SIGNAL BCRes_int             : std_logic
SIGNAL BCRes_vme             : std_logic
SIGNAL CLK0                  : std_ulogic          := '0'
SIGNAL CLK2X                 : std_ulogic          := '0'
SIGNAL CLK2X180              : std_ulogic          := '0'
SIGNAL CLKFX                 : std_ulogic          := '0'
SIGNAL CLKFX180              : std_ulogic          := '0'
SIGNAL CLKIN                 : std_logic
SIGNAL COMP_DLY0             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY1             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY2             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY3             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY4             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY5             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY6             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL COMP_DLY7             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL L1A_int               : std_logic
SIGNAL L1Ax                  : std_logic
SIGNAL L1RESETx              : std_logic
```

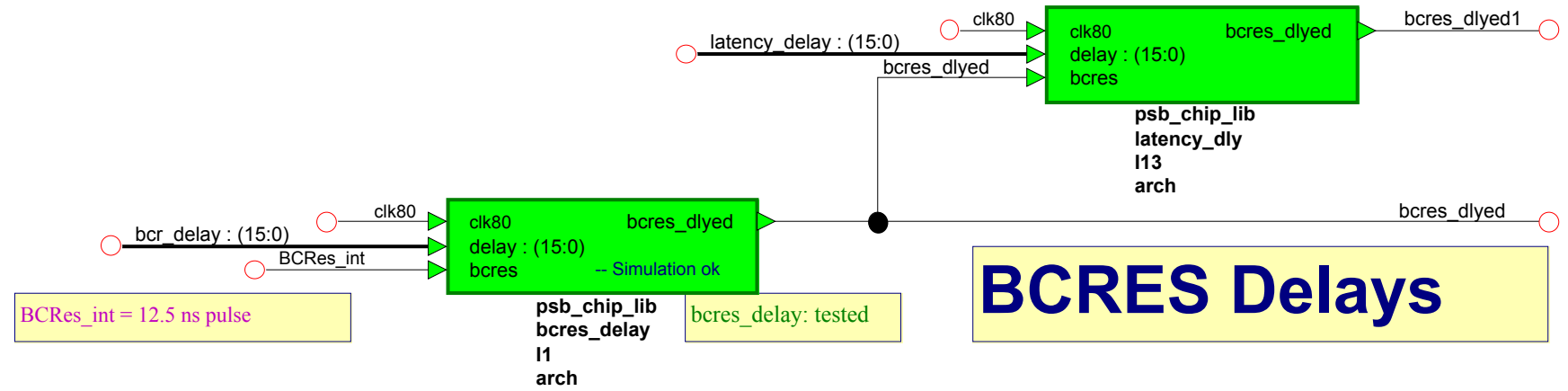
Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
USE IEEE.VITAL_Timing.all;
LIBRARY STD;
USE STD.TEXTIO.all;
LIBRARY unisim;
USE unisim.VPKG.all;
USE IEEE.VITAL_Primitives.all;
```



HEPHY		Project:	psb_chip
Title:	PSB_CHIP_V2	Design for Calo+Totem trigger data Simplified Design will be done for Technical Trigger data	
Path:	psb_chip_lib/psb_chip_v2/struct		
Edited:	by taurok on 13 Mär 2007		

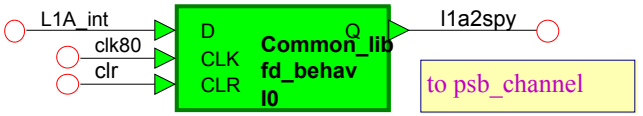
Common LATENCY DELAY for all channels
to read at same time from RingBuffers.
Min.latency = 4/2 = 2bx



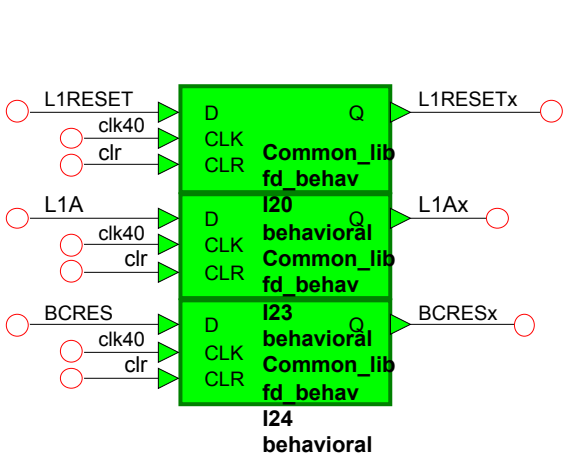
BCRes_int = 12.5 ns pulse

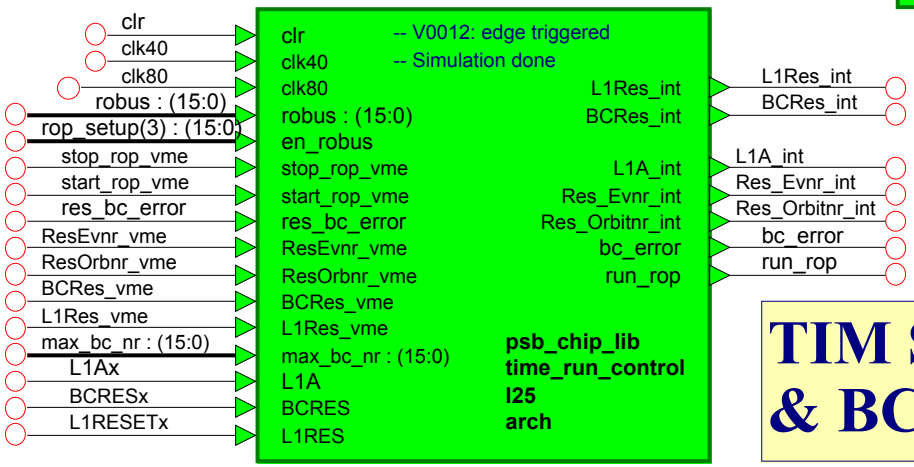
bcres_delay: tested

BCRES Delays



to psb_channel





BCRes_int = 12.5 ns pulse ==> DELAY

L1A_i = 12.5 ns pulse ==> ROP
Res_Evnr, L1Res_int ==> ROP
bc_error, run_rop ==> ROP

TIM Signal Decoder & BC_counter

PSB channels 5 & 4

Channel 5

Channels 4,5,6,7 are not used on PSB3(slot 15) and PSB_T (slot 9).

IN PADS

REC5 : (15:0)
clk160
nclk160

width = 16 (integer)

din : (width-1:0) dat_p : (width-1:0)
clk160 dat_n : (width-1:0)
nclk160

Common_lib
ifddr_vec
I11
behavioral

RECP5 : (15:0)
RECN5 : (15:0)

gnd_16 : (15:0)
TRX5 : (15:0)

lvds_data : (15:0) tst_en_spy
tst_we_spy
tr : (15:0) l1a_spy_status : (15:0)
vme_en_spy
vme_we_spy
vaddr : (19:1)
sim_mem : (15:0) vdin : (15:0)
sim_addr : (12:0) vdout : (15:0)

recp : (15:0) phase_cnta : (15:0)
recn : (15:0) phase_cntb : (15:0)
clk40
clk80 chout : (15:0)
clk160
nclk160 nchout : (15:0)
clr
l1a
bcres_dlyed
run_next_orbit
stop_spying
chan_reg : (15:0) ringbuf_address : (12:0)
chan_delay : (15:0) inc_phase : (3:0)
read_phase_cnta bc0_data
read_phase_cntb

psb_chip_lib
psb_channel_v2
I52

clk40
clk80
clk160
nclk160
clr

l1a2spy
bcres_dlyed
run_next_orbit(5) : (7:0)
stop_spying(5) : (15:0)
chan_reg5 : (15:0)
chan_delay5 : (15:0)
rd_phase_cnta(5) : (7:0)
rd_phase_cntb(5) : (7:0)

tst_en_spy5

VME acces to SIM_SPY mem

l1a_spy_status5 : (15:0)
vme_en_spy(5) : (7:0)
vme_we_spy(5) : (7:0)
vme_addr : (19:1)
vdin : (15:0)
vdout_ch5 : (15:0)

phase_cnta5 : (15:0)
phase_cntb5 : (15:0)

chout5 : (15:0)

nchout5

CH2(31:16) : (31:0)

width = 16 (integer)

d : (width-1:0)
q : (width-1:0)
clk80 clk **Common_lib**
clr clr **ofd_vec**
I4
behavioral

OUT PADS

bc0_data(5) : (7:0)

VME register

Channel 4

CABLE 2

IN PADS

REC4 : (15:0)
clk160
nclk160

width = 16 (integer)

din : (width-1:0) dat_p : (width-1:0)
clk160 dat_n : (width-1:0)
nclk160

Common_lib
ifddr_vec
I5
behavioral

RECP4 : (15:0)
RECN4 : (15:0)

gnd_16 : (15:0)
TRX4 : (15:0)

lvds_data : (15:0) tst_en_spy
tst_we_spy
tr : (15:0) l1a_spy_status : (15:0)
vme_en_spy
vme_we_spy
vaddr : (19:1)
sim_mem : (15:0) vdin : (15:0)
sim_addr : (12:0) vdout : (15:0)

recp : (15:0) phase_cnta : (15:0)
recn : (15:0) phase_cntb : (15:0)
clk40
clk80 chout : (15:0)
clk160
nclk160 nchout : (15:0)
clr
l1a
bcres_dlyed
run_next_orbit
stop_spying
chan_reg : (15:0) ringbuf_address : (12:0)
chan_delay : (15:0) inc_phase : (3:0)
read_phase_cnta bc0_data
read_phase_cntb

psb_chip_lib
psb_channel_v2
I56

clk40
clk80
clk160
nclk160
clr

l1a2spy
bcres_dlyed
run_next_orbit(4) : (7:0)
stop_spying(4) : (15:0)
chan_reg4 : (15:0)
chan_delay4 : (15:0)
rd_phase_cnta(4) : (7:0)
rd_phase_cntb(4) : (7:0)

tst_en_spy4

l1a_spy_status4 : (15:0)
vme_en_spy(4) : (7:0)
vme_we_spy(4) : (7:0)
vme_addr : (19:1)
vdin : (15:0)
vdout_ch4 : (15:0)

phase_cnta4 : (15:0)
phase_cntb4 : (15:0)

chout4 : (15:0)

nchout4

CH2(15:0) : (31:0)

width = 16 (integer)

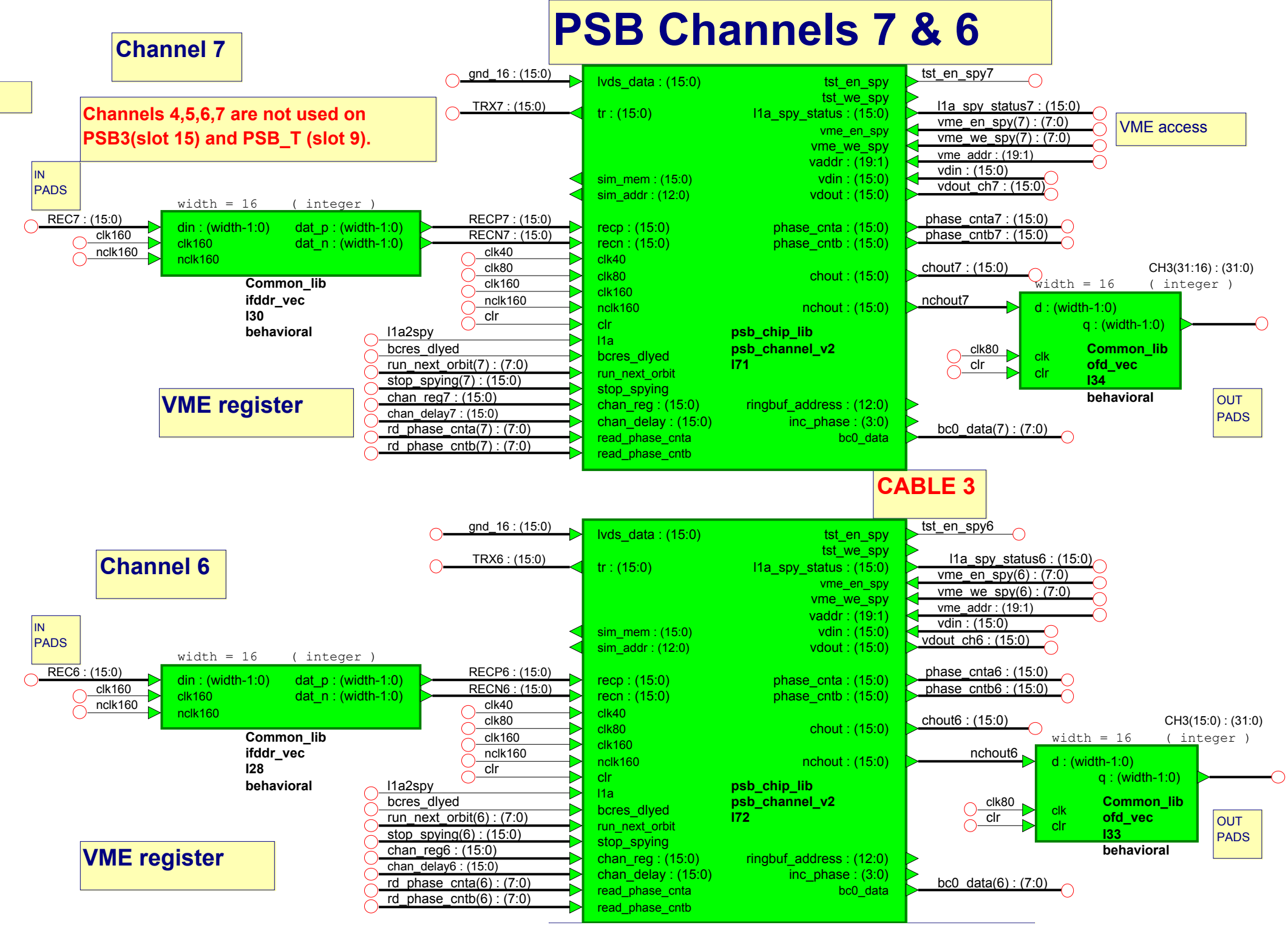
d : (width-1:0)
q : (width-1:0)
clk80 clk **Common_lib**
clr clr **ofd_vec**
I3
behavioral

OUT PADS

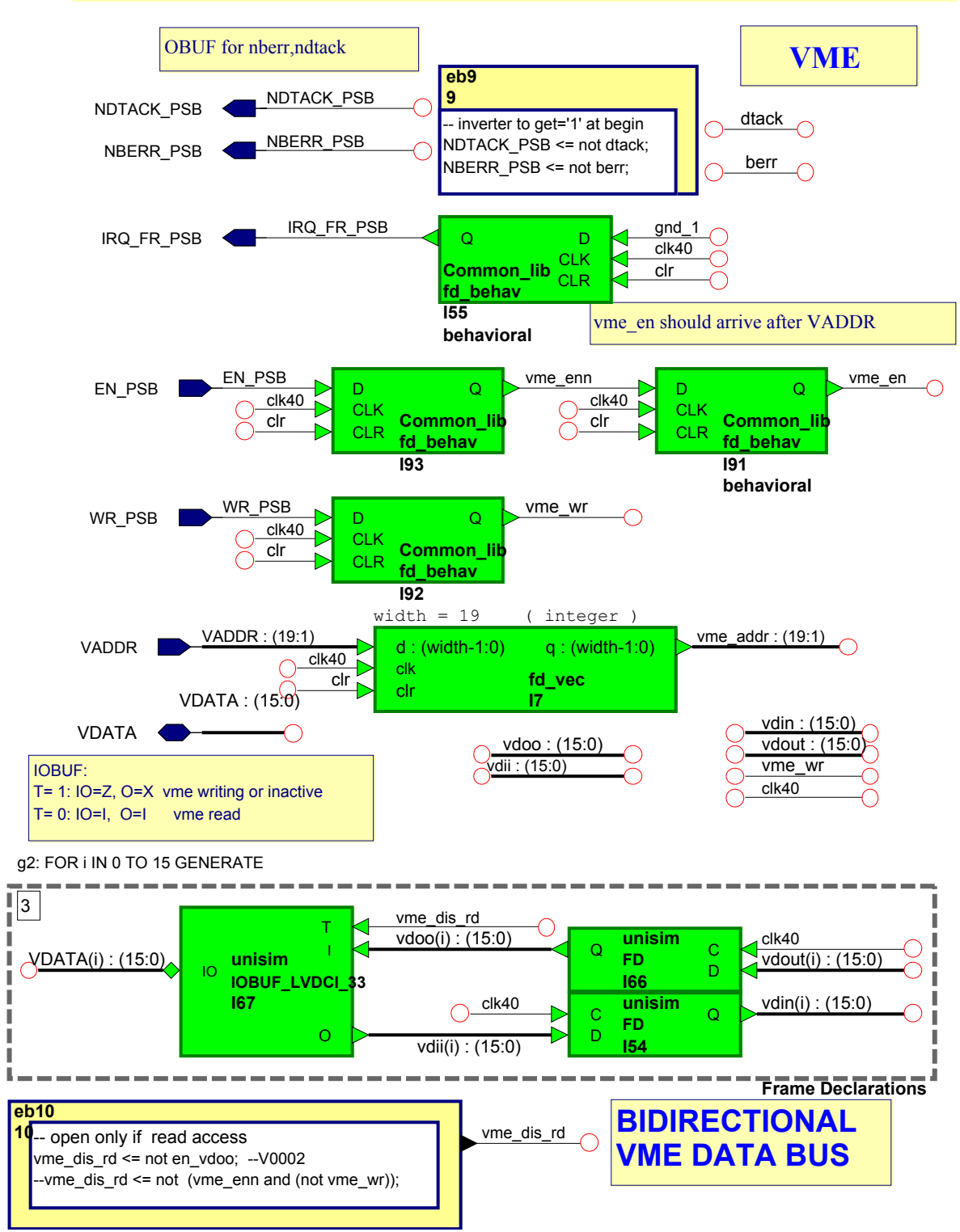
inc_phas4 : (3:0)
bc0_data(4) : (7:0)

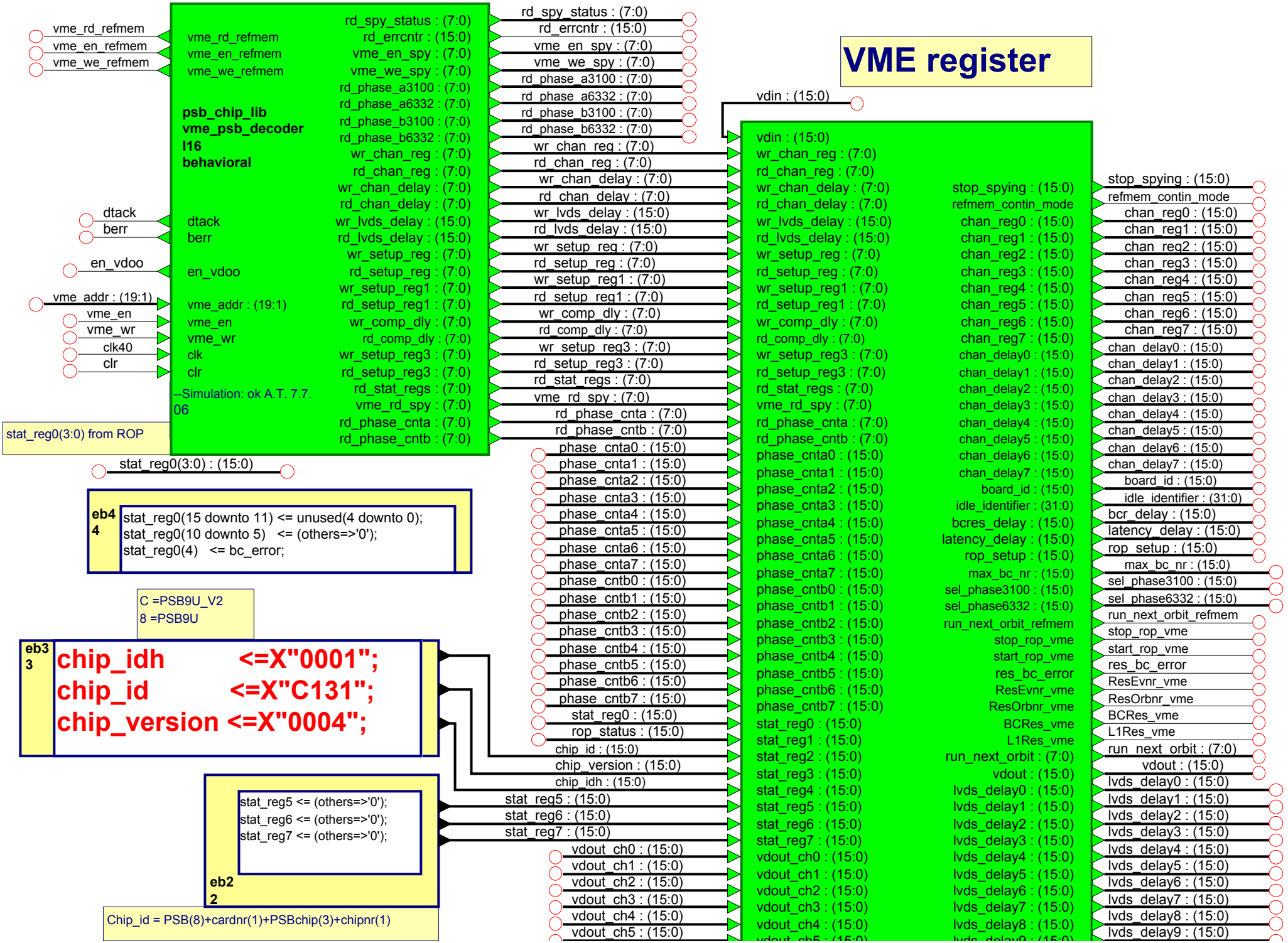
VME register

PSB Channels 7 & 6

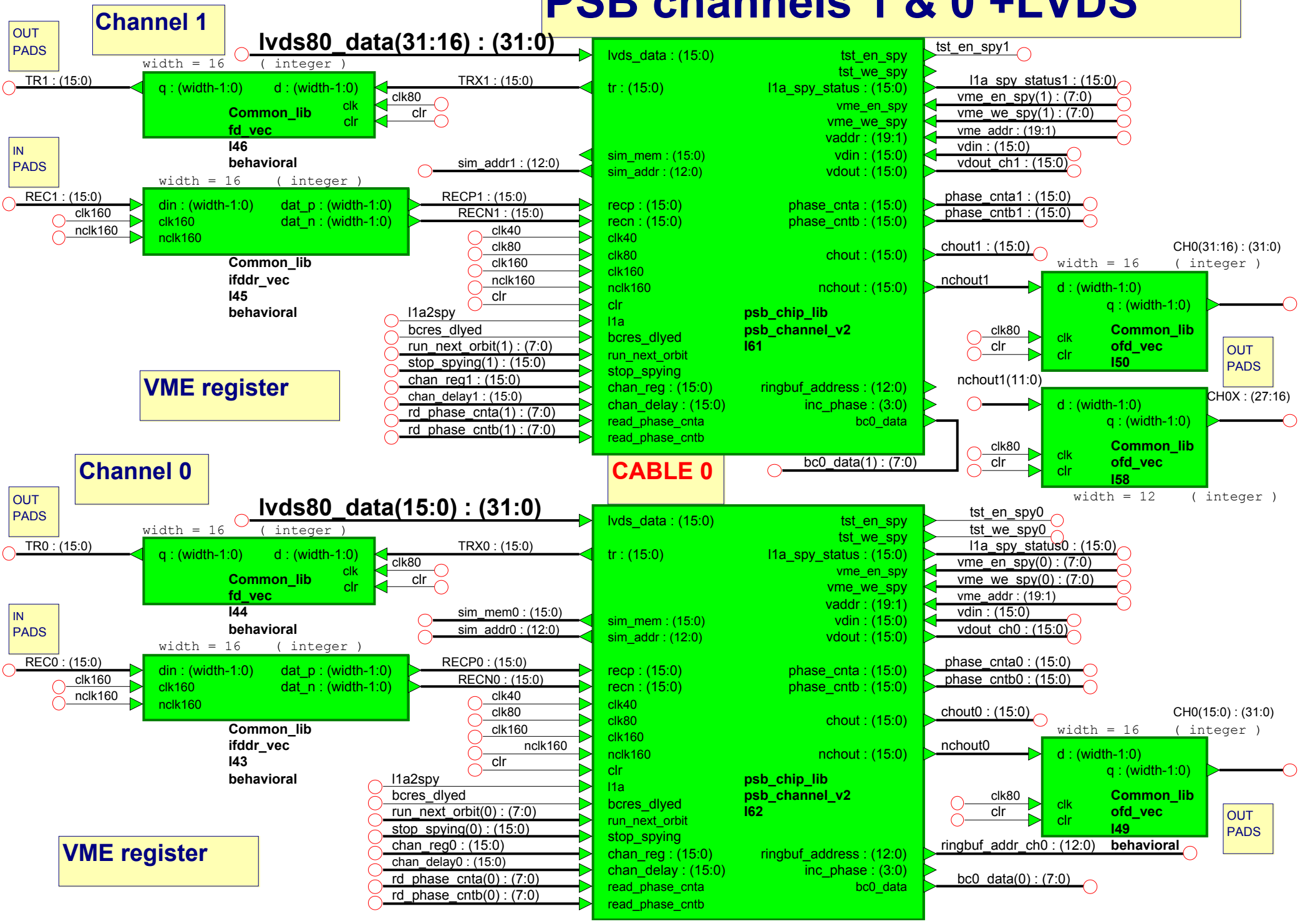


```
SIGNAL L1Res_int              : std_logic
SIGNAL L1Res_vme              : std_logic
SIGNAL PHASE_CNTR_A0_3        : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A12_15      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A16_19      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A20_23      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A24_27      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A28_31      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A32_35      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A36_39      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A40_43      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A44_47      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A48_51      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A4_7        : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A52_55      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A56_59      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A60_63      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_A8_11       : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B0_3        : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B12_15      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B16_19      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B20_23      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B24_27      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B28_31      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B32_35      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B36_39      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B40_43      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B44_47      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B48_51      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B4_7        : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B52_55      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B56_59      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B60_63      : std_logic_vector(15 DOWNTO 0)
SIGNAL PHASE_CNTR_B8_11       : std_logic_vector(15 DOWNTO 0)
SIGNAL RECN0                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN1                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN2                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN3                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN4                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN5                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN6                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECN7                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP0                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP1                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP2                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP3                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP4                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP5                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP6                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL RECP7                  : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL ResEvnr_vme            : std_logic
SIGNAL ResOrbnr_vme           : std_logic
SIGNAL Res_Evnr_int           : std_logic
SIGNAL Res_Orbitnr_int        : std_logic
SIGNAL TRX0                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX1                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX2                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX3                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX4                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX5                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX6                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL TRX7                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL bc0_data               : std_logic_VECTOR(7 DOWNTO 0)
SIGNAL bc_error               : std_logic
SIGNAL bcr_delay              : std_logic_vector(15 DOWNTO 0)
SIGNAL bcres_dlyed            : std_logic
SIGNAL bcres_dlyed1           : std_logic
SIGNAL berr                   : std_logic
SIGNAL board_id               : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay0            : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay1            : std_logic_vector(15 DOWNTO 0)
```

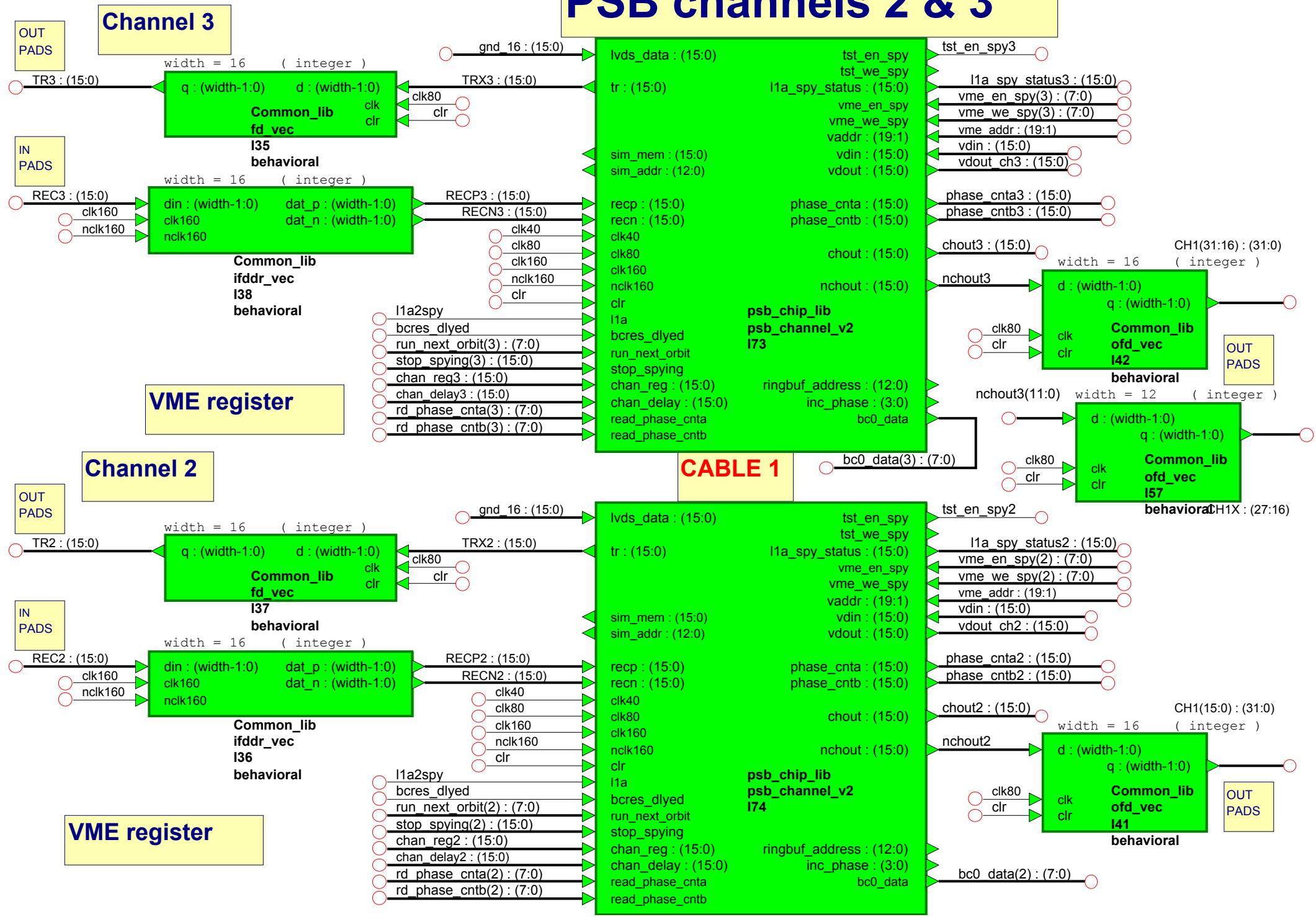



VME register
vme_rd_refmem
vme_en_refmem
vme_we_refmem
psb_chip_lib
vme_psb_decoder
l16
behavioral
dtack
berr
en_vdoo
vme_addr : (19:1)
vme_en
vme_wr
clk40
clr
--Simulation: ok A.T. 7.7.06
rd_spy_status : (7:0)
rd_errcntr : (15:0)
vme_en_spy : (7:0)
vme_we_spy : (7:0)
rd_phase_a3100 : (7:0)
rd_phase_a6332 : (7:0)
rd_phase_b3100 : (7:0)
rd_phase_b6332 : (7:0)
wr_chan_reg : (7:0)
rd_chan_reg : (7:0)
wr_chan_delay : (7:0)
rd_chan_delay : (7:0)
wr_lvds_delay : (15:0)
rd_lvds_delay : (15:0)
wr_setup_reg : (7:0)
rd_setup_reg : (7:0)
wr_setup_reg1 : (7:0)
rd_setup_reg1 : (7:0)
wr_comp_dly : (7:0)
rd_comp_dly : (7:0)
wr_setup_reg3 : (7:0)
rd_setup_reg3 : (7:0)
rd_stat_regs : (7:0)
vme_rd_spy : (7:0)
rd_phase_cnta : (7:0)
rd_phase_cntb : (7:0)
stat_reg0(3:0) from ROP
stat_reg0(3:0) : (15:0)
eb44
stat_reg0(15 downto 11) <= unused(4 downto 0);
stat_reg0(10 downto 5) <= (others=>'0');
stat_reg0(4) <= bc_error;
C =PSB9U_V2
8 =PSB9U
eb33
chip_idh <=X"0001";
chip_id <=X"C131";
chip_version <=X"0004";
eb22
stat_reg5 <= (others=>'0');
stat_reg6 <= (others=>'0');
stat_reg7 <= (others=>'0');
Chip_id = PSB(8)+cardnr(1)+PSBchip(3)+chipnr(1)
vdin : (15:0)
phase_cnta0 : (15:0)
phase_cnta1 : (15:0)
phase_cnta2 : (15:0)
phase_cnta3 : (15:0)
phase_cnta4 : (15:0)
phase_cnta5 : (15:0)
phase_cnta6 : (15:0)
phase_cnta7 : (15:0)
phase_cntb0 : (15:0)
phase_cntb1 : (15:0)
phase_cntb2 : (15:0)
phase_cntb3 : (15:0)
phase_cntb4 : (15:0)
phase_cntb5 : (15:0)
phase_cntb6 : (15:0)
phase_cntb7 : (15:0)
stat_reg0 : (15:0)
rop_status : (15:0)
chip_id : (15:0)
chip_version : (15:0)
chip_idh : (15:0)
stat_reg5 : (15:0)
stat_reg6 : (15:0)
stat_reg7 : (15:0)
vdout_ch0 : (15:0)
vdout_ch1 : (15:0)
vdout_ch2 : (15:0)
vdout_ch3 : (15:0)
vdout_ch4 : (15:0)
vdout_ch5 : (15:0)
stop_spying : (15:0)
refmem_contin_mode
chan_reg0 : (15:0)
chan_reg1 : (15:0)
chan_reg2 : (15:0)
chan_reg3 : (15:0)
chan_reg4 : (15:0)
chan_reg5 : (15:0)
chan_reg6 : (15:0)
chan_reg7 : (15:0)
chan_delay0 : (15:0)
chan_delay1 : (15:0)
chan_delay2 : (15:0)
chan_delay3 : (15:0)
chan_delay4 : (15:0)
chan_delay5 : (15:0)
chan_delay6 : (15:0)
chan_delay7 : (15:0)
board_id : (15:0)
idle_identifier : (31:0)
bcres_delay : (15:0)
latency_delay : (15:0)
rop_setup : (15:0)
max_bc_nr : (15:0)
sel_phase3100 : (15:0)
sel_phase6332 : (15:0)
run_next_orbit_refmem
stop_rop_vme
start_rop_vme
res_bc_error
ResEvnr_vme
ResOrbnr_vme
BCRes_vme
L1Res_vme
run_next_orbit : (7:0)
vdout : (15:0)
lvds_delay0 : (15:0)
lvds_delay1 : (15:0)
lvds_delay2 : (15:0)
lvds_delay3 : (15:0)
lvds_delay4 : (15:0)
lvds_delay5 : (15:0)
lvds_delay6 : (15:0)
lvds_delay7 : (15:0)
lvds_delay8 : (15:0)
lvds_delay9 : (15:0)

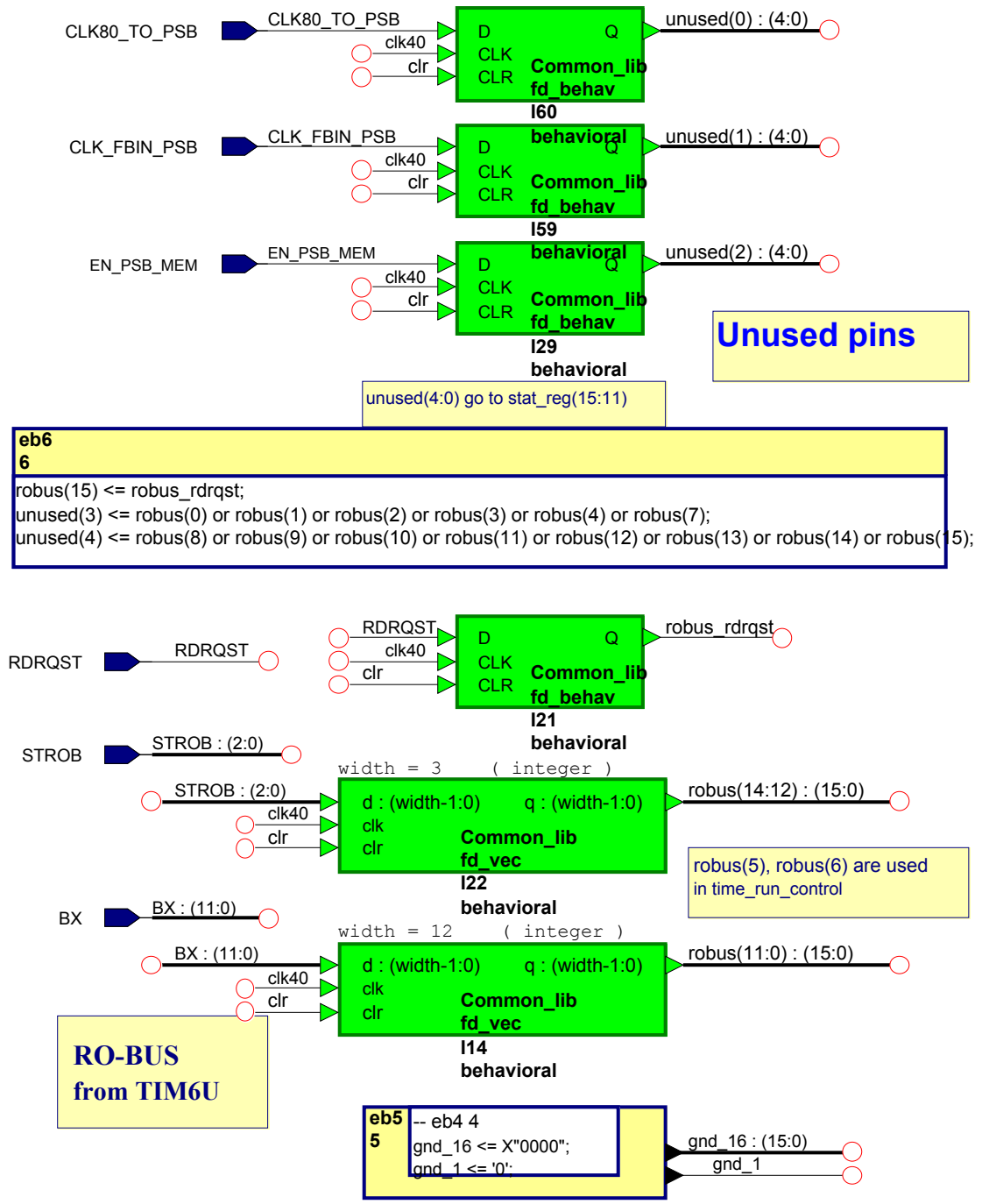
PSB channels 1 & 0 +LVDS

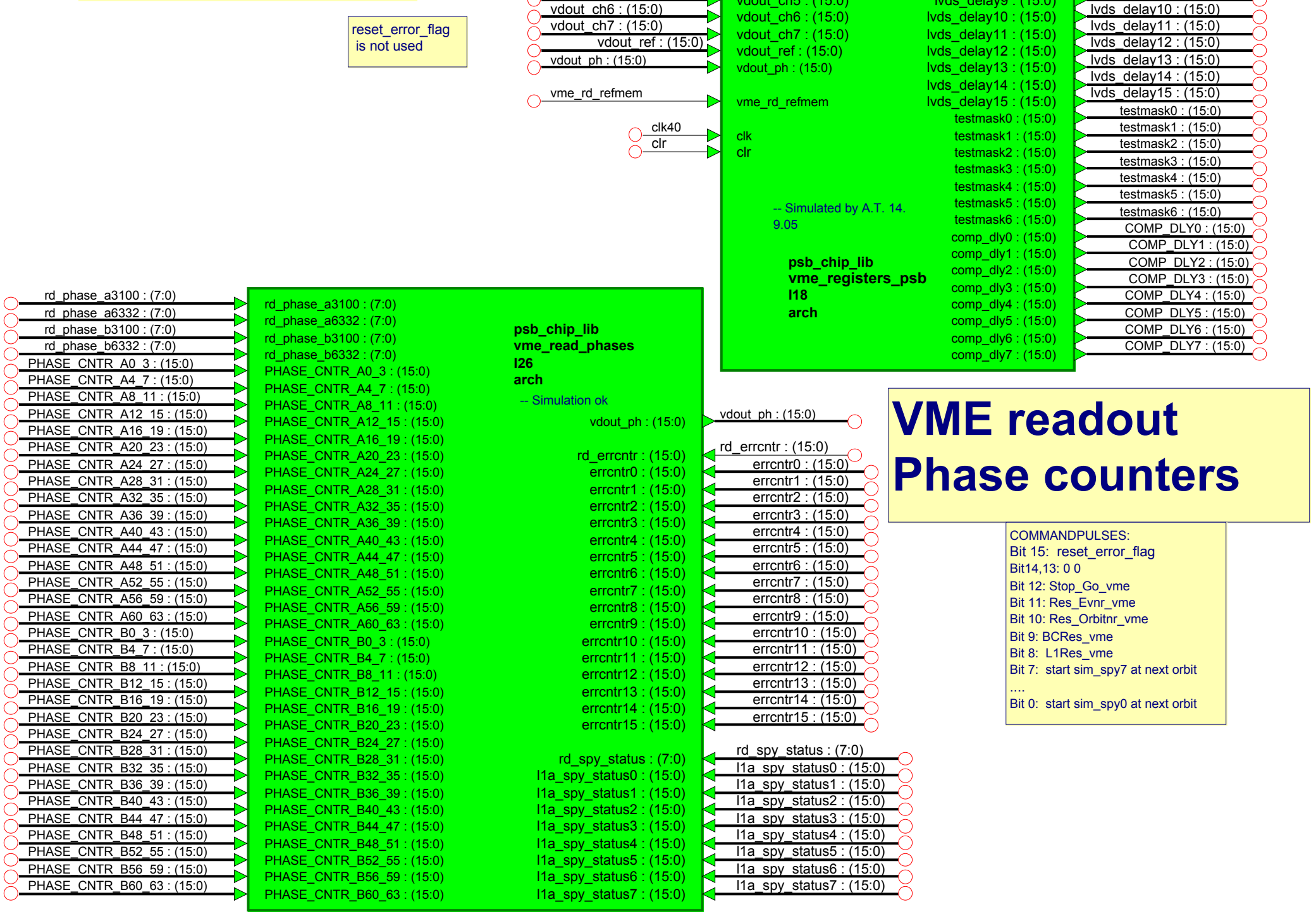


PSB channels 2 & 3



```
SIGNAL chan_delay2              : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay3              : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay4              : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay5              : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay6              : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_delay7              : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg0                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg1                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg2                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg3                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg4                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg5                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg6                : std_logic_vector(15 DOWNTO 0)
SIGNAL chan_reg7                : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_id                  : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_idh                 : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_version             : std_logic_vector(15 DOWNTO 0)
SIGNAL chout0                   : std_logic_vector(15 DOWNTO 0)
SIGNAL chout1                   : std_logic_vector(15 DOWNTO 0)
SIGNAL chout2                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL chout3                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL chout4                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL chout5                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL chout6                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL chout7                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL clk160                   : STD_ULOGIC
SIGNAL clk40                    : std_logic
SIGNAL clk80                    : std_logic
SIGNAL clk_locked               : std_logic
SIGNAL clr                      : std_logic
SIGNAL daq_data                 : std_logic_vector(27 DOWNTO 0)
SIGNAL dtack                    : std_logic
SIGNAL en_compp                 : std_logic
SIGNAL en_vdoo                  : std_logic
SIGNAL errcntr0                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr1                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr10                : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr11                : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr12                : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr13                : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr14                : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr15                : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr2                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr3                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr4                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr5                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr6                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr7                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr8                 : std_logic_vector(15 DOWNTO 0)
SIGNAL errcntr9                 : std_logic_vector(15 DOWNTO 0)
SIGNAL gnd_1                    : std_logic
SIGNAL gnd_16                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL ground                   : std_logic
SIGNAL gsr                      : STD_ULOGIC
SIGNAL gts                      : STD_ULOGIC
SIGNAL idle_identifier          : std_logic_vector(31 DOWNTO 0)
SIGNAL inc_lvd0sph              : std_logic_VECTOR(3 DOWNTO 0)
SIGNAL inc_phas4                : std_logic_vector(3 DOWNTO 0)
SIGNAL l1a2spy                  : std_logic
SIGNAL l1a_spy_status0          : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_spy_status1          : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_spy_status2          : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_spy_status3          : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_spy_status4          : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_spy_status5          : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL l1a_spy_status6          : std_logic_vector(15 DOWNTO 0)
SIGNAL l1a_spy_status7          : std_logic_vector(15 DOWNTO 0)
SIGNAL latency_delay            : std_logic_vector(15 DOWNTO 0)
SIGNAL lvds80_data              : std_logic_VECTOR(31 DOWNTO 0)
SIGNAL lvds_delay0              : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay1              : std_logic_VECTOR(15 DOWNTO 0)
```

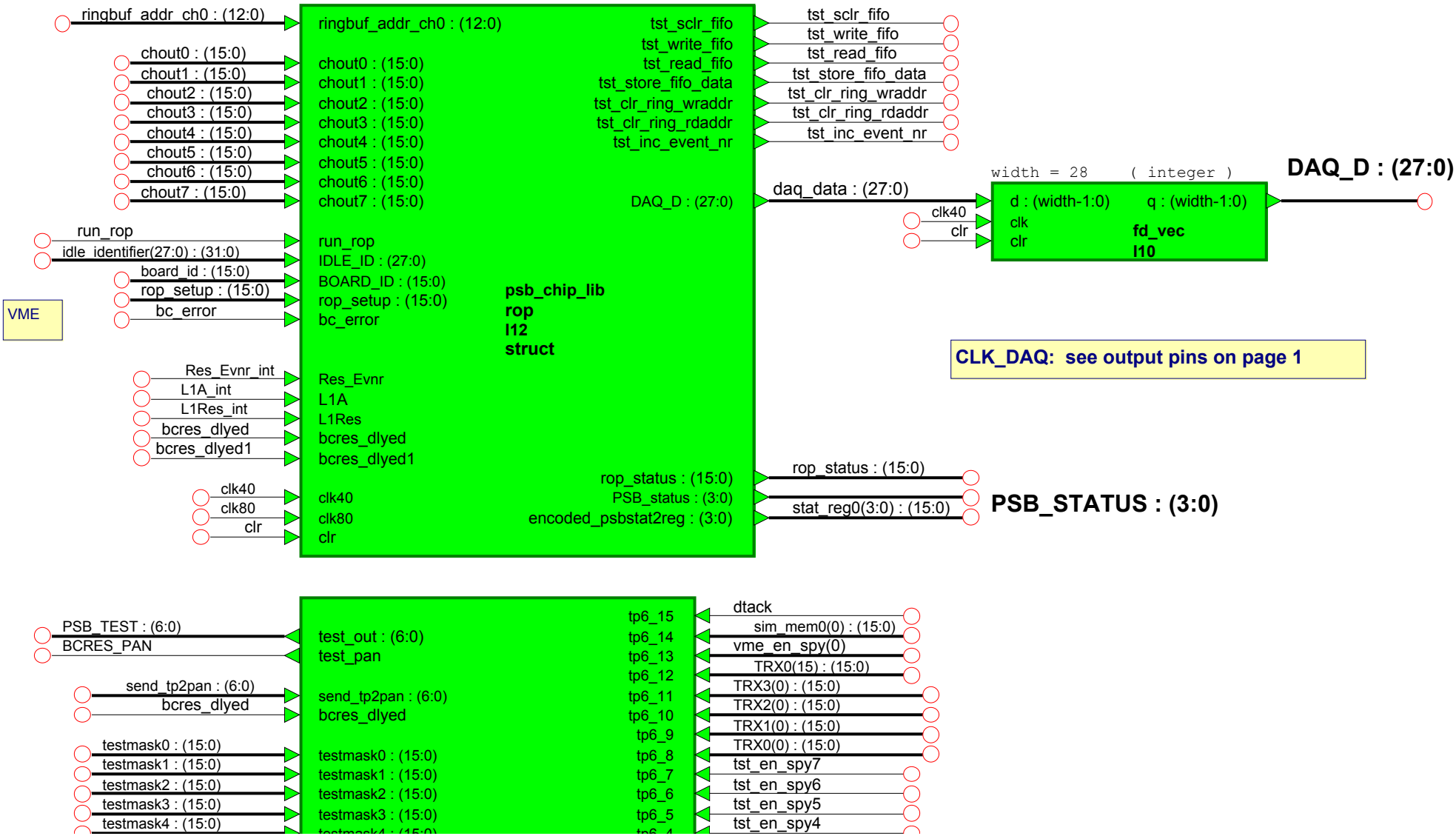



reset_error_flag
is not used
vdout_ch6 : (15:0)
vdout_ch7 : (15:0)
vdout_ref : (15:0)
vdout_ph : (15:0)
vme_rd_refmem
clk40
clr
-- Simulated by A.T. 14.9.05
psb_chip_lib
vme_registers_psb
l18
arch
lvds_delay10 : (15:0)
lvds_delay11 : (15:0)
lvds_delay12 : (15:0)
lvds_delay13 : (15:0)
lvds_delay14 : (15:0)
lvds_delay15 : (15:0)
testmask0 : (15:0)
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
testmask4 : (15:0)
testmask5 : (15:0)
testmask6 : (15:0)
COMP_DLY0 : (15:0)
COMP_DLY1 : (15:0)
COMP_DLY2 : (15:0)
COMP_DLY3 : (15:0)
COMP_DLY4 : (15:0)
COMP_DLY5 : (15:0)
COMP_DLY6 : (15:0)
COMP_DLY7 : (15:0)
rd_phase_a3100 : (7:0)
rd_phase_a6332 : (7:0)
rd_phase_b3100 : (7:0)
rd_phase_b6332 : (7:0)
PHASE_CNTR_A0_3 : (15:0)
PHASE_CNTR_A4_7 : (15:0)
PHASE_CNTR_A8_11 : (15:0)
PHASE_CNTR_A12_15 : (15:0)
PHASE_CNTR_A16_19 : (15:0)
PHASE_CNTR_A20_23 : (15:0)
PHASE_CNTR_A24_27 : (15:0)
PHASE_CNTR_A28_31 : (15:0)
PHASE_CNTR_A32_35 : (15:0)
PHASE_CNTR_A36_39 : (15:0)
PHASE_CNTR_A40_43 : (15:0)
PHASE_CNTR_A44_47 : (15:0)
PHASE_CNTR_A48_51 : (15:0)
PHASE_CNTR_A52_55 : (15:0)
PHASE_CNTR_A56_59 : (15:0)
PHASE_CNTR_A60_63 : (15:0)
PHASE_CNTR_B0_3 : (15:0)
PHASE_CNTR_B4_7 : (15:0)
PHASE_CNTR_B8_11 : (15:0)
PHASE_CNTR_B12_15 : (15:0)
PHASE_CNTR_B16_19 : (15:0)
PHASE_CNTR_B20_23 : (15:0)
PHASE_CNTR_B24_27 : (15:0)
PHASE_CNTR_B28_31 : (15:0)
PHASE_CNTR_B32_35 : (15:0)
PHASE_CNTR_B36_39 : (15:0)
PHASE_CNTR_B40_43 : (15:0)
PHASE_CNTR_B44_47 : (15:0)
PHASE_CNTR_B48_51 : (15:0)
PHASE_CNTR_B52_55 : (15:0)
PHASE_CNTR_B56_59 : (15:0)
PHASE_CNTR_B60_63 : (15:0)
psb_chip_lib
vme_read_phases
l26
arch
-- Simulation ok
vdout_ph : (15:0)
rd_errcntr : (15:0)
errcntr0 : (15:0)
errcntr1 : (15:0)
errcntr2 : (15:0)
errcntr3 : (15:0)
errcntr4 : (15:0)
errcntr5 : (15:0)
errcntr6 : (15:0)
errcntr7 : (15:0)
errcntr8 : (15:0)
errcntr9 : (15:0)
errcntr10 : (15:0)
errcntr11 : (15:0)
errcntr12 : (15:0)
errcntr13 : (15:0)
errcntr14 : (15:0)
errcntr15 : (15:0)
rd_spy_status : (7:0)
l1a_spy_status0 : (15:0)
l1a_spy_status1 : (15:0)
l1a_spy_status2 : (15:0)
l1a_spy_status3 : (15:0)
l1a_spy_status4 : (15:0)
l1a_spy_status5 : (15:0)
l1a_spy_status6 : (15:0)
l1a_spy_status7 : (15:0)
VME readout
Phase counters
COMMANDPULSES:
Bit 15: reset_error_flag
Bit14,13: 0 0
Bit 12: Stop_Go_vme
Bit 11: Res_Evnr_vme
Bit 10: Res_Orbitnr_vme
Bit 9: BCRes_vme
Bit 8: L1Res_vme
Bit 7: start sim_spy7 at next orbit
....
Bit 0: start sim_spy0 at next orbit

ROP

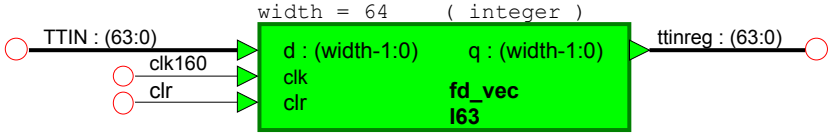
40MHz data to Channel Link

ringbuf_addr for debugging only

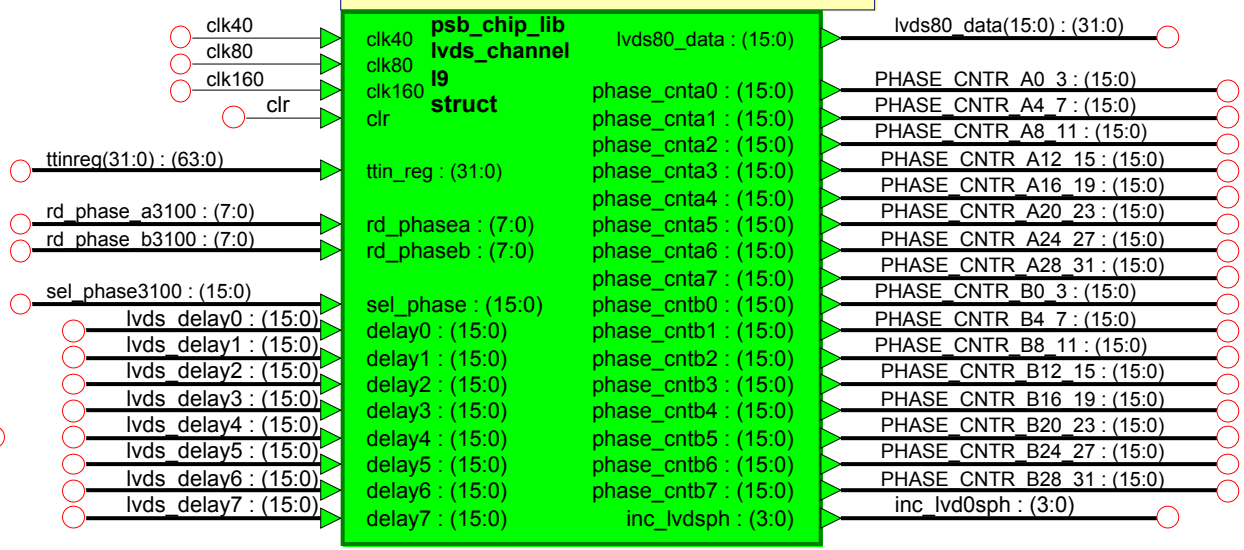


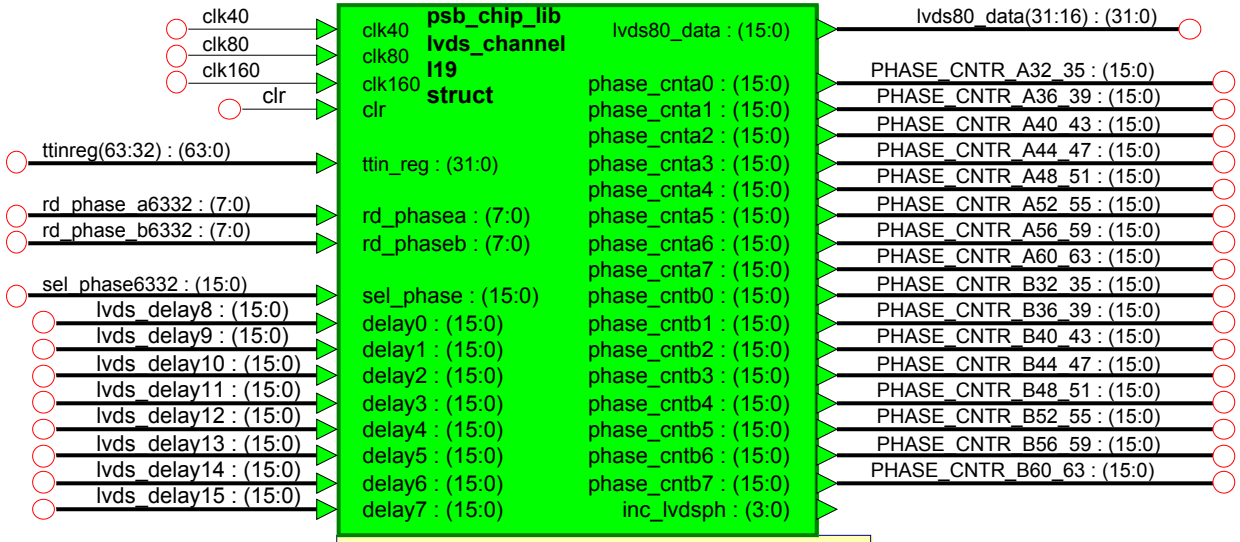
LVDS Channels for Totem

Add 160MHz register to use same clk for
both IOpins of a LVDS pair, where TTIN and REC
signals occupy pins of same IO-pair



multiplex with channel0





multiplex with channel 1

64 LVDS input bits

INTERLACING:
64 LVDS bits ==> 1 Quadruplet
(TTIN bits 15-00) are sent before (TTIN bits 31-16) like Calo_Obj1 before Obj3
(TTIN bits 47-32) are sent before (TTIN bits 63-48) like Calo_Obj2 before Obj4

64 LVDS bits:
Oversampling 4x per 25ns
interlace 2 40MHz-data streams
SIMSPY mem and Ringbuffer as for Calo data.

```
SIGNAL lvds_delay10            : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay11            : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay12            : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay13            : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay14            : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay15            : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay2             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay3             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay4             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay5             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay6             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay7             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay8             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL lvds_delay9             : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL max_bc_nr               : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout0                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout1                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout2                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout3                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout4                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout5                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout6                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nchout7                 : std_logic_vector(15 DOWNTO 0)
SIGNAL nclk160                 : STD_ULOGIC
SIGNAL nclk80                  : std_logic
SIGNAL phase_cnta0             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cnta1             : std_logic_vector(15 downto 0)
SIGNAL phase_cnta2             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cnta3             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cnta4             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cnta5             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cnta6             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cnta7             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cntb0             : std_logic_vector(15 downto 0)
SIGNAL phase_cntb1             : std_logic_vector(15 downto 0)
SIGNAL phase_cntb2             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cntb3             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cntb4             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cntb5             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cntb6             : std_logic_vector(15 DOWNTO 0)
SIGNAL phase_cntb7             : std_logic_vector(15 DOWNTO 0)
SIGNAL rd_chan_delay           : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_chan_reg             : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_comp_dly             : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_errcntr              : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL rd_lvds_delay           : std_logic_vector(15 DOWNTO 0)
SIGNAL rd_phase_a3100          : std_logic_VECTOR(7 DOWNTO 0)
SIGNAL rd_phase_a6332          : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_phase_b3100          : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_phase_b6332          : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_phase_cnta           : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_phase_cntb           : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_setup_reg            : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_setup_reg1           : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_setup_reg3           : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_spy_status           : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_stat_regs            : std_logic_vector(7 DOWNTO 0)
SIGNAL refmem_contin_mode      : std_logic
SIGNAL res_bc_error            : std_logic
SIGNAL ringbuf_addr_ch0        : std_logic_VECTOR(12 DOWNTO 0)
SIGNAL robus                   : std_logic_vector(15 DOWNTO 0)
SIGNAL robus_rdrqst            : std_logic
SIGNAL rop_setup               : std_logic_vector(15 DOWNTO 0)
SIGNAL rop_status              : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL rst_dcm                 : std_logic
SIGNAL run_next_orbit          : std_logic_vector(7 DOWNTO 0)
SIGNAL run_next_orbit_refmem   : std_logic
SIGNAL run_rop                 : std_logic
SIGNAL sel_phase3100           : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL sel_phase6332           : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL send_tp2pan             : std_logic_vector(6 DOWNTO 0)
SIGNAL sim_addr0               : std_logic_VECTOR(12 DOWNTO 0)
```

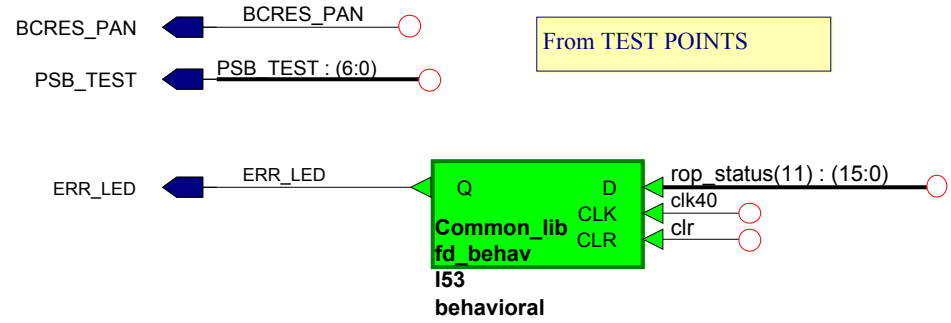
Positions on PSB9U board

CH7 TTCIN(63) <= TTCIN15_3
CH6
CH5
CH4
CH3
CH2
CH1
CH0 TTCIN(0)<=TTCIN0_0

TTCIN63-32 sent as CH3 data
TTCIN31-00 sent as CH2 data
to be sent as CA10 channel
from the PSB3 to the GTL board

OFD for various signals

Front Panel



bit11=ROP_ERROR
not all FIFOs empty, FIFO is/are full

TEST POINTS of PSB chip_v2 V0001

V2_V0001: clk80 removed, bc0_data added, bc0_data_ch4 removed

rop_setup(14:8) : (15:0) → **eb1 1** send_tp2pan(6 downto 0) <= rop_setup(14 downto 8); → send_tp2pan : (6:0)

TESTPOINT 0	TESTPOINT 1	TESTPOINT 2	TESTPOINT 3	TESTPOINT 4	TESTPOINT 5	TESTPOINT 6
clk40	gnd_1	vme_wr	clr	gnd_1	vme_en	dtack
BCRes_int	bc_error	bcres_dlyed	bcres_dlyed1	gnd_1	tst_we_spy0	sim_mem0(0) : (15:0)
Res_Evnr_int	Res_Orbitnr_int	L1Res_int	run_rop	gnd_1	vme_we_spy(0)	vme_en_spy(0)
run_next_orbit(0)	rd_chan_reg(0)	wr_chan_reg(0)	chout5(15) : (15:0)	gnd_1	chout4(15) : (15:0)	TRX0(15) : (15:0)
L1Res_vme	gnd_1	L1A_int	L1A_int	gnd_1	BCRes_vme	TRX3(0) : (15:0)
PSB_STATUS(0)	PSB_STATUS(1)	PSB_STATUS(2)	PSB_STATUS(3)	gnd_1	run_next_orbit_refmem	TRX2(0) : (15:0)
start_rop_vme	stop_rop_vme	vme_rd_spy(0)	ResEvnr_vme	gnd_1	res_bc_error	TRX1(0) : (15:0)
daq_data(24)	daq_data(25)	daq_data(26)	daq_data(27)	gnd_1	run_next_orbit(4)	TRX0(0) : (15:0)
tst_write_fifo	tst_read_fifo	tst_store_fifo_data	tst_sclr_fifo	bc0_data(7) : (7:0)	chout7(0) : (15:0)	tst_en_spy7
tst_clr_ring_rdaddr	tst_clr_ring_wraddr	en_compp	tst_inc_event_nr	bc0_data(6) : (7:0)	chout6(0) : (15:0)	tst_en_spy6
sim_addr1(0)	sim_addr1(1)	sim_addr1(2)	sim_addr1(3)	bc0_data(5) : (7:0)	chout5(0) : (15:0)	tst_en_spy5
sim_addr0(0)	sim_addr0(1)	sim_addr0(2)	sim_addr0(3)	bc0_data(4) : (7:0)	chout4(0) : (15:0)	tst_en_spy4
vdout_ch1(0)	vdout_ch1(1)	vdout_ch1(2)	vdout_ch1(3)	bc0_data(3) : (7:0)	chout3(0) : (15:0)	tst_en_spy3
inc_phas4(0)	inc_phas4(1)	inc_phas4(2)	inc_phas4(3)	bc0_data(2) : (7:0)	chout2(0) : (15:0)	tst_en_spy2
inc_lvd0sph(0)	inc_lvd0sph(1)	inc_lvd0sph(2)	inc_lvd0sph(3)	bc0_data(1) : (7:0)	chout1(0) : (15:0)	tst_en_spy1
stat_reg0(0)	stat_reg0(1)	stat_reg0(2)	stat_reg0(3)	bc0_data(0) : (7:0)	chout0(0) : (15:0)	tst_en_spy0

bit 15 · bit 11 · bit 7 · bit 0

MASK bits

testmask0 : (15:0)
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
testmask4 : (15:0)
testmask5 : (15:0)
testmask6 : (15:0)

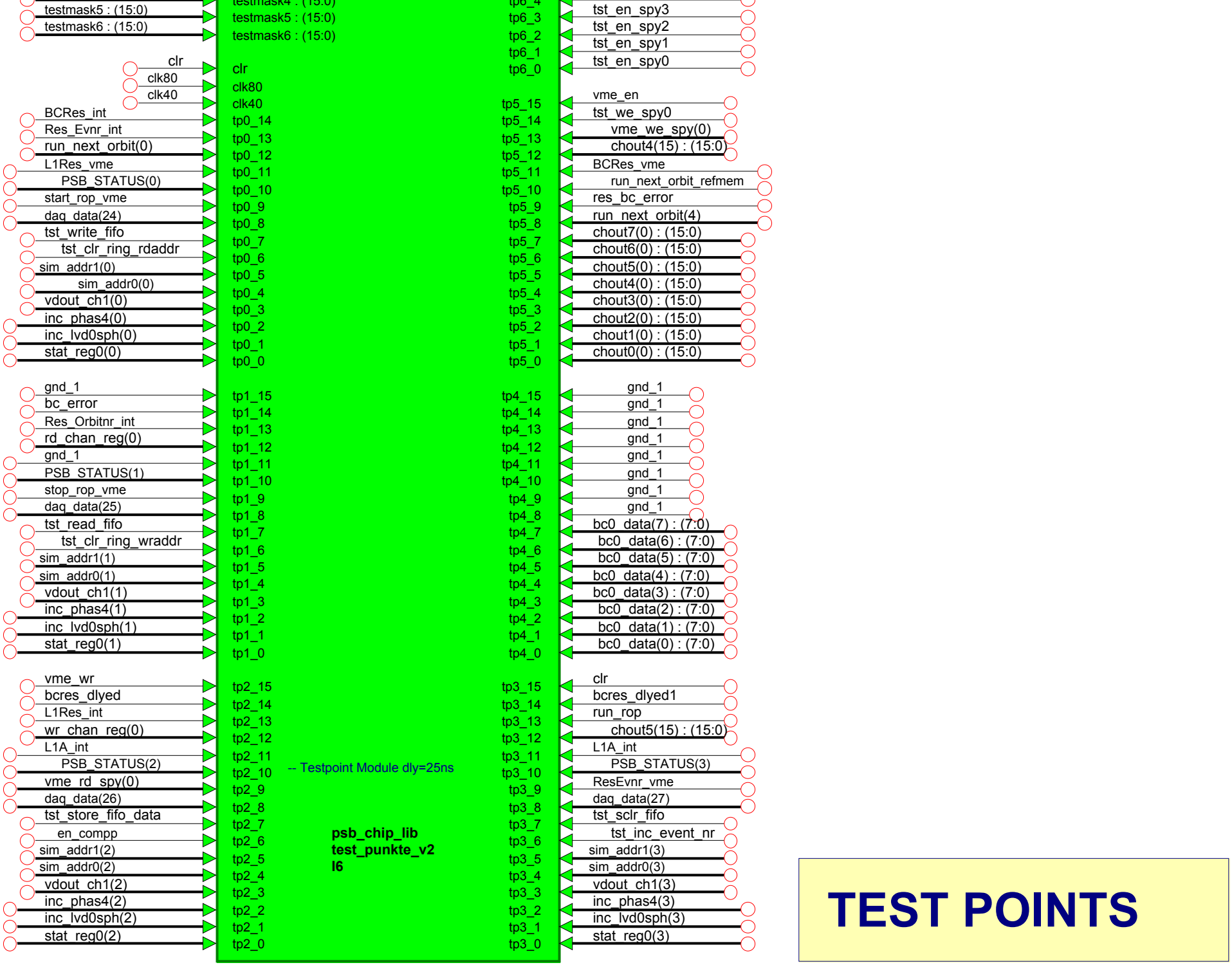
PSB_TEST : (6:0)

output to test point pins

stat_reg0(4) = bc_error (testpoint1:14)
stat_reg0(3) = ready
stat_reg0(2) = busy
stat_reg0(1) = out_of_Sync
stat_reg0(0) = warning

```
rop_status(15) <=  roc_is_idle;
rop_status(14) <=   run_rop;   --run flag
rop_status(13) <=   '0';
rop_status(12) <=   out_of_sync;
rop_status(11) <=   error;
rop_status(10) <=   warning;
rop_status(9) <=  full_fifo;
rop_status(8 downto 0) <= empty(8 downto 0)
```

send_tp2pan connects a TESTPOINT to the FrontPanel Lemo
send_tp2pan ="000 0000" ==> bcres_dlyed goes to Frontpanel

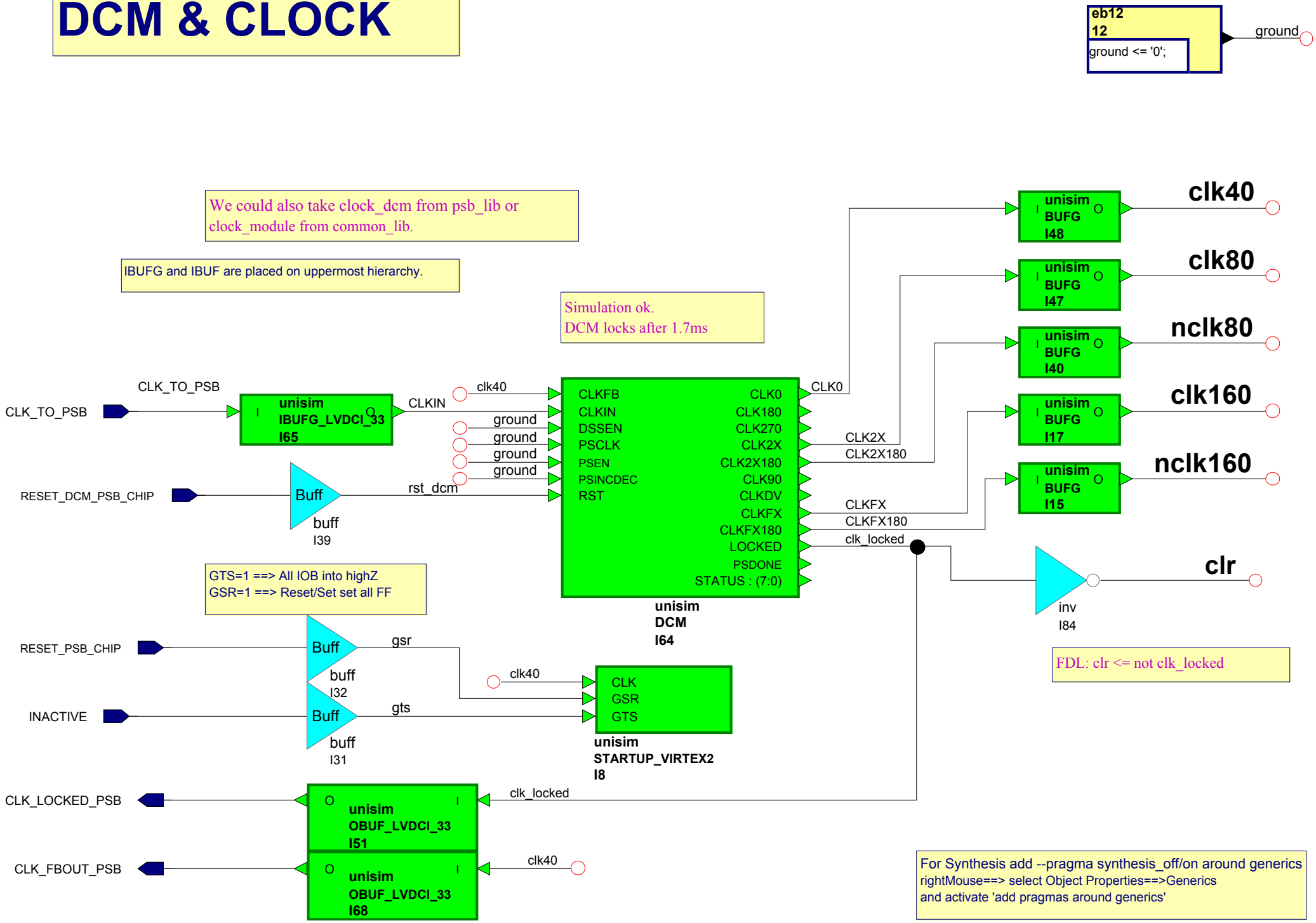

testmask5 : (15:0)
testmask6 : (15:0)
clr
clk80
clk40
BCRes_int
Res_Evnr_int
run_next_orbit(0)
L1Res_vme
PSB_STATUS(0)
start_rop_vme
daq_data(24)
tst_write_fifo
tst_clr_ring_rdaddr
sim_addr1(0)
sim_addr0(0)
vdout_ch1(0)
inc_phas4(0)
inc_lvd0sph(0)
stat_reg0(0)
gnd_1
bc_error
Res_Orbitnr_int
rd_chan_reg(0)
gnd_1
PSB_STATUS(1)
stop_rop_vme
daq_data(25)
tst_read_fifo
tst_clr_ring_wraddr
sim_addr1(1)
sim_addr0(1)
vdout_ch1(1)
inc_phas4(1)
inc_lvd0sph(1)
stat_reg0(1)
vme_wr
bcres_dlyed
L1Res_int
wr_chan_reg(0)
L1A_int
PSB_STATUS(2)
vme_rd_spy(0)
daq_data(26)
tst_store_fifo_data
en_compp
sim_addr1(2)
sim_addr0(2)
vdout_ch1(2)
inc_phas4(2)
inc_lvd0sph(2)
stat_reg0(2)
tp0_14 tp0_13 tp0_12 tp0_11 tp0_10 tp0_9 tp0_8 tp0_7 tp0_6 tp0_5 tp0_4 tp0_3 tp0_2 tp0_1 tp0_0
tp1_15 tp1_14 tp1_13 tp1_12 tp1_11 tp1_10 tp1_9 tp1_8 tp1_7 tp1_6 tp1_5 tp1_4 tp1_3 tp1_2 tp1_1 tp1_0
tp2_15 tp2_14 tp2_13 tp2_12 tp2_11 tp2_10 tp2_9 tp2_8 tp2_7 tp2_6 tp2_5 tp2_4 tp2_3 tp2_2 tp2_1 tp2_0
-- Testpoint Module dly=25ns
psb_chip_lib
test_punkte_v2
I6
tp6_4 tp6_3 tp6_2 tp6_1 tp6_0
tp5_15 tp5_14 tp5_13 tp5_12 tp5_11 tp5_10 tp5_9 tp5_8 tp5_7 tp5_6 tp5_5 tp5_4 tp5_3 tp5_2 tp5_1 tp5_0
tp4_15 tp4_14 tp4_13 tp4_12 tp4_11 tp4_10 tp4_9 tp4_8 tp4_7 tp4_6 tp4_5 tp4_4 tp4_3 tp4_2 tp4_1 tp4_0
tp3_15 tp3_14 tp3_13 tp3_12 tp3_11 tp3_10 tp3_9 tp3_8 tp3_7 tp3_6 tp3_5 tp3_4 tp3_3 tp3_2 tp3_1 tp3_0
tst_en_spy3
tst_en_spy2
tst_en_spy1
tst_en_spy0
vme_en
tst_we_spy0
vme_we_spy(0)
chout4(15) : (15:0)
BCRes_vme
run_next_orbit_refmem
res_bc_error
run_next_orbit(4)
chout7(0) : (15:0)
chout6(0) : (15:0)
chout5(0) : (15:0)
chout4(0) : (15:0)
chout3(0) : (15:0)
chout2(0) : (15:0)
chout1(0) : (15:0)
chout0(0) : (15:0)
gnd_1
gnd_1
gnd_1
gnd_1
gnd_1
gnd_1
gnd_1
gnd_1
bc0_data(7) : (7:0)
bc0_data(6) : (7:0)
bc0_data(5) : (7:0)
bc0_data(4) : (7:0)
bc0_data(3) : (7:0)
bc0_data(2) : (7:0)
bc0_data(1) : (7:0)
bc0_data(0) : (7:0)
clr
bcres_dlyed1
run_rop
chout5(15) : (15:0)
L1A_int
PSB_STATUS(3)
ResEvnr_vme
daq_data(27)
tst_sclr_fifo
tst_inc_event_nr
sim_addr1(3)
sim_addr0(3)
vdout_ch1(3)
inc_phas4(3)
inc_lvd0sph(3)
stat_reg0(3)

TEST POINTS

Compare transmitted with received data

```
SIGNAL sim_addr0              : std_logic_VECTOR(12 DOWNTO 0)
SIGNAL sim_addr1              : std_logic_VECTOR(12 DOWNTO 0)
SIGNAL sim_mem0               : std_logic_vector(15 DOWNTO 0)
SIGNAL start_rop_vme          : std_logic
SIGNAL stat_reg0              : std_logic_vector(15 DOWNTO 0)
SIGNAL stat_reg5              : std_logic_vector(15 downto 0)
SIGNAL stat_reg6              : std_logic_vector(15 downto 0)
SIGNAL stat_reg7              : std_logic_vector(15 DOWNTO 0)
SIGNAL stop_rop_vme           : std_logic
SIGNAL stop_spying            : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask0              : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask1              : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask2              : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask3              : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask4              : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask5              : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask6              : std_logic_vector(15 DOWNTO 0)
SIGNAL tst_clr_ring_rdaddr    : std_logic
SIGNAL tst_clr_ring_wraddr    : std_logic
SIGNAL tst_en_spy0            : std_logic
SIGNAL tst_en_spy1            : std_logic
SIGNAL tst_en_spy2            : std_logic
SIGNAL tst_en_spy3            : std_logic
SIGNAL tst_en_spy4            : std_logic
SIGNAL tst_en_spy5            : std_logic
SIGNAL tst_en_spy6            : std_logic
SIGNAL tst_en_spy7            : std_logic
SIGNAL tst_inc_event_nr       : std_logic
SIGNAL tst_read_fifo          : std_logic
SIGNAL tst_sclr_fifo          : std_logic
SIGNAL tst_store_fifo_data    : std_logic
SIGNAL tst_we_spy0            : std_logic
SIGNAL tst_write_fifo         : std_logic
SIGNAL ttinreg                : std_logic_VECTOR(63 DOWNTO 0)
SIGNAL unused                 : std_logic_vector(4 DOWNTO 0)
SIGNAL vdii                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vdin                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vdoo                   : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vdout                  : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch0              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch1              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch2              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch3              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch4              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch5              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch6              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ch7              : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ph               : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_ref              : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL vme_addr               : std_logic_VECTOR(19 DOWNTO 1)
SIGNAL vme_dis_rd             : std_logic
SIGNAL vme_en                 : std_logic
SIGNAL vme_en_refmem          : std_logic
SIGNAL vme_en_spy             : std_logic_vector(7 DOWNTO 0)
SIGNAL vme_enn                : std_logic
SIGNAL vme_rd_refmem          : std_logic
SIGNAL vme_rd_spy             : std_logic_vector(7 DOWNTO 0)
SIGNAL vme_we_refmem          : std_logic
SIGNAL vme_we_spy             : std_logic_vector(7 DOWNTO 0)
SIGNAL vme_wr                 : std_logic
SIGNAL wr_chan_delay          : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_chan_reg            : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_comp_dly            : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_lvds_delay          : std_logic_vector(15 DOWNTO 0)
SIGNAL wr_setup_reg           : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_setup_reg1          : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_setup_reg3          : std_logic_VECTOR(7 DOWNTO 0)
```

DCM & CLOCK


eb12
12
ground <= '0';
ground
We could also take clock_dcm from psb_lib or clock_module from common_lib.
IBUFG and IBUF are placed on uppermost hierarchy.
Simulation ok.
DCM locks after 1.7ms
CLK_TO_PSB
CLK_TO_PSB
unisim
IBUFG_LVDCI_33
I65
CLKIN
clk40
ground
ground
ground
ground
RESET_DCM_PSB_CHIP
Buff
buff
I39
rst_dcm
CLKFB
CLKIN
DSSEN
PSCLK
PSEN
PSINCDEC
RST
CLK0
CLK180
CLK270
CLK2X
CLK2X180
CLK90
CLKDV
CLKFX
CLKFX180
LOCKED
PSDONE
STATUS : (7:0)
unisim
DCM
I64
CLK0
CLK2X
CLK2X180
CLKFX
CLKFX180
clk_locked
unisim
BUFG
I48
clk40
unisim
BUFG
I47
clk80
unisim
BUFG
I40
nclk80
unisim
BUFG
I17
clk160
unisim
BUFG
I15
nclk160
inv
I84
clr
FDL: clr <= not clk_locked
GTS=1 ==> All IOB into highZ
GSR=1 ==> Reset/Set set all FF
RESET_PSB_CHIP
Buff
buff
I32
gsr
INACTIVE
Buff
buff
I31
gts
clk40
CLK
GSR
GTS
unisim
STARTUP_VIRTEX2
I8
CLK_LOCKED_PSB
unisim
OBUF_LVDCI_33
I51
clk_locked
CLK_FBOUT_PSB
unisim
OBUF_LVDCI_33
I68
clk40
For Synthesis add --pragma synthesis_off/on around generics
rightMouse==> select Object Properties==>Generics
and activate 'add pragmas around generics'

```
TimingChecksOn                          = true                  ( boolean          )
InstancePath                            = "*"                   ( string           )
Xon                                     = true                  ( boolean          )
MsgOn                                   = false                 ( boolean          )
thold_PSEN_PSCLK_negedge_posedge        = 0.000 ns              ( VitalDelayType   )
thold_PSEN_PSCLK_posedge_posedge        = 0.000 ns              ( VitalDelayType   )
thold_PSINCDEC_PSCLK_negedge_posedge    = 0.000 ns              ( VitalDelayType   )
thold_PSINCDEC_PSCLK_posedge_posedge    = 0.000 ns              ( VitalDelayType   )
tipd_CLKFB                              = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_CLKIN                              = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_DSSEN                              = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_PSCLK                              = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_PSEN                               = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_PSINCDEC                           = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_RST                                = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tpd_CLKIN_LOCKED                        = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tpd_PSCLK_PSDONE                        = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tperiod_CLKIN_POSEDGE                   = 0.000 ns              ( VitalDelayType   )
tperiod_PSCLK_POSEDGE                   = 0.000 ns              ( VitalDelayType   )
tpw_CLKIN_negedge                       = 0.000 ns              ( VitalDelayType   )
tpw_CLKIN_posedge                       = 0.000 ns              ( VitalDelayType   )
tpw_PSCLK_negedge                       = 0.000 ns              ( VitalDelayType   )
tpw_PSCLK_posedge                       = 0.000 ns              ( VitalDelayType   )
tpw_RST_posedge                         = 0.000 ns              ( VitalDelayType   )
tsetup_PSEN_PSCLK_negedge_posedge       = 0.000 ns              ( VitalDelayType   )
tsetup_PSEN_PSCLK_posedge_posedge       = 0.000 ns              ( VitalDelayType   )
tsetup_PSINCDEC_PSCLK_negedge_posedge   = 0.000 ns              ( VitalDelayType   )
tsetup_PSINCDEC_PSCLK_posedge_posedge   = 0.000 ns              ( VitalDelayType   )
CLKDV_DIVIDE                            = 2.0                   ( real             )
CLKFX_DIVIDE                            = 1                     ( integer          )
CLKFX_MULTIPLY                          = 4                     ( integer          )
CLKIN_DIVIDE_BY_2                       = false                 ( boolean          )
CLKIN_PERIOD                            = 24.0                  ( real             )
CLKOUT_PHASE_SHIFT                      = "NONE"                ( string           )
CLK_FEEDBACK                            = "1X"                  ( string           )
DESKEW_ADJUST                           = "SYSTEM_SYNCHRONOUS"  ( string           )
DFS_FREQUENCY_MODE                      = "LOW"                 ( string           )
DLL_FREQUENCY_MODE                      = "LOW"                 ( string           )
DSS_MODE                                = "NONE"                ( string           )
DUTY_CYCLE_CORRECTION                   = true                  ( boolean          )
FACTORY_JF                              = X"C080"               ( bit_vector       )
MAXPERCLKIN                             = 1000000 ps            ( time             )
MAXPERPSCLK                             = 100000000 ps          ( time             )
PHASE_SHIFT                             = 0                     ( integer          )
SIM_CLKIN_CYCLE_JITTER                  = 300 ps                ( time             )
SIM_CLKIN_PERIOD_JITTER                 = 1000 ps               ( time             )
STARTUP_WAIT                            = false                 ( boolean          )
```

PSB_chip: for board PSB9U....(first version)
V0001: psb_chip_struct\psb_chip_impl_6 // 4 phases
V0002: psb_chip_struct\psb_chip_impl_7 // 2 phases
V0003: without GTLp outputs
V0004: 2 phases with inverted GTLP_DCI outputs
V0005 :2 phases with inverted GTLP outputs ==> less power
V0006 : 2 phases, inverted GTLP, TRx as LVDCI_DV2_33
V0007 : 2 phases, inverted GTLP, TRx as LVDCI_DV2_33, new testpoint
SIM/SPY RAM with 'read first'
V0008: as V0007 but with behavioral address counters for sim/spy mem's.
V0009: as V0008, new testpoints, with new...6Sept05.ucf file
V0010: with traffic_police and Reference Memory
V0011: with traffic_police, Reference Memory, ignore 1T=0 on en_psb
V0012: BC0 data detection, shorter VME dtack
****

PSB_chip_v2: v0012 copied and then modified for new board PSB9U_V2
V0001: normal TTIN63 input, Testpoint4 is used,
new pin_assignment for Channel Link,
simspy_ctrl with L1A to stop spying, new cmds, new SPY_STATUS regs
V0002: (impl3)VME-read access: put only new data onto the vme-data bus
V0004: (impl4) ROP: Error corrected: ls.bit cut to get correct 12 bit BCNr
TESTPOINTS code improved