VME64x-CHIP

of

PSB-9U_V2-card

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Version 0x1012

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1 Introduction

The VME64x Interface for Global Trigger boards is made for a slave module without interrupt capabilities. It works in systems with backplanes supplying VME64x standard as well as in systems with VME/VME64 backplanes. The Interface will contain a VME64x-chip, a VME-CHIP-PSB, transceivers for VME-data, logic for "live-insertion", DTACK*- and BERR*-drivers and a special VME64x connector (P1/J1).

2 VME64x-chip

2.1 Versionshistory

- **V1012: based** on **V1011**, but no BLT implemented, only F0 used. (HB120407) NEW
- **V1011: based** on **V1010**, but only fixed test-outputs implemented (USER_CSR not used in this version). (HB280307)
- V1010: based on V100F, but VME-addresses are latched on the inputs. (HB290207)
- V100F: based on V100F of VME64x-chip of PSB-card to get a proper JTAGoverVME access. (HB011206)
- V100E: based on V100D of VME64x-chip, but changes in logic of TEST_OUT module made and NIRQ1 implemented. (HB241006)
- V100D: based on V100C of VME64x-chip of PSB-card, but USER_CR.vhd V2.3 used for serial number. (HB300806)

2.2 Changes of signals NEW

The following signals to VME-PSB-chip of the board have got a different meaning:

- ASCYC is S31 (which represents the CARD_NR3).
- ASSYNC is S30 (which represents the CARD_NR2).
- ASPULS is S29 (which represents the CARD_NR1).
- D08_E is S28 (which represents the CARD_NR0).

2.3 Hardware

The VME64x-chip is an Altera EP1K10QC208-3.

2.4 Firmware

```
serial-nr.:    PSB_V2nn        (nn = CARD_NR [dec] jumpers S31-S28)
chip_id:       0x0001Cn11      (n = CARD_NR [hex] jumpers S31-S28)
version:       0x00001012
```

2.5 References

See VME64-specification and VME64x-specification for definitions.

2.6 Features of the VME64x-chip (V1012) NEW

- **User Configuration ROM** (USER_CR: address range 0x01003..0x01033, size is 13 bytes) for **"chip identifier" and "version"** of VME64x-chip (see 2.10.3) [0x01003-0x0101F] and for **"serial number"** of board (see 2.10.3) [0x01023-0x01033].
- **"Card number"** is part of **"chip identifier"** and is fix soldered by jumpers on the lines S31-S28 (CARD_NR[3..0]).
- **"Serial number"** is **PSB_V2nn** (nn is the decimal expression of **"card number"** with leading zero - exception: PSB_V2 #16 has "card number"=0).
- **Function 0** (F0) – **D16** only, base-address at **A31-A25**, AM=**0x0D** and **0x09** (only **single** transfer).

2.7 Fixed test-outputs NEW

TST_OUT_1: CLK_VME64X (40 MHz clock)
TST_OUT_2: DTACK_EXT (from VME-chip)
TST_OUT_3: BERR_EXT (from VME-chip)
TST_OUT_4: DTACK_CR_CSR (internal signal)

2.8 Programmable test-outputs NEW

Not used in this version!!!

2.9 Address spaces overview

AM: **0x2F**, access: **D08_O**
A23-A19: Geographic address (=VME slot number) or '11110'=amnesia address

A18-A00	=>	**Register-name**
mask: 0x000000FF		
0x00003 - 0x007FF	=>	512x8 bit Configuration ROM (read)
0x01003	=>	chip-id_3 (read)
0x01007	=>	chip-id_2 (read)
0x0100B	=>	chip-id_1 (read)
0x0100F	=>	chip-id_0 (read)
0x01013	=>	version_3 (read)
0x01017	=>	version_2 (read)
0x0101B	=>	version_1 (read)
0x0101F	=>	version_0 (read)
0x01023 - 0x0103F	=>	8 bytes Serial Number [PSB_V2nn] (read)
0x03003 - 0x037FF	=>	CRAM 512x8 bit RAM (not used!!) (read/write)
0x05003 - 0x05007	=>	USER_CSR (not used in this version!!) (read/write)
[0x7FC03 - 0x7FFFF	=>	Command/Status registers (read/write)]
0x7FF63	=>	ADER-F0_3 register (read/write)
0x7FF67	=>	ADER-F0_2 register (read/write)
0x7FF6B	=>	ADER-F0_1 register (read/write)
0x7FF6F	=>	ADER-F0_0 register (read/write)
0x7FF73	=>	ADER-F1_3 register (read/write)
0x7FF77	=>	ADER-F1_2 register (read/write)
0x7FF7B	=>	ADER-F1_1 register (read/write)
0x7FF7F	=>	ADER-F1_0 register (read/write)
0x7FFF7	=>	Bit Clear Register [BCR] (read/write)
0x7FFFB	=>	Bit Set Register [BSR] (read/write)
0x7FFFF	=>	BAR - Geographic address (read)

2.10 Parts of the VME64x-chip

2.10.1 Defined Configuration ROM (CR)

The definition of the CR is made in the VME64x-specification (10.2.1 The defined CR area, page 39 and Table 10-12, page 53).

- Checksum (0x03): see VME64-specification (Table 2-32, page 55)
  not calculated yet, to be done in cr.mif!!!
- Length of ROM (0x07..0x0F): see VME64-specification (Table 2-32, page 55)

not calculated yet, to be done in cr.mif!!!

- Configuration ROM data access width (0x13): see VME64-specification (Table 2-32, page 55)
  0x81 => "Only use D08(O), every fourth byte".
- CSR data access width (0x17): see VME64-specification (Table 2-32, page 55)
  0x81 => "Only use D08(O), every fourth byte".
- CR/CSR space specification ID (0x1B): see VME64x-specification (Rule 10.3, page 39)
  0x02 => VME64x.
- Manufactor's ID (0x27..0x2F): see VME64-specification (Table 2-32, page 56)
  0x00.
- Board ID (0x33..0x3F): see VME64-specification (Table 2-32, page 56)
  not fixed yet, has to be defined for all boards of the GT-system!!
- Revision ID (0x43..0x4F): see VME64-specification (Table 2-32, page 56)
  not fixed yet, has to be defined for all boards of the GT-system!!
- Program ID (0x7F): see VME64-specification (Table 2-32, page 56)
  0x01 => "No program, ID ROM only".
- Offset to BEG_USER_CR (0x83..0x8B): see VME64x-specification (Table 10-12, page 53)
  0x01003 => used for chip_id- and version-register.
- Offset to END_USER_CR (0x8F..0x97): see VME64x-specification (Table 10-12, page 53)
  0x0101F => used for chip_id- and version-register.
- Offset to BEG_CRAM (0x9B..0xA3): see VME64x-specification (Table 10-12, page 53)
  0x03003 => used for future applications.
- Offset to END_CRAM (0xA7..0xAF): see VME64x-specification (Table 10-12, page 53)
  0x037FF => used for future applications.
- Offset to BEG_USER_CSR (0xB3..0xBB): see VME64x-specification (Table 10-12, page 53)
  0x05003 => not used.
- Offset to END_USER_CSR (0xBF..0xC7): see VME64x-specification (Table 10-12, page 53)
  0x0502F => not used.
- Offset to BEG_SN (0xCB..0xD3): see VME64x-specification (Table 10-12, page 53)
  0x01023 => part of USER_CR, contains the "serial number".
- Offset to END_SN (0xD7..0xDF): see VME64x-specification (Table 10-12, page 53)
  0x0103F.
- Slave characteristics parameter (0xE3): see VME64x-specification (Table 10-1, page 40)
  0x00.
- Master characteristics parameter (0xEB): see VME64x-specification (Table 10-2, page 40)
  0x00.
- CRAM_ACCESS_WIDTH (0xFF): see VME64x-specification (Table 10-10, page 49)
  0x81 => "Only use D08(O), every fourth byte".
- Function 0 DAWPR (0x103..0x107): see VME64x-specification (Table 10-3, page 42)
  0x83 => "Accepts D16 cycles only".
- Function 0 AMCAP (0x123..0x13F): see VME64x-specification (Table 10-5, page 44)
  0x0000 0000 0000 2200 => AM=0x0D and 0x09 "extended data access" - single access.
- Function 0 ADEM (0x623..0x63F): see VME64x-specification (Table 10-4, page 43)
  0xFE000000 => "mask bits 31-25=1".

2.10.2 Defined Control/Status Register (CSR)

The definition of the CSR is made in the VME64x-specification (10.2.2 The defined CSR area, page 45 and Table 10-13, page 55).

- **Base Address Register** (BAR) (0x7FFFF): see VME64x-specification (Table 10-13, page 55), set with geographical address or amnesia address.
- **Bit Set Register** (BSR) (0x7FFFB): see VME64x-specification (Table 10-13, page 55), for settting see Table 10-6, page 45.
- **Bit Clear Register** (BCR) (0x7FFF7): see VME64x-specification (Table 10-13, page 55), for settting see Table 10-7, page 46.
  BCR, BSR bits:
  Bit 7: EN/DIS RESET_MODE
  Bit 4: EN/DIS MODULE
  Bit 3: EN/DIS BERR FLAG
- **Function 0 ADER** (0x7FF63..0x7FF6F): see VME64x-specification (Table 10-13, page 55), used for address relocation with Function 0 ADEM and Function 0 AMCAP (see Table 10-8, page 47).

2.10.3 Chip_ID and version ROM space

A user configuration ROM is implemented for the “chip_ID“ and “version” of the VME64x-chip of the board. It is located at the addresses 0x01003-0x0101F, size is 8 bytes, part of the USER_CR.

2.10.4 Serial Number ROM space

A user configuration ROM is implemented for the “serial number“ of the board. It is located at the addresses 0x01023-0x0103F, size is 8 bytes (PSB_V2nn), part of the USER_CR.

2.10.5 USER_CSR space

Not used in this version!!!

2.10.6 CRAM space

The configuration RAM (CRAM) is defined as a RAM for special purpose. The size is 512 bytes. The CRAM is located at addresses 0x03003..0x037FF.
The contains of the CRAM has to be defined!!!

3 Softwareguide for the VME64x Interface

3.1 Module enable

After power-up the module is disabled through the default value of the “ENABLE MODULE”-bit of the BitSet-register in the CommandStatusRegister (CSR) of VME64x.
To enable the module, one has to set bit 4 in the CSR, that means to write 0x10 to address 0x7FFFB with AM=0x2F.