Declarations

Ports:

```
ADDR           : std_logic_vector(21 DOWNTO 1)
BCRES          : std_logic
CA3            : std_logic_vector(31 DOWNTO 0)
CA4            : std_logic_vector(31 DOWNTO 0)
CA5            : std_logic_vector(31 DOWNTO 0)
CA6            : std_logic_vector(31 DOWNTO 0)
CLK_FBIN_REC2  : std_logic
CLK_REC2       : std_logic
EN_REC2        : std_logic
L1A            : std_logic
L1RESET        : std_logic
RESERVEVME     : std_logic
RES_DCM        : std_logic
WR_REC2        : std_logic
CA313A         : std_logic_vector(15 DOWNTO 0)
CA313B         : std_logic_vector(15 DOWNTO 0)
CA324A         : std_logic_vector(15 DOWNTO 0)
CA324B         : std_logic_vector(15 DOWNTO 0)
CA413A         : std_logic_vector(15 DOWNTO 0)
CA413B         : std_logic_vector(15 DOWNTO 0)
CA424A         : std_logic_vector(15 DOWNTO 0)
CA424B         : std_logic_vector(15 DOWNTO 0)
CA513A         : std_logic_vector(15 DOWNTO 0)
CA513B         : std_logic_vector(15 DOWNTO 0)
CA524A         : std_logic_vector(15 DOWNTO 0)
CA524B         : std_logic_vector(15 DOWNTO 0)
CA613A         : std_logic_vector(15 DOWNTO 0)
CA613B         : std_logic_vector(15 DOWNTO 0)
CA624A         : std_logic_vector(15 DOWNTO 0)
CA624B         : std_logic_vector(15 DOWNTO 0)
CLK_FBOUT_REC2 : std_logic
CLK_LOCKED     : std_logic
NDTACK_REC     : std_logic
RESERVE1       : std_logic_vector(15 DOWNTO 0)
RESERVE2       : std_logic_vector(15 DOWNTO 0)
STAT_REC2      : std_logic_vector(1 DOWNTO 0)
TEST0          : std_logic
TEST1          : std_logic
TEST2          : std_logic
TEST3          : std_logic
VDATA          : std_logic_vector(15 DOWNTO 0)
```

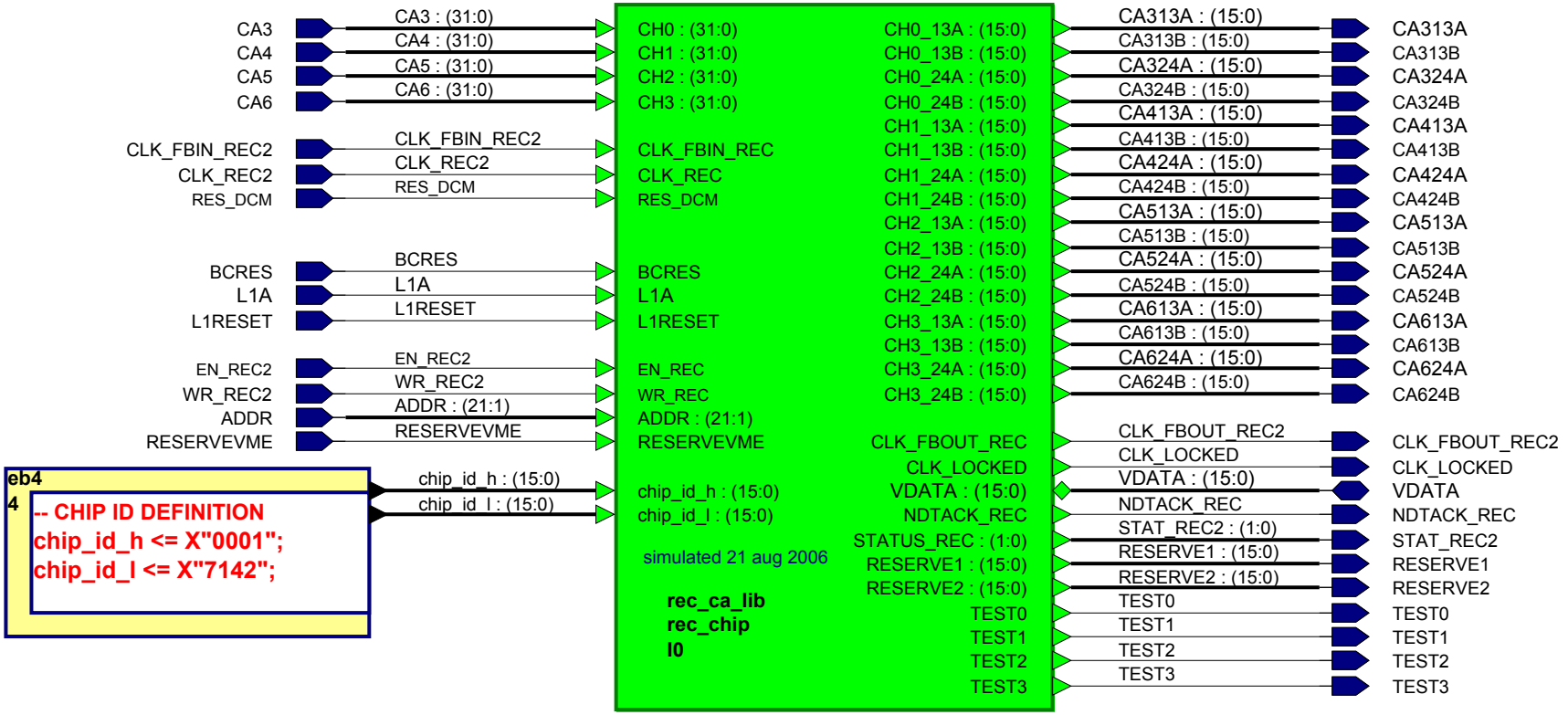
Diagram Signals:

```
SIGNAL chip_id_h      : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_id_l      : std_logic_vector(15 DOWNTO 0)
```

Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
USE IEEE.VITAL_Timing.all;
LIBRARY STD;
USE STD.TEXTIO.all;
LIBRARY unisim;
USE unisim.VPKG.all;
USE IEEE.numeric_std.all;
USE unisim.VCOMPONENTS.all;
```

<company name>		Project:	rec_ca
		<enter comments here>	
Title:	<enter diagram title here>		
Path:	rec_ca_lib/rec2_chip/struct		
Edited:	by taurok on 23 Aug 2006		



WRAPPING FILE for REC2 chip

REC2 chip