Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
```

Declarations

Ports:

```
ADDR           : std_logic_vector(21 DOWNTO 1)
BCRES          : std_logic
CA1            : std_logic_vector(31 DOWNTO 0)
CA2            : std_logic_vector(31 DOWNTO 0)
CLK_FBIN_REC1  : std_logic
CLK_REC1       : std_logic
EN_REC1        : std_logic
L1A            : std_logic
L1RESET        : std_logic
MUON12         : std_logic_vector(29 DOWNTO 0)
MUON34         : std_logic_vector(29 DOWNTO 0)
RESERVEVME     : std_logic
RES_DCM        : std_logic
WR_REC1        : std_logic
CA113A         : std_logic_vector(15 DOWNTO 0)
CA113B         : std_logic_vector(15 DOWNTO 0)
CA124A         : std_logic_vector(15 DOWNTO 0)
CA124B         : std_logic_vector(15 DOWNTO 0)
CA213A         : std_logic_vector(15 DOWNTO 0)
CA213B         : std_logic_vector(15 DOWNTO 0)
CA224A         : std_logic_vector(15 DOWNTO 0)
CA224B         : std_logic_vector(15 DOWNTO 0)
CLK_FBOUT_REC1 : std_logic
CLK_LOCKED     : std_logic
MU1A           : std_logic_vector(29 DOWNTO 0)
MU1B           : std_logic_vector(29 DOWNTO 0)
MU3A           : std_logic_vector(29 DOWNTO 0)
MU3B           : std_logic_vector(29 DOWNTO 0)
NDTACK_REC     : std_logic
RESERVE1       : std_logic_vector(15 DOWNTO 0)
RESERVE2       : std_logic_vector(15 DOWNTO 0)
STAT_REC1      : std_logic_vector(1 DOWNTO 0)
TEST0          : std_logic
TEST1          : std_logic
TEST2          : std_logic
TEST3          : std_logic
VDATA          : std_logic_vector(15 DOWNTO 0)
```

Diagram Signals:

```
SIGNAL CH0           : std_logic_vector(31 DOWNTO 0)
SIGNAL CH0_13A       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH0_13B       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH0_24A       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH0_24B       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH1           : std_logic_vector(31 DOWNTO 0)
SIGNAL CH1_13A       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH1_13B       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH1_24A       : std_logic_vector(15 DOWNTO 0)
SIGNAL CH1_24B       : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_id_h     : std_logic_vector(15 DOWNTO 0)
SIGNAL chip_id_l     : std_logic_vector(15 DOWNTO 0)
```

<company name>		Project:	rec_ca
		<enter comments here>	
Title:	<enter diagram title here>		
Path:	rec_ca_lib/rec1_chip/struct		
Edited:	by taurok on 23 Aug 2006		

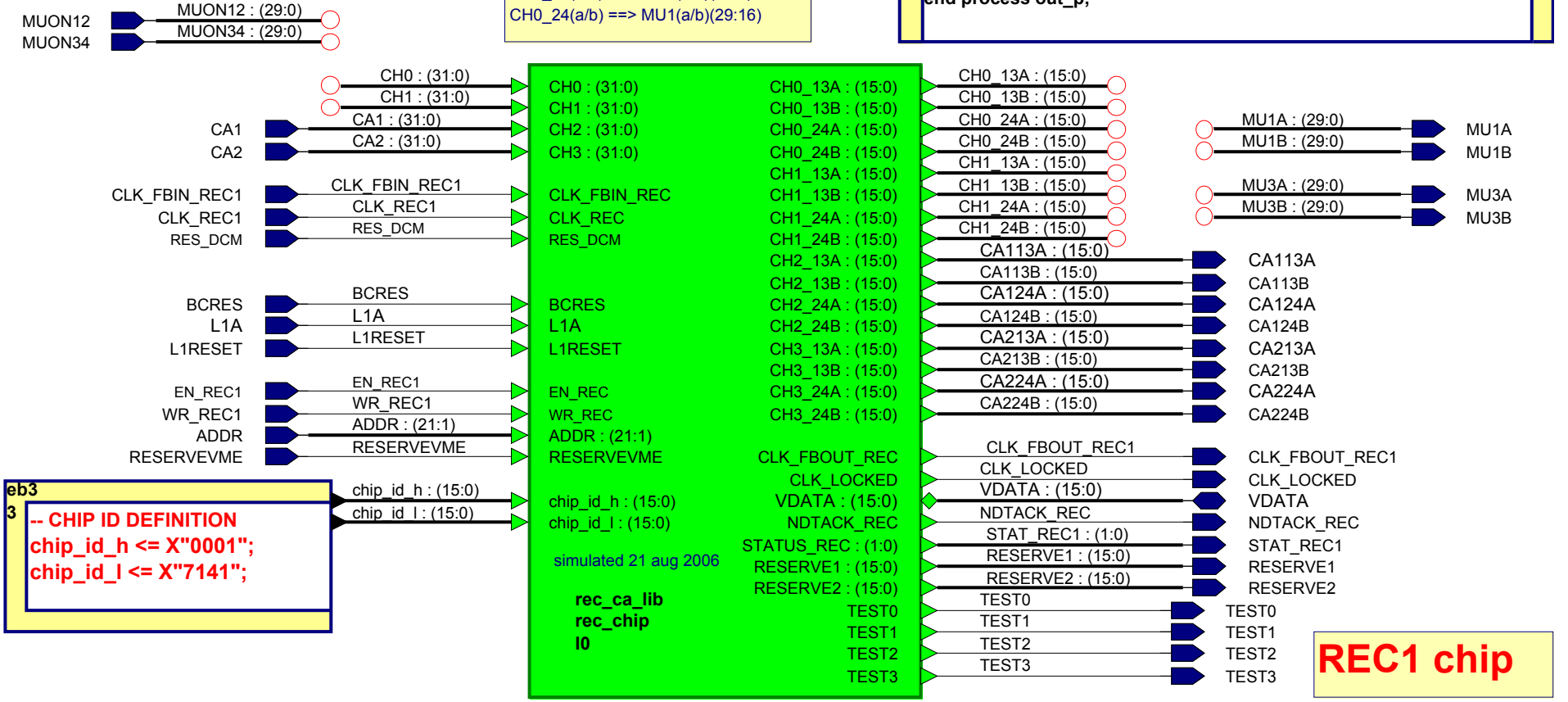
eb1
1

```
-- eb1 1
assign_p: process(MUON12, MUON34)
  begin
  for i in 0 to 29 loop
    CH0(i) <= MUON12(i);
    CH1(i) <= MUON34(i);
  end loop;
  CH0(30) <= '0'; CH0(31) <= '0';
  CH1(30) <= '0'; CH1(31) <= '0';
end process assign_p;
```

eb2
2

```
out_p: process(
    CH0_13A, CH0_13B, CH1_13A, CH1_13B,
    CH0_24A, CH0_24B, CH1_24A, CH1_24B)
 begin
 for i in 0 to 15 loop
   MU1A(i) <= CH0_13A(i); MU1B(i) <= CH0_13B(i);
   MU3A(i) <= CH1_13A(i); MU3B(i) <= CH1_13B(i);
 end loop;
 for i in 16 to 29 loop
   MU1A(i) <= CH0_24A(i-16); MU1B(i) <= CH0_24B(i-16);
   MU3A(i) <= CH1_24A(i-16); MU3B(i) <= CH1_24B(i-16);
 end loop;
end process out_p;
```

CH0_13(a/b) ==> MU1(a/b)(15:0)
CH0_24(a/b) ==> MU1(a/b)(29:16)



eb3
3

```
-- CHIP ID DEFINITION
chip_id_h <= X"0001";
chip_id_l <= X"7141";
```

REC1 chip