Declarations

Ports:

```
ADDR           : std_logic_vector(21 DOWNTO 1)
BCRES          : std_logic
CH0            : std_logic_vector(31 DOWNTO 0)
CH1            : std_logic_vector(31 DOWNTO 0)
CH2            : std_logic_vector(31 DOWNTO 0)
CH3            : std_logic_vector(31 DOWNTO 0)
CLK_FBIN_REC   : std_logic
CLK_REC        : std_logic
EN_REC         : std_logic
L1A            : std_logic
L1RESET        : std_logic
RESERVEVME     : std_logic
RES_DCM        : std_logic
WR_REC         : std_logic
chip_id_h      : std_logic_vector(15 DOWNTO 0)
chip_id_l      : std_logic_vector(15 DOWNTO 0)
CH0_13A        : std_logic_vector(15 DOWNTO 0)
CH0_13B        : std_logic_vector(15 DOWNTO 0)
CH0_24A        : std_logic_vector(15 DOWNTO 0)
CH0_24B        : std_logic_vector(15 DOWNTO 0)
CH1_13A        : std_logic_vector(15 DOWNTO 0)
CH1_13B        : std_logic_vector(15 DOWNTO 0)
CH1_24A        : std_logic_vector(15 DOWNTO 0)
CH1_24B        : std_logic_vector(15 DOWNTO 0)
CH2_13A        : std_logic_vector(15 DOWNTO 0)
CH2_13B        : std_logic_vector(15 DOWNTO 0)
CH2_24A        : std_logic_vector(15 DOWNTO 0)
CH2_24B        : std_logic_vector(15 DOWNTO 0)
CH3_13A        : std_logic_vector(15 DOWNTO 0)
CH3_13B        : std_logic_vector(15 DOWNTO 0)
CH3_24A        : std_logic_vector(15 DOWNTO 0)
CH3_24B        : std_logic_vector(15 DOWNTO 0)
CLK_FBOUT_REC  : std_logic
CLK_LOCKED     : std_logic
NDTACK_REC     : std_logic
RESERVE1       : std_logic_vector(15 DOWNTO 0)
RESERVE2       : std_logic_vector(15 DOWNTO 0)
STATUS_REC     : std_logic_vector(1 DOWNTO 0)
TEST0          : std_logic
TEST1          : std_logic
TEST2          : std_logic
TEST3          : std_logic
VDATA          : std_logic_vector(15 DOWNTO 0)
```

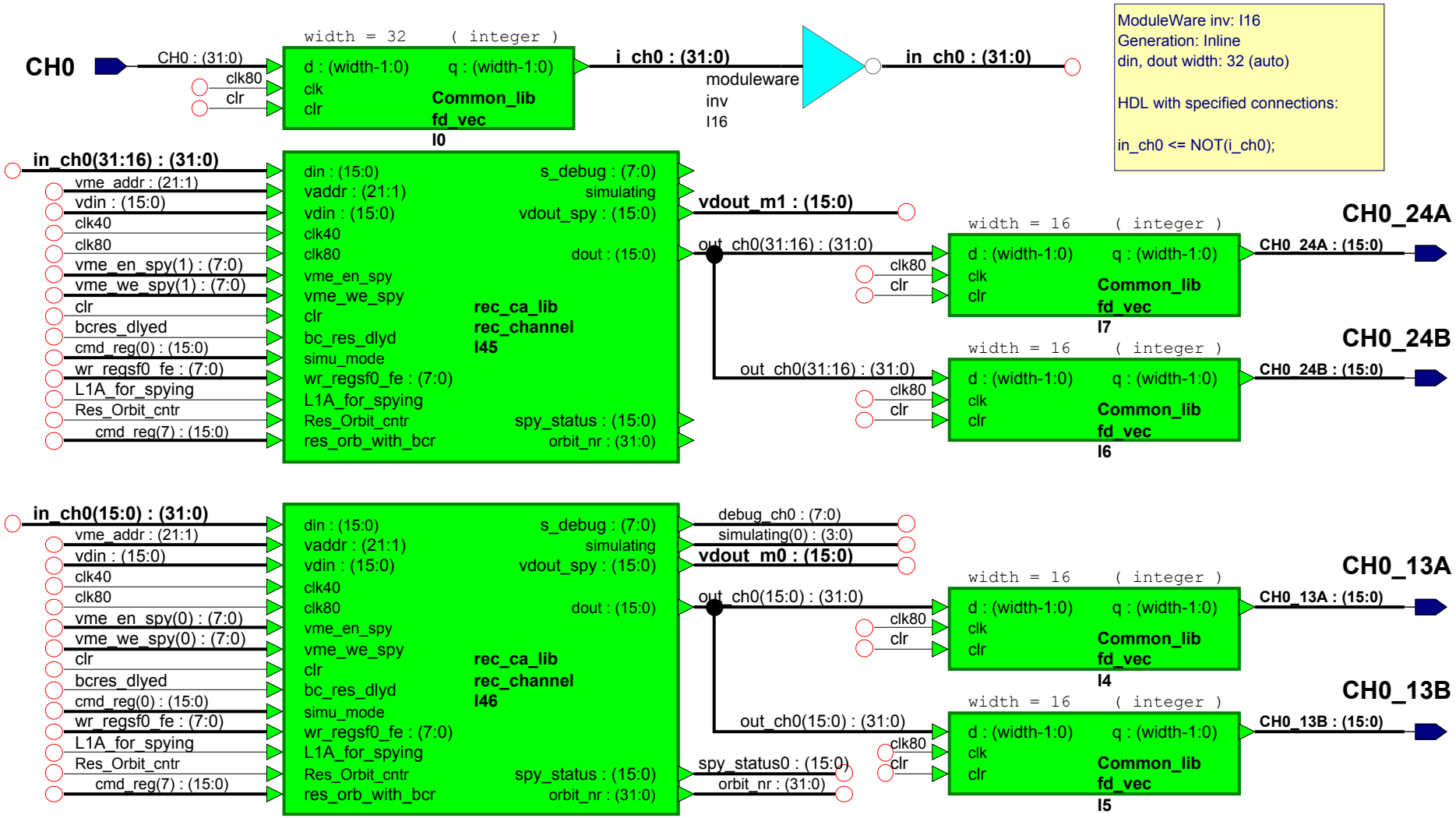
Diagram Signals:

```
SIGNAL BCRESx         : std_logic
SIGNAL BCRes_int      : std_logic
SIGNAL CLK0           : std_ulogic
SIGNAL CLK2X          : std_ulogic
SIGNAL CLKIN          : std_ulogic
SIGNAL L1A_for_spying : std_logic
SIGNAL L1Ax           : std_logic
SIGNAL L1RESETx       : std_logic
SIGNAL L1Res_int      : std_logic
SIGNAL LOCKED         : std_ulogic
SIGNAL RST            : std_ulogic
SIGNAL Res_Orbit_cntr : std_logic
SIGNAL bc_error_flag  : std_logic
```

Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
USE IEEE.VITAL_Timing.all;
LIBRARY STD;
USE STD.TEXTIO.all;
LIBRARY unisim;
USE unisim.VPKG.all;
USE IEEE.numeric_std.all;
USE unisim.VCOMPONENTS.all;
USE IEEE.VITAL_Primitives.all;
```

<company name>		Project:	rec_ca
		V1005	
Title:	<enter diagram title here>		
Path:	rec_ca_lib/rec_chip/struct		
Edited:	by taurok on 23 Aug 2006		

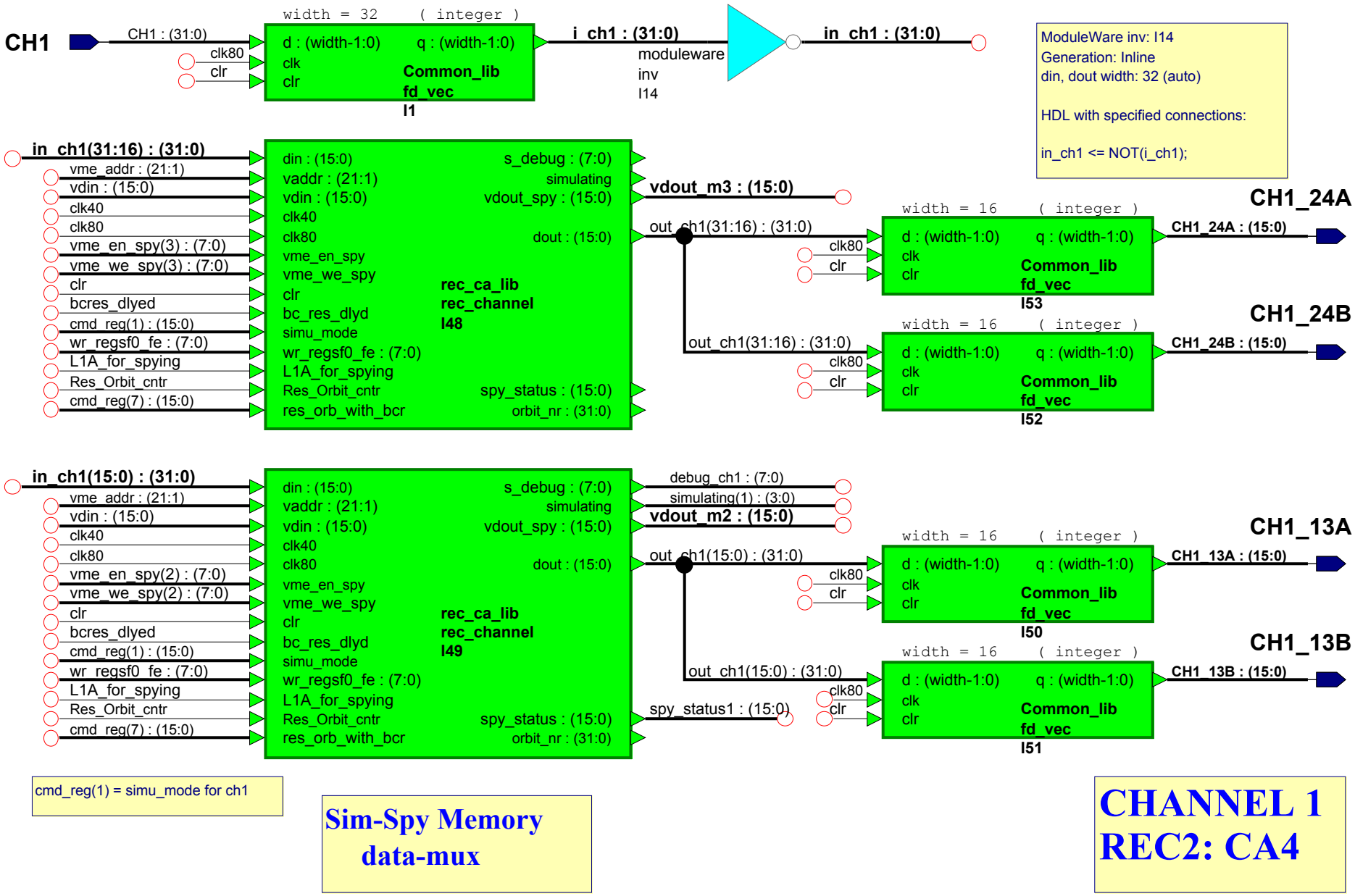


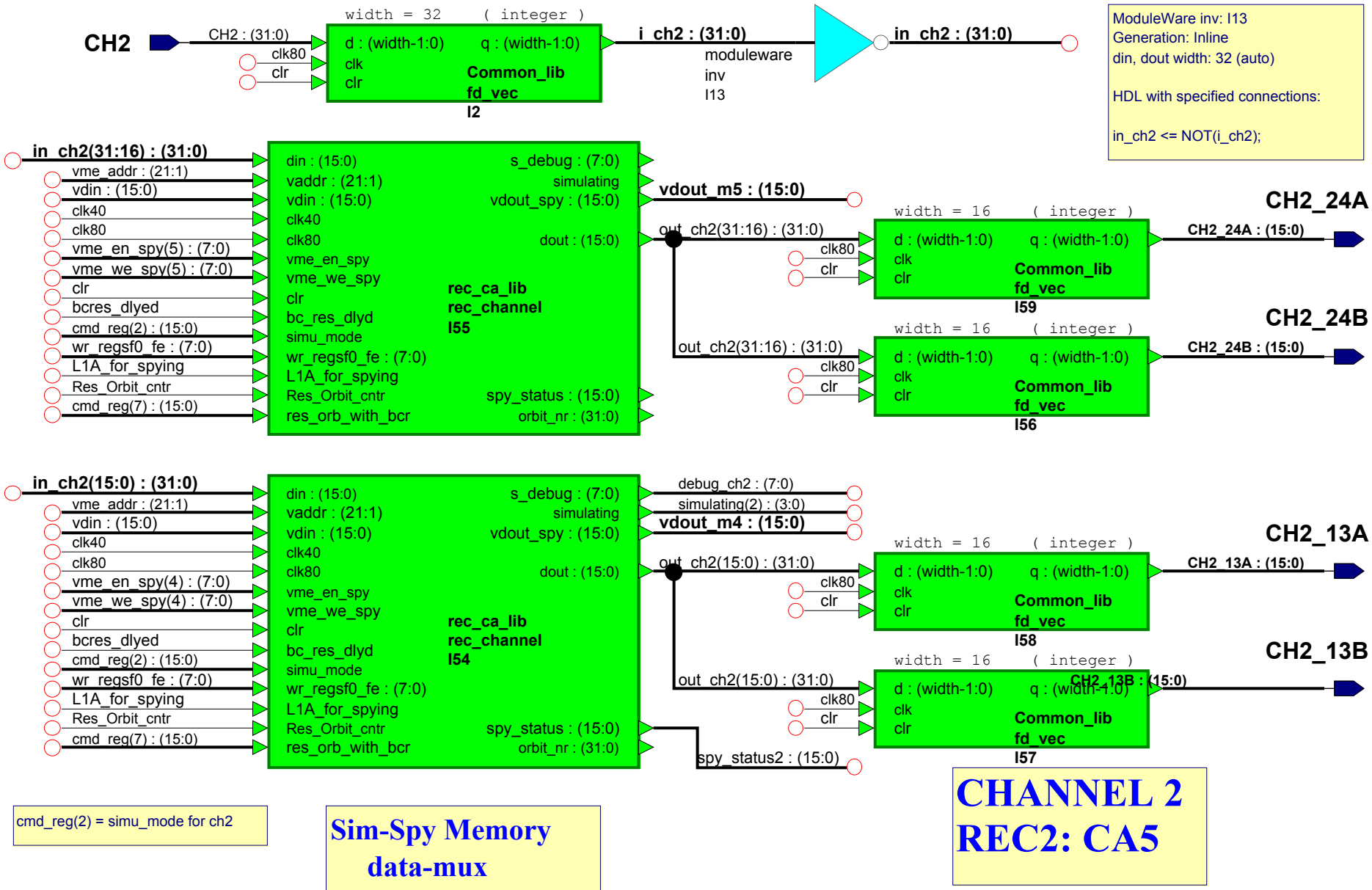
INTERFACE Description GCT ==> PSB:
Remark: obj1 = highest rank
GCT--->|---------- PSB ---------->|------- Backplane -->| ------ REC ----> COND
cable0:pin 5,6 ==> pair1 ==> ch1: obj2 then 4 ==> CAx(31:16) =======> CAx24
cable0:pin 2,3 ==> pair0 ==> ch0: obj1 then 3 ==> CAx(15:00) =======> CAx13

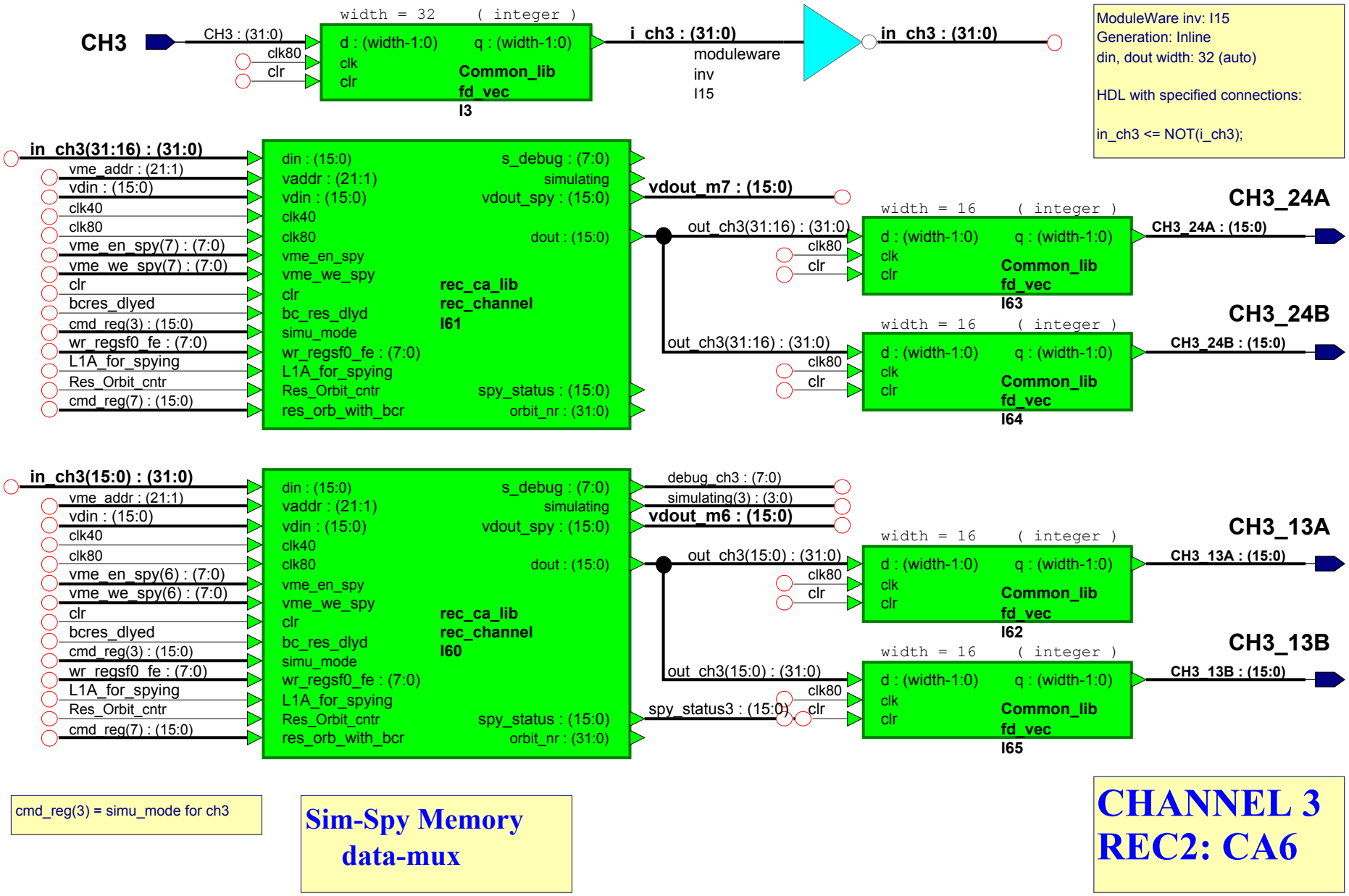
cmd_reg(0) = simu_mode for ch0

Sim-Spy Memory data-mux

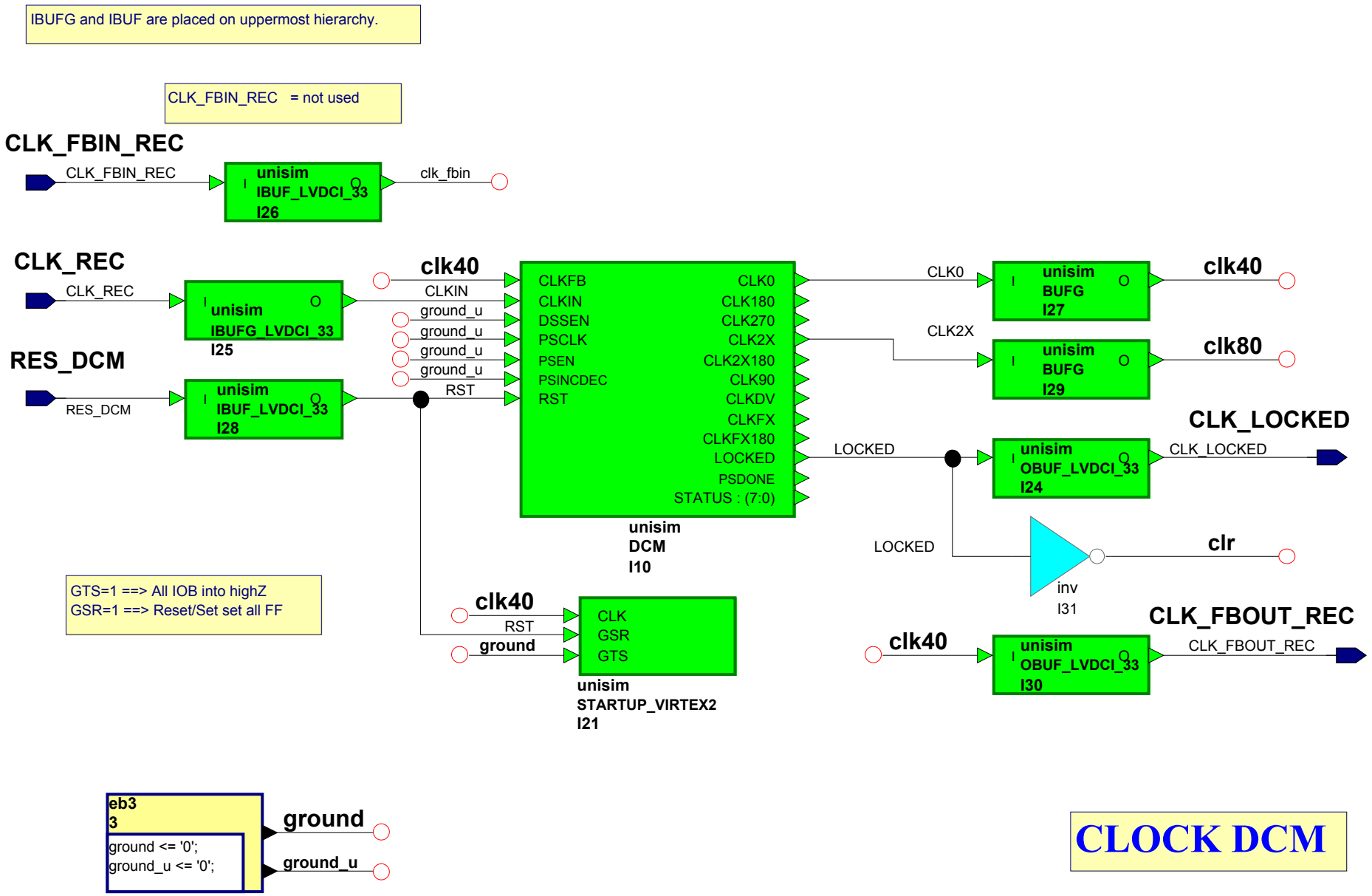
CHANNEL 0
REC2: CA3

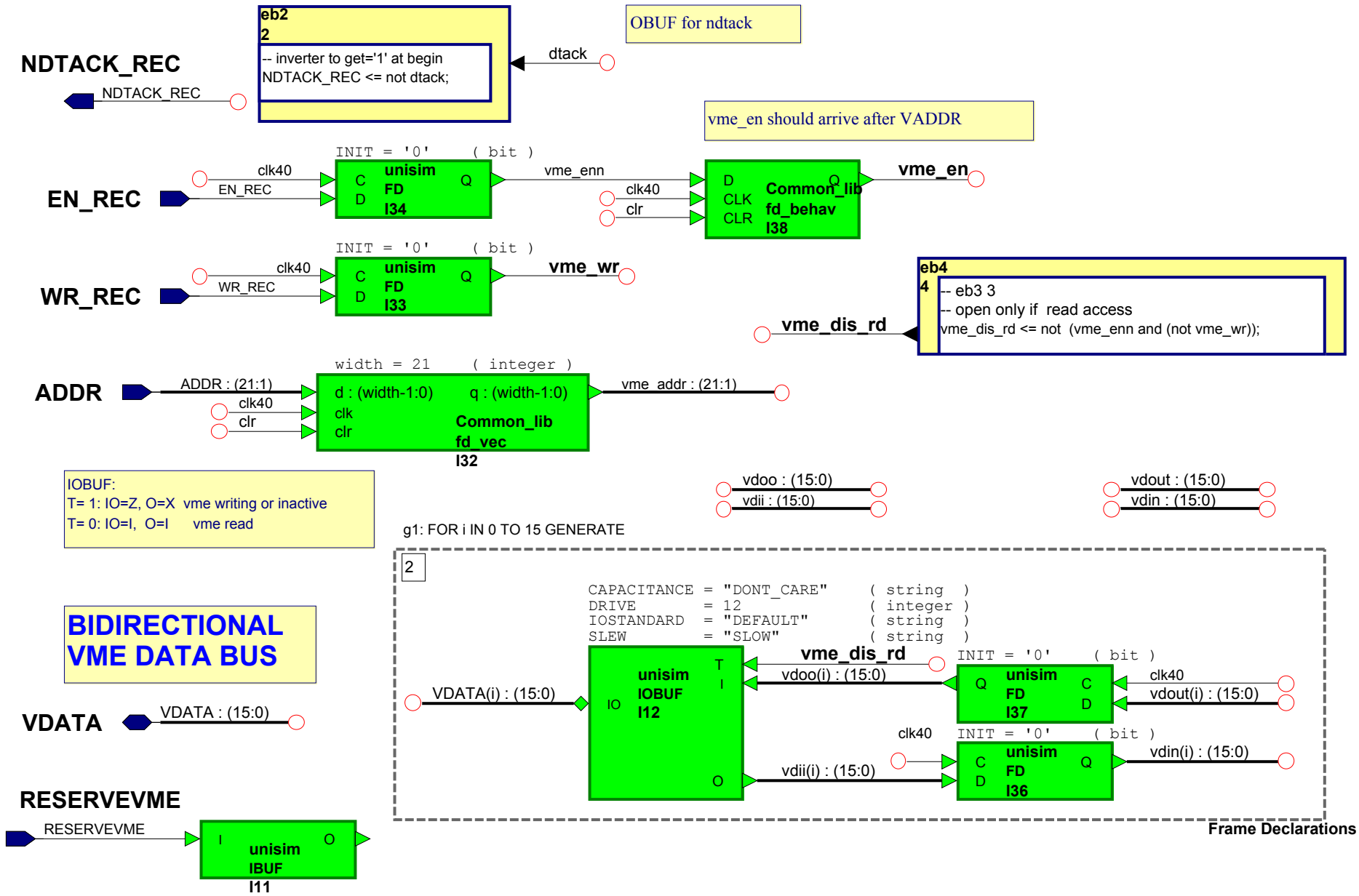

CH1
CH1 : (31:0)
clk80
clr
width = 32 (integer)
d : (width-1:0)
q : (width-1:0)
clk
clr
Common_lib
fd_vec
I1
i_ch1 : (31:0)
moduleware
inv
I14
in_ch1 : (31:0)
ModuleWare inv: I14
Generation: Inline
din, dout width: 32 (auto)
HDL with specified connections:
in_ch1 <= NOT(i_ch1);
in_ch1(31:16) : (31:0)
vme_addr : (21:1)
vdin : (15:0)
clk40
clk80
vme_en_spy(3) : (7:0)
vme_we_spy(3) : (7:0)
clr
bcres_dlyed
cmd_reg(1) : (15:0)
wr_regsf0_fe : (7:0)
L1A_for_spying
Res_Orbit_cntr
cmd_reg(7) : (15:0)
din : (15:0)
vaddr : (21:1)
vdin : (15:0)
clk40
clk80
vme_en_spy
vme_we_spy
clr
bc_res_dlyd
simu_mode
wr_regsf0_fe : (7:0)
L1A_for_spying
Res_Orbit_cntr
res_orb_with_bcr
s_debug : (7:0)
simulating
vdout_spy : (15:0)
dout : (15:0)
spy_status : (15:0)
orbit_nr : (31:0)
rec_ca_lib
rec_channel
I48
vdout_m3 : (15:0)
out_ch1(31:16) : (31:0)
CH1_24A
CH1_24A : (15:0)
CH1_24B
CH1_24B : (15:0)
I53
I52
in_ch1(15:0) : (31:0)
debug_ch1 : (7:0)
simulating(1) : (3:0)
vdout_m2 : (15:0)
out_ch1(15:0) : (31:0)
spy_status1 : (15:0)
CH1_13A
CH1_13A : (15:0)
CH1_13B
CH1_13B : (15:0)
I50
I51
cmd_reg(1) = simu_mode for ch1
Sim-Spy Memory
data-mux
CHANNEL 1
REC2: CA4

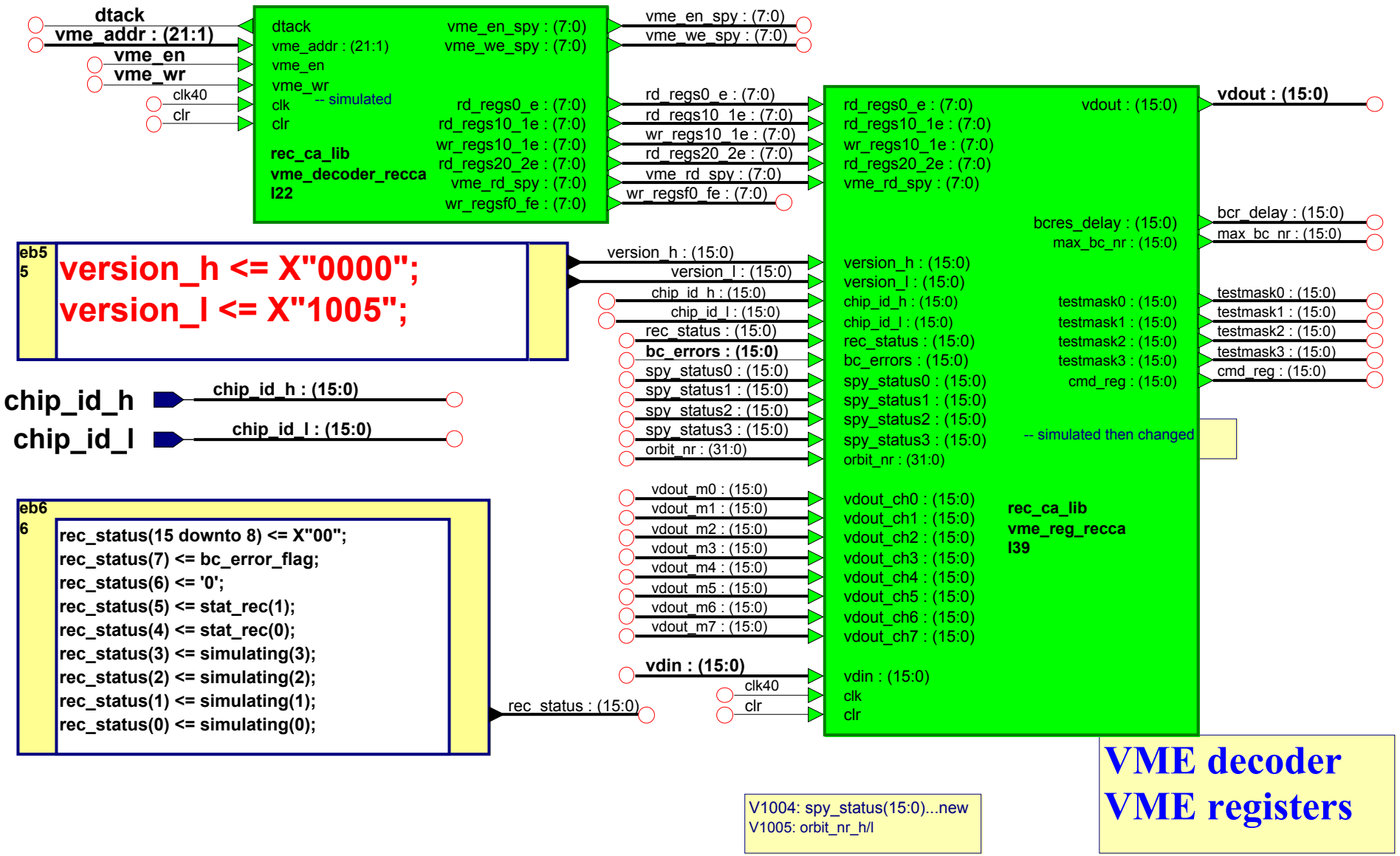

CH2
CH2 : (31:0)
clk80
clr
width = 32 (integer)
d : (width-1:0)
q : (width-1:0)
clk
clr
Common_lib
fd_vec
I2
i_ch2 : (31:0)
moduleware
inv
I13
in_ch2 : (31:0)
ModuleWare inv: I13
Generation: Inline
din, dout width: 32 (auto)
HDL with specified connections:
in_ch2 <= NOT(i_ch2);
in_ch2(31:16) : (31:0)
vme_addr : (21:1)
vdin : (15:0)
clk40
clk80
vme_en_spy(5) : (7:0)
vme_we_spy(5) : (7:0)
clr
bcres_dlyed
cmd_reg(2) : (15:0)
wr_regsf0_fe : (7:0)
L1A_for_spying
Res_Orbit_cntr
cmd_reg(7) : (15:0)
din : (15:0)
vaddr : (21:1)
vdin : (15:0)
clk40
clk80
vme_en_spy
vme_we_spy
clr
bc_res_dlyd
simu_mode
wr_regsf0_fe : (7:0)
L1A_for_spying
Res_Orbit_cntr
res_orb_with_bcr
s_debug : (7:0)
simulating
vdout_spy : (15:0)
dout : (15:0)
spy_status : (15:0)
orbit_nr : (31:0)
rec_ca_lib
rec_channel
I55
vdout_m5 : (15:0)
out_ch2(31:16) : (31:0)
width = 16 (integer)
CH2_24A
CH2_24A : (15:0)
Common_lib
fd_vec
I59
CH2_24B
CH2_24B : (15:0)
I56
in_ch2(15:0) : (31:0)
debug_ch2 : (7:0)
simulating(2) : (3:0)
vdout_m4 : (15:0)
out_ch2(15:0) : (31:0)
CH2_13A
CH2_13A : (15:0)
I58
CH2_13B
CH2_13B : (15:0)
I57
spy_status2 : (15:0)
cmd_reg(2) = simu_mode for ch2
Sim-Spy Memory
data-mux
CHANNEL 2
REC2: CA5


CH3
CH3 : (31:0)
clk80
clr
width = 32 (integer)
d : (width-1:0)
q : (width-1:0)
clk
clr
Common_lib
fd_vec
I3
i_ch3 : (31:0)
moduleware
inv
I15
in_ch3 : (31:0)
ModuleWare inv: I15
Generation: Inline
din, dout width: 32 (auto)
HDL with specified connections:
in_ch3 <= NOT(i_ch3);
in_ch3(31:16) : (31:0)
vme_addr : (21:1)
vdin : (15:0)
clk40
clk80
vme_en_spy(7) : (7:0)
vme_we_spy(7) : (7:0)
clr
bcres_dlyed
cmd_reg(3) : (15:0)
wr_regsf0_fe : (7:0)
L1A_for_spying
Res_Orbit_cntr
cmd_reg(7) : (15:0)
din : (15:0)
vaddr : (21:1)
vdin : (15:0)
clk40
clk80
vme_en_spy
vme_we_spy
clr
bc_res_dlyd
simu_mode
wr_regsf0_fe : (7:0)
L1A_for_spying
Res_Orbit_cntr
res_orb_with_bcr
s_debug : (7:0)
simulating
vdout_spy : (15:0)
dout : (15:0)
spy_status : (15:0)
orbit_nr : (31:0)
rec_ca_lib
rec_channel
I61
vdout_m7 : (15:0)
out_ch3(31:16) : (31:0)
width = 16 (integer)
CH3_24A
CH3_24A : (15:0)
I63
CH3_24B
CH3_24B : (15:0)
I64
in_ch3(15:0) : (31:0)
debug_ch3 : (7:0)
simulating(3) : (3:0)
vdout_m6 : (15:0)
out_ch3(15:0) : (31:0)
spy_status3 : (15:0)
CH3_13A
CH3_13A : (15:0)
I62
CH3_13B
CH3_13B : (15:0)
I65
cmd_reg(3) = simu_mode for ch3
Sim-Spy Memory
data-mux
CHANNEL 3
REC2: CA6

```
SIGNAL bc_errors      : std_logic_vector(15 DOWNTO 0)
SIGNAL bcr_delay      : std_logic_vector(15 DOWNTO 0)
SIGNAL bcres_dlyed    : std_logic
SIGNAL clk40          : std_ulogic
SIGNAL clk80          : std_logic
SIGNAL clk_fbin       : std_ulogic
SIGNAL clr            : std_logic
SIGNAL cmd_reg        : std_logic_vector(15 DOWNTO 0)
SIGNAL debug_ch0      : std_logic_vector(7 DOWNTO 0) -- debug output
SIGNAL debug_ch1      : std_logic_vector(7 DOWNTO 0) -- debug output
SIGNAL debug_ch2      : std_logic_vector(7 DOWNTO 0) -- debug output
SIGNAL debug_ch3      : std_logic_vector(7 DOWNTO 0) -- debug output
SIGNAL dtack          : std_logic
SIGNAL ground         : std_ulogic
SIGNAL ground_u       : std_ulogic
SIGNAL i_ch0          : std_logic_vector(31 DOWNTO 0)
SIGNAL i_ch1          : std_logic_vector(31 DOWNTO 0)
SIGNAL i_ch2          : std_logic_vector(31 DOWNTO 0)
SIGNAL i_ch3          : std_logic_vector(31 DOWNTO 0)
SIGNAL in_ch0         : std_logic_vector(31 DOWNTO 0)
SIGNAL in_ch1         : std_logic_vector(31 DOWNTO 0)
SIGNAL in_ch2         : std_logic_vector(31 DOWNTO 0)
SIGNAL in_ch3         : std_logic_vector(31 DOWNTO 0)
SIGNAL inc_bcerror    : std_logic
SIGNAL max_bc_nr      : std_logic_vector(15 DOWNTO 0)
SIGNAL orbit_nr       : std_logic_vector(31 DOWNTO 0)
SIGNAL out_ch0        : std_logic_vector(31 DOWNTO 0)
SIGNAL out_ch1        : std_logic_vector(31 DOWNTO 0)
SIGNAL out_ch2        : std_logic_vector(31 DOWNTO 0)
SIGNAL out_ch3        : std_logic_vector(31 DOWNTO 0)
SIGNAL rd_regs0_e     : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_regs10_1e   : std_logic_vector(7 DOWNTO 0)
SIGNAL rd_regs20_2e   : std_logic_vector(7 DOWNTO 0)
SIGNAL rec_status     : std_logic_vector(15 DOWNTO 0)
SIGNAL simulating     : std_logic_vector(3 DOWNTO 0)
SIGNAL spy_status0    : std_logic_vector(15 DOWNTO 0)
SIGNAL spy_status1    : std_logic_vector(15 DOWNTO 0)
SIGNAL spy_status2    : std_logic_vector(15 DOWNTO 0)
SIGNAL spy_status3    : std_logic_vector(15 DOWNTO 0)
SIGNAL stat_rec       : std_logic_vector(1 DOWNTO 0)
SIGNAL testmask0      : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask1      : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask2      : std_logic_vector(15 DOWNTO 0)
SIGNAL testmask3      : std_logic_vector(15 DOWNTO 0)
SIGNAL vdii           : std_logic_vector(15 DOWNTO 0)
SIGNAL vdin           : std_logic_vector(15 DOWNTO 0)
SIGNAL vdoo           : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout          : std_logic_vector(15 DOWNTO 0) --to vme
SIGNAL vdout_m0       : std_logic_vector(15 DOWNTO 0) --simspy
SIGNAL vdout_m1       : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_m2       : std_logic_vector(15 DOWNTO 0) --simspy
SIGNAL vdout_m3       : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_m4       : std_logic_vector(15 DOWNTO 0) --simspy
SIGNAL vdout_m5       : std_logic_vector(15 DOWNTO 0)
SIGNAL vdout_m6       : std_logic_vector(15 DOWNTO 0) --simspy
SIGNAL vdout_m7       : std_logic_vector(15 DOWNTO 0)
SIGNAL version_h      : std_logic_vector(15 DOWNTO 0)
SIGNAL version_l      : std_logic_vector(15 DOWNTO 0)
SIGNAL vme_addr       : std_logic_vector(21 DOWNTO 1)
SIGNAL vme_dis_rd     : std_ulogic
SIGNAL vme_en         : std_logic
SIGNAL vme_en_spy     : std_logic_vector(7 DOWNTO 0) -- to mem's
```

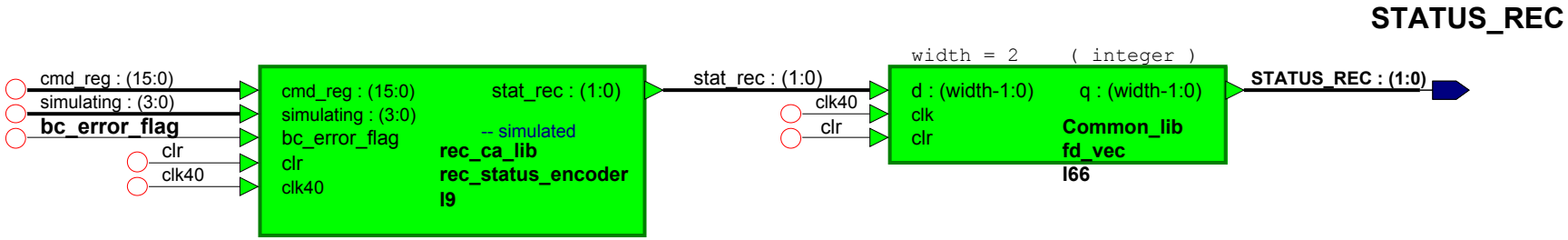

IBUFG and IBUF are placed on uppermost hierarchy.
CLK_FBIN_REC = not used
CLK_FBIN_REC
CLK_FBIN_REC
unisim
IBUF_LVDCI_33
I26
clk_fbin
CLK_REC
CLK_REC
unisim
IBUFG_LVDCI_33
I25
RES_DCM
RES_DCM
unisim
IBUF_LVDCI_33
I28
clk40
CLKIN
ground_u
ground_u
ground_u
ground_u
RST
CLKFB
CLKIN
DSSEN
PSCLK
PSEN
PSINCDEC
RST
CLK0
CLK180
CLK270
CLK2X
CLK2X180
CLK90
CLKDV
CLKFX
CLKFX180
LOCKED
PSDONE
STATUS : (7:0)
unisim
DCM
I10
CLK0
unisim
BUFG
I27
clk40
CLK2X
unisim
BUFG
I29
clk80
LOCKED
unisim
OBUF_LVDCI_33
I24
CLK_LOCKED
CLK_LOCKED
LOCKED
inv
I31
clr
GTS=1 ==> All IOB into highZ
GSR=1 ==> Reset/Set set all FF
clk40
RST
ground
CLK
GSR
GTS
unisim
STARTUP_VIRTEX2
I21
clk40
unisim
OBUF_LVDCI_33
I30
CLK_FBOUT_REC
CLK_FBOUT_REC
eb3
3
ground <= '0';
ground_u <= '0';
ground
ground_u
CLOCK DCM


eb2
2
-- inverter to get='1' at begin
NDTACK_REC <= not dtack;
OBUF for ndtack
NDTACK_REC
NDTACK_REC
dtack
vme_en should arrive after VADDR
INIT = '0' (bit)
EN_REC
clk40
EN_REC
C
D
unisim
FD
I34
Q
vme_enn
clk40
clr
D
CLK
CLR
Q
Common_lib
fd_behav
I38
vme_en
INIT = '0' (bit)
WR_REC
clk40
WR_REC
C
D
unisim
FD
I33
Q
vme_wr
eb4
4
-- eb3 3
-- open only if read access
vme_dis_rd <= not (vme_enn and (not vme_wr));
vme_dis_rd
width = 21 (integer)
ADDR
ADDR : (21:1)
clk40
clr
d : (width-1:0)
clk
clr
q : (width-1:0)
Common_lib
fd_vec
I32
vme_addr : (21:1)
IOBUF:
T= 1: IO=Z, O=X vme writing or inactive
T= 0: IO=I, O=I vme read
vdoo : (15:0)
vdii : (15:0)
vdout : (15:0)
vdin : (15:0)
g1: FOR i IN 0 TO 15 GENERATE
2
CAPACITANCE = "DONT_CARE" (string)
DRIVE = 12 (integer)
IOSTANDARD = "DEFAULT" (string)
SLEW = "SLOW" (string)
BIDIRECTIONAL
VME DATA BUS
VDATA
VDATA : (15:0)
VDATA(i) : (15:0)
IO
unisim
IOBUF
I12
T
I
O
vme_dis_rd
vdoo(i) : (15:0)
vdii(i) : (15:0)
INIT = '0' (bit)
Q
unisim
FD
I37
C
D
clk40
vdout(i) : (15:0)
clk40
INIT = '0' (bit)
C
D
unisim
FD
I36
Q
vdin(i) : (15:0)
RESERVEVME
RESERVEVME
I
unisim
IBUF
I11
O
Frame Declarations


dtack
vme_addr : (21:1)
vme_en
vme_wr
clk40
clr
dtack
vme_addr : (21:1)
vme_en
vme_wr
clk -- simulated
clr
rec_ca_lib
vme_decoder_recca
l22
vme_en_spy : (7:0)
vme_we_spy : (7:0)
rd_regs0_e : (7:0)
rd_regs10_1e : (7:0)
wr_regs10_1e : (7:0)
rd_regs20_2e : (7:0)
vme_rd_spy : (7:0)
wr_regsf0_fe : (7:0)
vme_en_spy : (7:0)
vme_we_spy : (7:0)
rd_regs0_e : (7:0)
rd_regs10_1e : (7:0)
wr_regs10_1e : (7:0)
rd_regs20_2e : (7:0)
vme_rd_spy : (7:0)
vdout : (15:0)
vdout : (15:0)
bcres_delay : (15:0)
max_bc_nr : (15:0)
bcr_delay : (15:0)
max_bc_nr : (15:0)
eb55
version_h <= X"0000";
version_l <= X"1005";
version_h : (15:0)
version_l : (15:0)
chip_id_h : (15:0)
chip_id_l : (15:0)
rec_status : (15:0)
bc_errors : (15:0)
spy_status0 : (15:0)
spy_status1 : (15:0)
spy_status2 : (15:0)
spy_status3 : (15:0)
orbit_nr : (31:0)
testmask0 : (15:0)
testmask1 : (15:0)
testmask2 : (15:0)
testmask3 : (15:0)
cmd_reg : (15:0)
-- simulated then changed
chip_id_h
chip_id_h : (15:0)
chip_id_l
chip_id_l : (15:0)
eb66
rec_status(15 downto 8) <= X"00";
rec_status(7) <= bc_error_flag;
rec_status(6) <= '0';
rec_status(5) <= stat_rec(1);
rec_status(4) <= stat_rec(0);
rec_status(3) <= simulating(3);
rec_status(2) <= simulating(2);
rec_status(1) <= simulating(1);
rec_status(0) <= simulating(0);
rec_status : (15:0)
vdout_m0 : (15:0)
vdout_m1 : (15:0)
vdout_m2 : (15:0)
vdout_m3 : (15:0)
vdout_m4 : (15:0)
vdout_m5 : (15:0)
vdout_m6 : (15:0)
vdout_m7 : (15:0)
vdout_ch0 : (15:0)
vdout_ch1 : (15:0)
vdout_ch2 : (15:0)
vdout_ch3 : (15:0)
vdout_ch4 : (15:0)
vdout_ch5 : (15:0)
vdout_ch6 : (15:0)
vdout_ch7 : (15:0)
rec_ca_lib
vme_reg_recca
l39
vdin : (15:0)
clk40
clr
vdin : (15:0)
clk
clr
V1004: spy_status(15:0)...new
V1005: orbit_nr_h/l
VME decoder
VME registers

STATUS Encoder

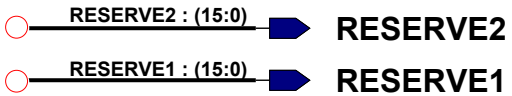
```
-- 00 REC chip is DISCONNECTED  … default status when READY=0 & after power up
-- 01 REC chip is BUSY          … during transfer of test data  <== 'simulating=1'
-- 10 REC chip is READY         … when CMD_REG(4) is set =1
-- 11 REC chip is ERROR         … error status after enabled bc_error
```




```
cmd_reg
(3:0) simu_mode
 4: REC_IS_READY
 5: EN_BC_ERROR
```

Spare signals are unused

```
eb7
7
-- eb6 6
RESERVE2 <= (others => '0');
RESERVE1 <= (others => '0');
```

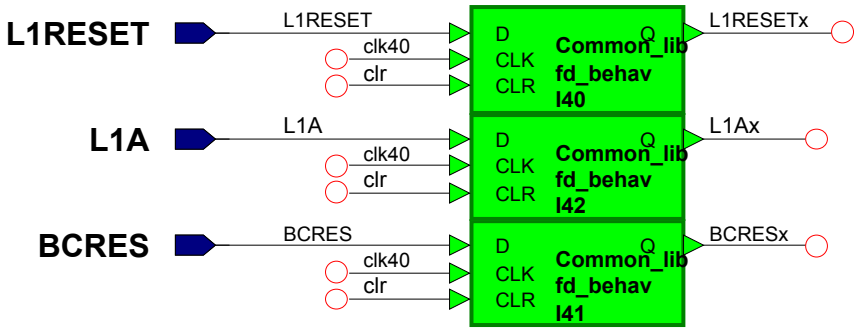


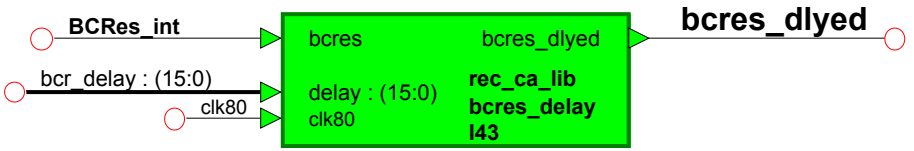
```
SIGNAL vme_en_spy      : std_logic_vector(7 DOWNTO 0) -- to mem's
SIGNAL vme_enn         : std_ulogic
SIGNAL vme_rd_spy      : std_logic_vector(7 DOWNTO 0) -- to vme read mux
SIGNAL vme_we_spy      : std_logic_vector(7 DOWNTO 0) -- to mem's
SIGNAL vme_wr          : std_logic
SIGNAL wr_regs10_1e    : std_logic_vector(7 DOWNTO 0)
SIGNAL wr_regsf0_fe    : std_logic_vector(7 DOWNTO 0)
```

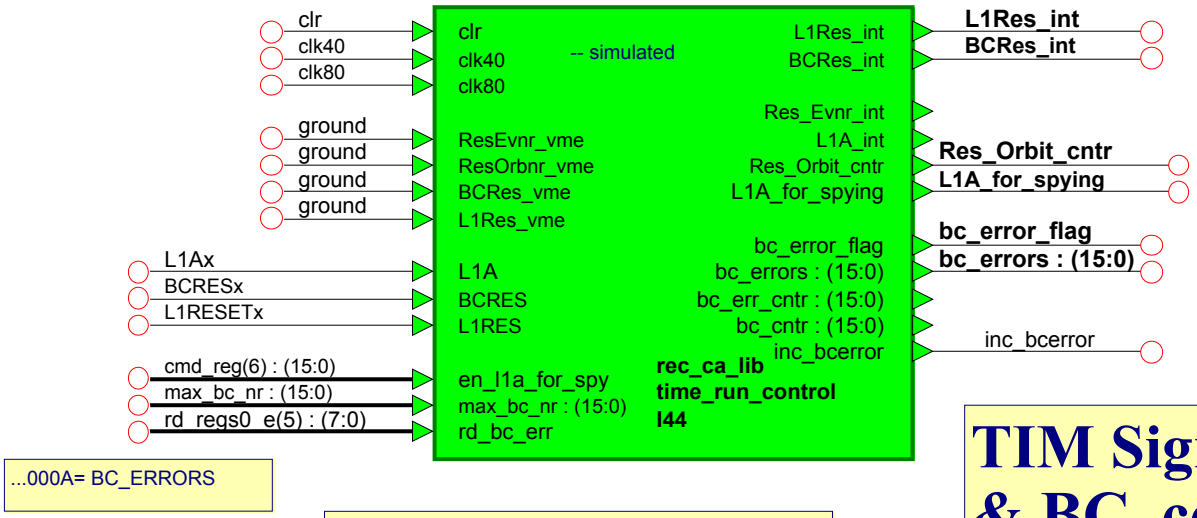
Because of fatal error in ModelSim
I inserted the Xilinx52 defaultvalues
with CLKIN_PERIOD 23.000 as in PSB chip.
Since then Modelsim runs without fatal error.

```
TimingChecksOn                        = true                  ( boolean          )
InstancePath                          = "*"                   ( string           )
Xon                                   = true                  ( boolean          )
MsgOn                                 = false                 ( boolean          )
thold_PSEN_PSCLK_negedge_posedge      = 0.010 ns              ( VitalDelayType   )
thold_PSEN_PSCLK_posedge_posedge      = 0.010 ns              ( VitalDelayType   )
thold_PSINCDEC_PSCLK_negedge_posedge  = 0.010 ns              ( VitalDelayType   )
thold_PSINCDEC_PSCLK_posedge_posedge  = 0.010 ns              ( VitalDelayType   )
tipd_CLKFB                            = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_CLKIN                            = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_DSSEN                            = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_PSCLK                            = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_PSEN                             = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_PSINCDEC                         = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tipd_RST                              = (0.000 ns, 0.000 ns)  ( VitalDelayType01 )
tpd_CLKIN_LOCKED                      = (0.100 ns, 0.100 ns)  ( VitalDelayType01 )
tpd_PSCLK_PSDONE                      = (0.100 ns, 0.100 ns)  ( VitalDelayType01 )
tperiod_CLKIN_POSEDGE                 = 1.111 ns              ( VitalDelayType   )
tperiod_PSCLK_POSEDGE                 = 1.111 ns              ( VitalDelayType   )
tpw_CLKIN_negedge                     = 0.010 ns              ( VitalDelayType   )
tpw_CLKIN_posedge                     = 0.010 ns              ( VitalDelayType   )
tpw_PSCLK_negedge                     = 0.010 ns              ( VitalDelayType   )
tpw_PSCLK_posedge                     = 0.010 ns              ( VitalDelayType   )
tpw_RST_posedge                       = 0.010 ns              ( VitalDelayType   )
tsetup_PSEN_PSCLK_negedge_posedge     = 0.010 ns              ( VitalDelayType   )
tsetup_PSEN_PSCLK_posedge_posedge     = 0.010 ns              ( VitalDelayType   )
tsetup_PSINCDEC_PSCLK_negedge_posedge = 0.010 ns              ( VitalDelayType   )
tsetup_PSINCDEC_PSCLK_posedge_posedge = 0.010 ns              ( VitalDelayType   )
CLKDV_DIVIDE                          = 2.0                   ( real             )
CLKFX_DIVIDE                          = 1                     ( integer          )
CLKFX_MULTIPLY                        = 4                     ( integer          )
CLKIN_DIVIDE_BY_2                     = false                 ( boolean          )
CLKIN_PERIOD                          = 23.000                ( real             )
CLKOUT_PHASE_SHIFT                    = "NONE"                ( string           )
CLK_FEEDBACK                          = "1X"                  ( string           )
DESKEW_ADJUST                         = "SYSTEM_SYNCHRONOUS"  ( string           )
DFS_FREQUENCY_MODE                    = "LOW"                 ( string           )
DLL_FREQUENCY_MODE                    = "LOW"                 ( string           )
DSS_MODE                              = "NONE"                ( string           )
DUTY_CYCLE_CORRECTION                 = true                  ( boolean          )
FACTORY_JF                            = X"C080"               ( bit_vector       )
MAXPERCLKIN                           = 1000000 ps            ( time             )
MAXPERPSCLK                           = 100000000 ps          ( time             )
PHASE_SHIFT                           = 0                     ( integer          )
SIM_CLKIN_CYCLE_JITTER                = 300 ps                ( time             )
SIM_CLKIN_PERIOD_JITTER               = 1000 ps               ( time             )
STARTUP_WAIT                          = false                 ( boolean          )
```

BCRES Delay



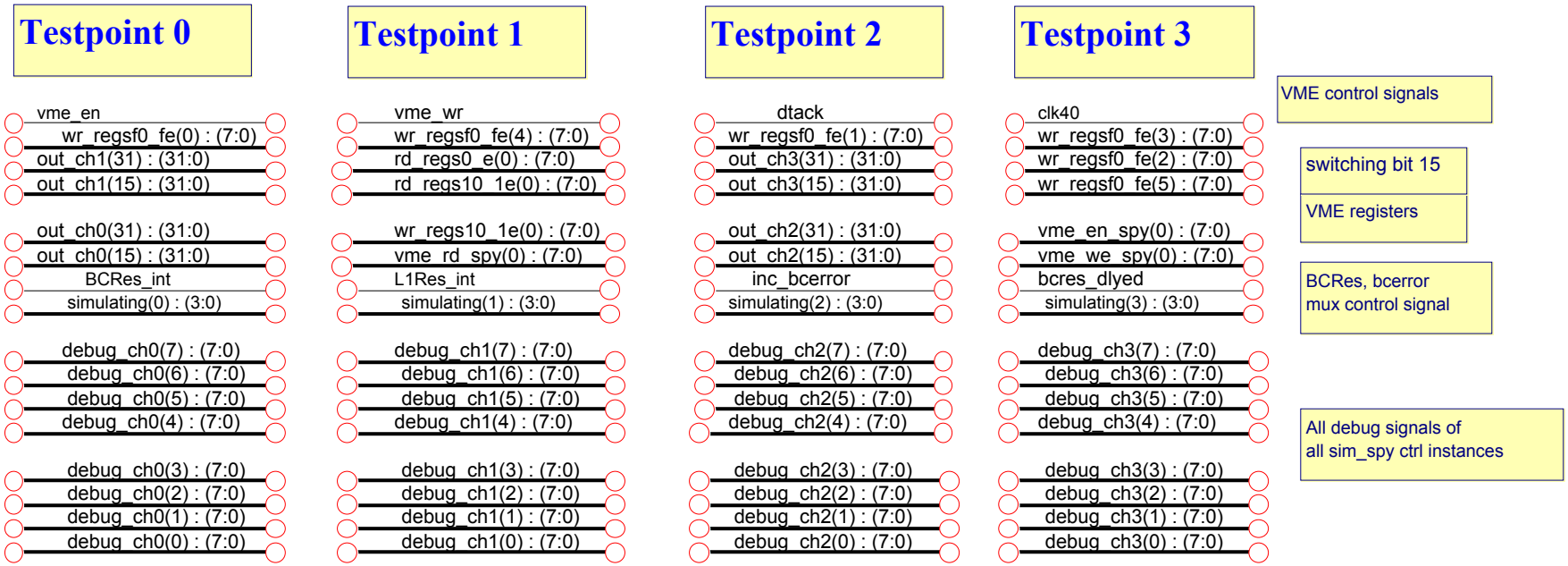




...000A= BC_ERRORS

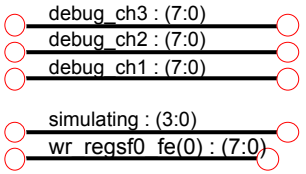
Res_Evnr_int, L1A_int, Res_Orbitnr_int,
inc_bcerror
go to Testpoints only to check backplane signals.

TIM Signal Decoder & BC_counter & bc_error counter



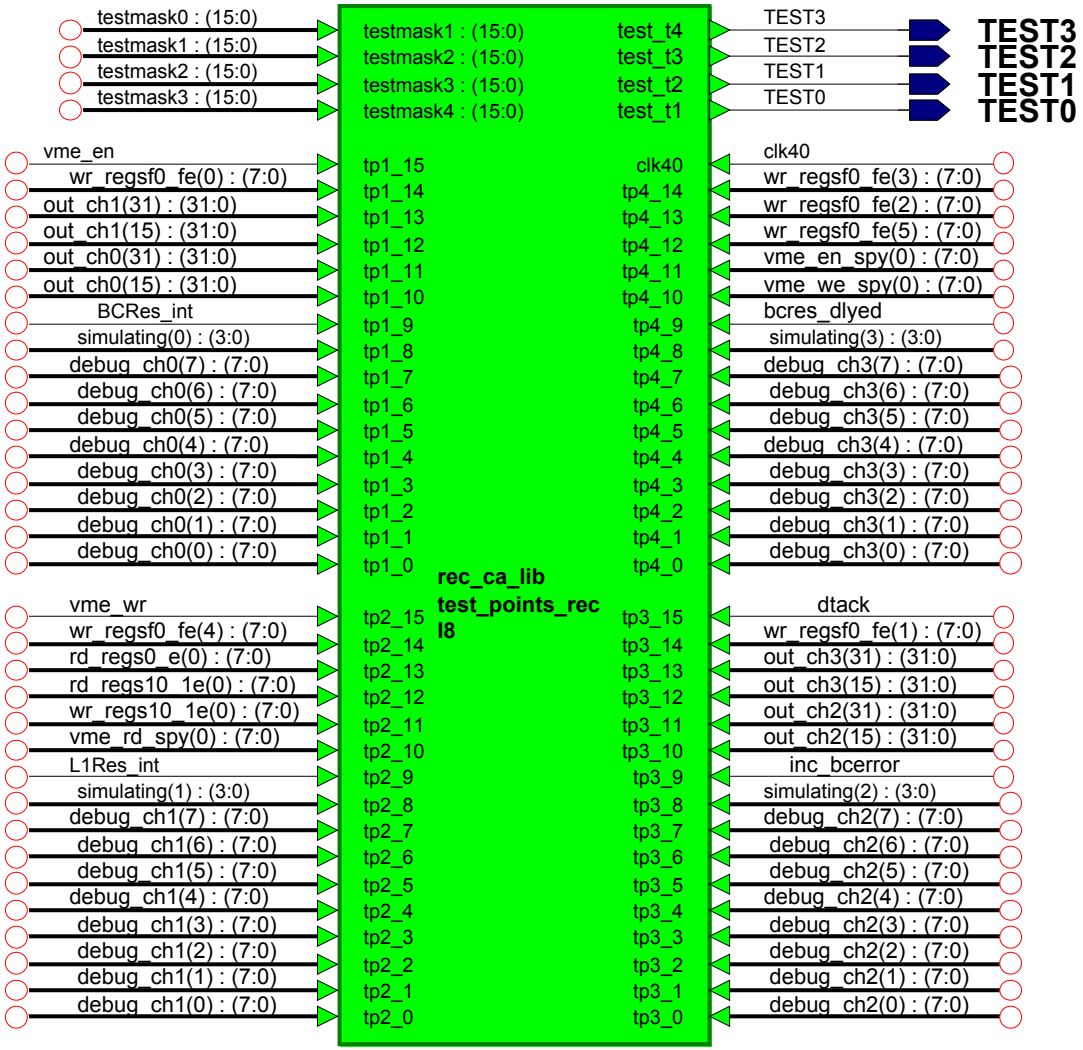
Debug signals from sim_spy control:

```
debug(7) <= start_syy;
debug(6) <= stop_syy;
debug(5) <= start_syuend;
debug(4) <= stop_syuend;
debug(3) <=  set_ensimspy;
debug(2) <=  clr_ensimspy;
debug(1) <= stop_syncff;
debug(0) <= stop_syncff1;
```




```
run_v              <= wr_regsf0_fe(0);  -- start immediately and run without stopping
run_v_u_end      <= wr_regsf0_fe(1);  -- start immediately and run 1x until end of memory
run_sync           <= wr_regsf0_fe(2);  -- start at begin of orbit and run without stopping
run_sync_u_end <= wr_regsf0_fe(3);  -- start at begin of orbit and run 1x until end of orbit
stop_v             <= wr_regsf0_fe(4);  -- stop immediately
stop_sync          <= wr_regsf0_fe(5);  -- stop at end of orbit
stop_spying_with_next_L1A  <= wr_regsf0_fe(4);  -- L1A stops immediately
```

-- not simulated, copied from tim_chip



TESTPOINTS

V1004: Stop spying with L1A, SPY_STATUS registers
V1005: ORBIT counter

Declarations

Ports:

```
L1A_for_spying   : std_logic
Res_Orbit_cntr   : std_logic
bc_res_dlyd      : std_logic
clk40            : std_logic
clk80            : std_logic
clr              : std_logic
din              : std_logic_vector(15 DOWNTO 0)
res_orb_with_bcr : std_logic
simu_mode        : std_logic
vaddr            : std_logic_vector(21 DOWNTO 1)
vdin             : std_logic_vector(15 DOWNTO 0)
vme_en_spy       : std_logic
vme_we_spy       : std_logic
wr_regsf0_fe     : std_logic_vector(7 DOWNTO 0)
dout             : std_logic_vector(15 DOWNTO 0)
orbit_nr         : std_logic_vector(31 DOWNTO 0)
s_debug          : std_logic_vector(7 DOWNTO 0) -- debug output
simulating       : std_logic
spy_status       : std_logic_vector(15 DOWNTO 0)
vdout_spy        : std_logic_vector(15 DOWNTO 0)
```

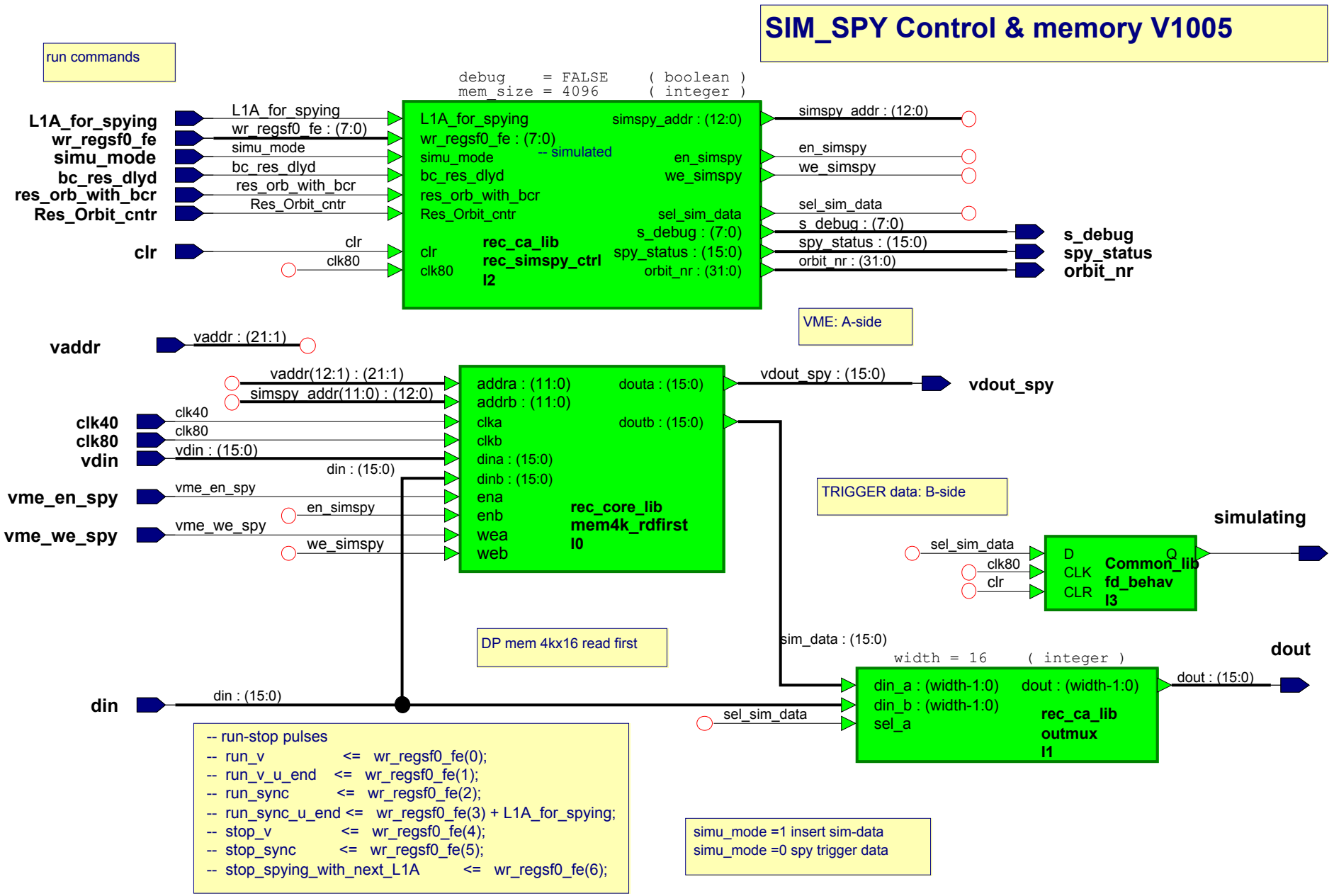
Diagram Signals:

```
SIGNAL en_simspy        : std_logic
SIGNAL sel_sim_data     : std_logic
SIGNAL sim_data         : std_logic_VECTOR(15 DOWNTO 0)
SIGNAL simspy_addr      : std_logic_vector(12 DOWNTO 0)
SIGNAL we_simspy        : std_logic
```

Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.STD_LOGIC_UNSIGNED.all;
```

<company name>		Project:	rec_ca
		<enter comments here>	
Title:	<enter diagram title here>		
Path:	rec_ca_lib/rec_channel/struct		
Edited:	by taurok on 23 Aug 2006		


SIM_SPY Control & memory V1005
run commands
debug = FALSE (boolean)
mem_size = 4096 (integer)
L1A_for_spying
wr_regsf0_fe
simu_mode
bc_res_dlyd
res_orb_with_bcr
Res_Orbit_cntr
clr
clk80
simspy_addr : (12:0)
en_simspy
we_simspy
sel_sim_data
s_debug : (7:0)
spy_status : (15:0)
orbit_nr : (31:0)
-- simulated
rec_ca_lib
rec_simspy_ctrl
I2
s_debug
spy_status
orbit_nr
VME: A-side
vaddr
vaddr : (21:1)
vaddr(12:1) : (21:1)
simspy_addr(11:0) : (12:0)
addra : (11:0)
addrb : (11:0)
clka
clkb
dina : (15:0)
dinb : (15:0)
ena
enb
wea
web
douta : (15:0)
doutb : (15:0)
vdout_spy : (15:0)
vdout_spy
clk40
vdin : (15:0)
din : (15:0)
vme_en_spy
vme_we_spy
rec_core_lib
mem4k_rdfirst
I0
TRIGGER data: B-side
simulating
D
CLK
CLR
Q
Common_lib
fd_behav
I3
DP mem 4kx16 read first
sim_data : (15:0)
dout
width = 16 (integer)
din_a : (width-1:0)
din_b : (width-1:0)
sel_a
dout : (width-1:0)
dout : (15:0)
rec_ca_lib
outmux
I1
-- run-stop pulses
-- run_v <= wr_regsf0_fe(0);
-- run_v_u_end <= wr_regsf0_fe(1);
-- run_sync <= wr_regsf0_fe(2);
-- run_sync_u_end <= wr_regsf0_fe(3) + L1A_for_spying;
-- stop_v <= wr_regsf0_fe(4);
-- stop_sync <= wr_regsf0_fe(5);
-- stop_spying_with_next_L1A <= wr_regsf0_fe(6);
simu_mode =1 insert sim-data
simu_mode =0 spy trigger data