Global Trigger Logic Module

B. Arnold, H. Bergauer, M. Eichberger, K. Kastner, B. Neuherz, M. Padrta, T. Schreiner, A. Taurok

HEPHY Vienna, Austria

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Revision 1.2

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1 General description

1.1 Document updates

1.1.1 Revision 1.2

Description of ALGO_BX_EN-memories added (February 1, 2012).

1.1.2 Revision 1.1

Corrections in tables for "Bit assignments on GT Calorimeter channel 10 (CA10)", because of PSB-chip version V100C changes on LVDS signals "mapping" (April 20, 2010).

1.1.3 Revision 1.0

Updates in firmware for correlation conditions with HtMiss (March 9, 2010).

1.1.4 Revision 0.0

First design with status of hard- and firmware of March 10, 2009.

1.2 Summary of hardware changes

1.2.1 Revision 2.0

Max. 192 algorithms possible, but only 128 are send to FDL-board (4 cables with 32 bits), because FDL can only use this number of algorithms now (March 10, 2009).

1.2.2 Revision 1.0

Errors in basic design therefore following changes made:

- Pull-up resistor (10kΩ, 1/8W) on NSYSRES_I signal.
- Pull-up resistor (10kΩ, 1/8W) on NSYSRES_VME signal.
- Additional capacitor (100nF, C0805) parallel to R172 (10kΩ, R0805) - against „spikes" on NSYSRES signal.
- Termination resistors (R114, R115, R116 and R223) for TTC-signals from backplane not inserted.
- Instead of R77 and R80 (10kΩ) solder-bridges are inserted.

1.2.3 Revision 0.0

Basic design for GTL-9U module.

1.3 Overview

The GTL-9U Module is part of the Global Trigger System of the CMS Experiment. It woks as a VME64x-bus slave.
The module receives 10 channels of calorimeter particle data and muons from the backplane in the Receiver Chips (devices of XILINX® company). The Condition Chips (devices of ALTERA® company) contain the conditions and algorithms to calculate the triggers, the algorithm-bits are send to the FDL-9U Module. Both the Receiver Chips and the Condition Chips have sim/spy memories (via VME) for tests.
Configuration of the Condition Chips and Receiver Chips (FPGAs) is done via JTAG.

1.4 Block diagram

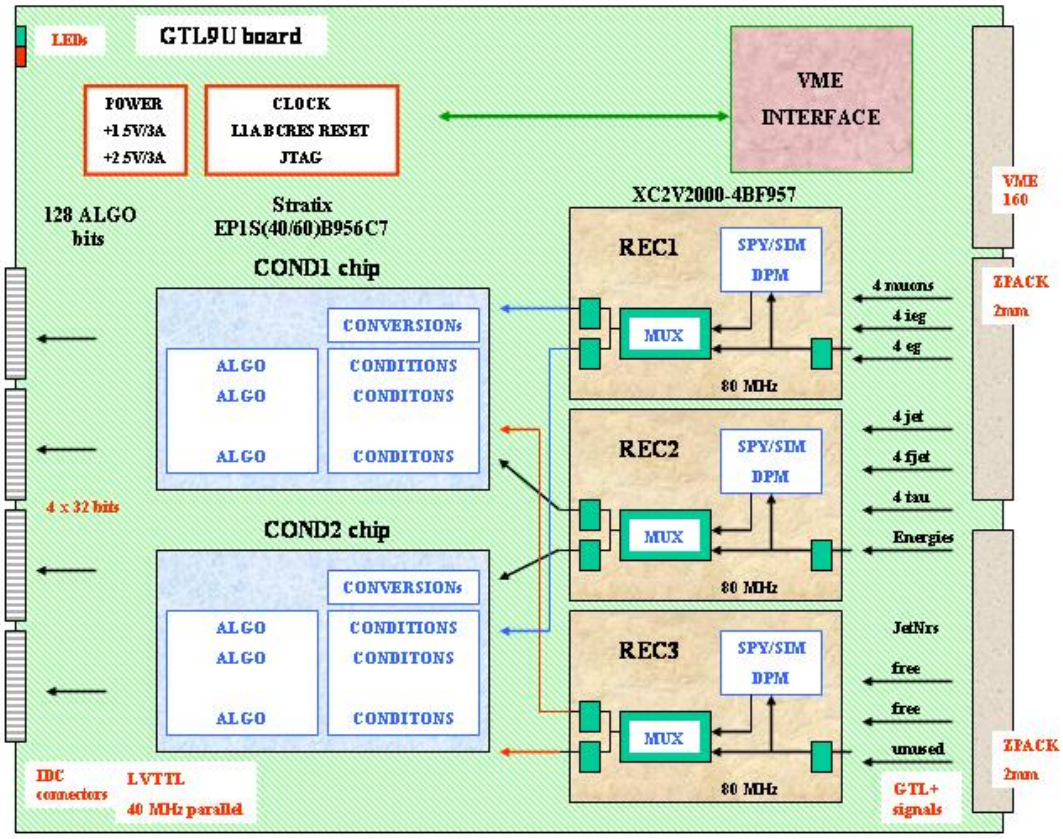

Figure 1.1: Block diagram of GTL-9U Module

1.5 Features

- Max. 192 algorithms possible.
- VME interface with two FPGAs (VME64x- and VME-GTL-chip, ALTERA devices).
- VME access to registers and memories.
- Condition Chips and Receiver Chips have sim/spy memories (via VME) for tests.
- Configuration of PROMs of FPGAs and FPGAs with ALTERA and XILINX cables.
- "JTAG over VME" for configuration of PROMs of FPGAs.
- Configuration of Condition Chips (FPGAs) via VME.
- BCRES, L1A and Status-bits features of Trigger-Control-System.
- Hot-swap-able module.

2 Technical specifications

2.1 Packaging

The GTL-9U Module is a 1-unit wide 9U high VME64x module with ZPACK connectors to the backplane of the Global Trigger System rack.

2.1.1 Serial number and Card number

The serial number of the module in the VME64x system is "GTLx", where x is the card number of the module, which runs from 1 to 4.

2.1.2 Backplane coding

The coding for the GTL-9U Module is "pastell orange - 1247" at the 2mm-connector type A. The module has to be inserted in slot 11 or 12 in the Global Trigger System rack, default is slot 11.

2.2 Power requirements

Power	Name	Current	Remarks
+5V	VCC	? A	from backplane
+3,3V	LV3V3	? A	from backplane
+2,5V	LV2V5_VME	? A	onboard
+1,5V	LV1V5_COND1	? A	onboard
+1,5V	LV1V5_COND2	? A	onboard
+1,5V	LV1V5_XIL	? A	onboard

Table 2.1: Power requirements

2.3 External components

The location of the components is shown in 2.4 Front panel.

2.3.1 Buttons

ON: Press ON button to set module in RUNNING state.
OFF: Press OFF button to set module in INACTIVE state (hot-swap-able).

2.3.2 LEDs

OFF: module is in INACTIVE state (red LED).
ON: module is in RUNNING state (green LED).
LOCK: all FPGAs are in LOCKED state (green LED).
FPGA: all FPGAs are configured (green LED).
VME: a VME access is done (green LED).

2.3.3 Connectors

TEST: LEMO 00 connector, output LVTTL, I_O = 24mA.
(Buffered TEST0 output of COND1-chip. Default signal on TEST0 is CLK40).

ALGO00-191: six connectors (ERNI - SMC Type B right angle male connector, 68 contacts, Part Number 114805), outputs LVTTL.
(These six connections send the 192 algorithm-bits to the FDL-9U Module).

2.3.4 Cables

ALGO00-191: six cables with ERNI - SMC Type B female connector, SKV 68 contacts, Part Number 124263.

2.4 Front panel

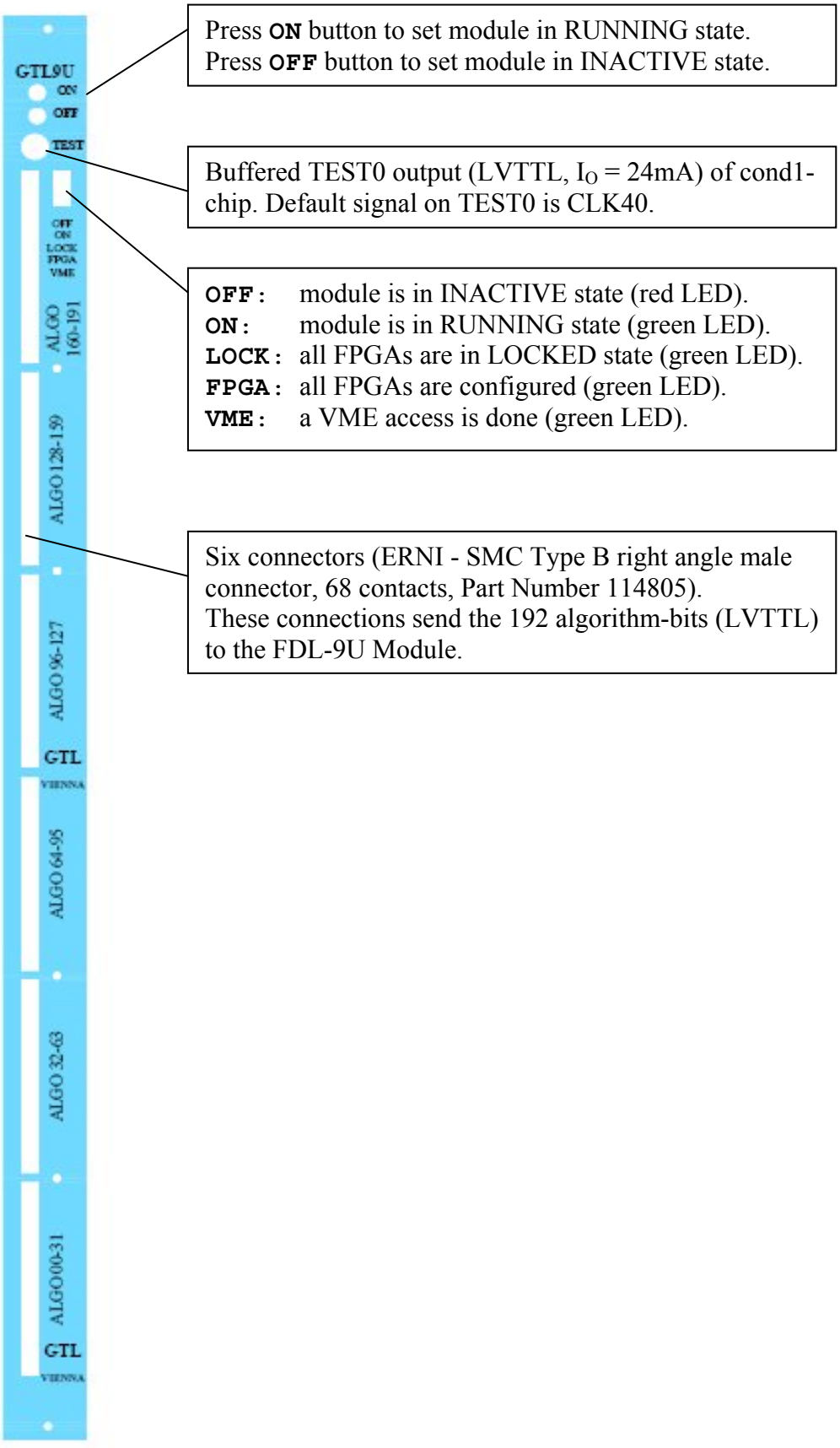

Figure 2.1: Front panel

2.5 Internal hardware components

2.5.1 Jumpers

The description of the jumpers is made in 6.2 Jumper settings.

2.5.2 Switches

No switches on GTL-9U module.

2.6 Programming and configuring of FPGAs

2.6.1 General

The PROMs of the VME64x- and VME-GTL Chips (FPGAs) contain a fixed firmware, updates are made by experts.
The Condition Chips and Receiver Chips are FPGAs too, the methods of programming and configuration are listed below. Each FPGA has one or more PROMs, which contain the firmware. Configuration cycles are started after power-up or by a VME-instruction.

2.6.2 Generation of Firmware

The generation of the firmware of VME64x-, VME-GTL- and Receiver Chips is made by experts.
For the Condition Chips it is necessary, to have "fast" updates of the firmware, because of the changes in the requirements on the trigger, so it exists a software-tool called L1-Trigger-Menu-Editor (TME) in the Trigger-Supervisor environment (TS) to edit the trigger-algorithms and to be able to generate all the files (VHDL and others), which are used from ALTERA Quartus software to make the programming files.

2.6.3 Methods of programming and configuring

Different methods are implemented to program and configure the FPGAs and their PROMs.

2.6.3.1 Programming Cables

Both, ALTERA and XILINX provide programming cables, to bring the firmware into the FPGAs/PROMs. JTAG-chains are used for this method. For the ALTERA devices one can use the cables "MasterBlaster" or "ByteBlasterII", for XILINX devices "Parallel-Cable IV". ALTERA SOF/POF-files and XILINX MCS-files are used as programming/configuring files.

2.6.3.2 JTAGoverVME

A method, which can be used without external cables is "JTAGoverVME", it means that the firmware is loaded by VME accesses into the FPGAs/PROMs via the JTAG-chains. Therefore SVF-files are used as programming/configuring files.

2.6.3.3 Programming via VME

Programming via VME means that the firmware is loaded by VME accesses into the FPGAs via the configuration pins of the FPGAs. After power-down the information is lost. This method is not possible for PROMs. ALTERA RBF-files are used as programming files.

2.6.4 JTAG-chains

On the GTL-9U Module there are two JTAG-chains implemented, one for ALTERA devices and one for XILINX devices.

2.6.4.1 Default settings of JTAG-chains

ALTERA-chain	Device	Status	Jumper	Pins
VME64x-chip	EP1K10QC208	OUT	JP40	2-3
PROM VME64x-chip	EPC2	OUT	JP41	2-3
VME-GTL-chip	EP1K100QC208	OUT	JP42	2-3
PROM VME-GTL-chip	EPC2	OUT	JP43	2-3
PROM COND1-chip	EPC16	IN	JP44	1-2

COND1-chip	MEZZ1020	OUT	JP45	2-3
PROM COND2-chip	EPC16	IN	JP46	1-2
COND2-chip	MEZZ1020	OUT	JP47	2-3

Table 2.2: Default JTAG-chain for ALTERA devices

XILINX-chain	Device	Status	Jumper	Pins
4 x PROM REC3-chip	XC18V04	IN	JP49-JP52	1-2
REC3-chip	MEZZ957	IN *)	JP48	1-2
4 x PROM REC2-chip	XC18V04	IN	JP53-JP56	1-2
REC2-chip	MEZZ957	IN *)	JP57	1-2
4 x PROM REC1-chip	XC18V04	IN	JP59-JP62	1-2
REC1-chip	MEZZ957	IN *)	JP58	1-2

*) RECx-chips must always be in JTAG-chain, because TMS-signal could not be disabled - no jumper on TMS-signal for RECx-chips.

Table 2.3: Default JTAG-chain for XILINX devices

2.7 Technical specifications table

Packaging	1-unit wide 9U high VME64x module with ZPACK connectors to the backplane
VME64x	F0 and F1 used A32 D08, D16 for R/W D16 for BLT
Backplane connections	ZPACK-2mm-connectors
FPGA configuration	Programming cables, JTAGoverVME, Programming via VME
LED display	ON, OFF, LOCK, FPGA, VME
Panel outputs	1 LEMO 00 (LVTTL), 6 IDC connectors 68 contacts (LVTTL)

Table 2.4: GTL-9U Module technical specification

3 Hardware

3.1 Interface definitions

3.1.1 VME64x-interface

The connection to the VME64x-bus of the GT-system is made with connector VME64_P12 which contains all signals from the J1/P1 and J2/P2 connectors of a standard VME64x-bus system. The description of the signals one can find in the VMEbus Specification Manual [5], American National Standard for VME64 [1] and American National Standard for VME64 Extensions [2] (see 7 References).

Pin Number	Z Signal Mnemonic	A Signal Mnemonic	B Signal Mnemonic	C Signal Mnemonic	D Signal Mnemonic
1	GND	D00	BBSY* (1)	D08	+3,3V BIAS
2	+3,3V	D01	BCLR* (1)	D09	GND
3	+3,3V	D02	ACFAIL* (1)	D10	RETRY*
4	+3,3V	D03	+1,8V (1)	D11	A24
5	GND	D04	+1,8V (1)	D12	A25
6	+3,3V	D05	+1,8V (1)	D13	A26
7	+3,3V	D06	+1,8V (1)	D14	A27
8	+3,3V	D07	+1,8V (1)	D15	A28
9	+3,3V	GND	+1,8V (1)	GND	A29
10	+3,3V	SYSCLK (1)	+1,8V (1)	SYSFAIL* (1)	A30
11	+3,3V	GND	+1,8V (1)	BERR*	A31
12	+3,3V	DS1*	+1,8V (1)	SYSRESET*	GND
13	GND	DS0*	+1,8V (1)	LWORD*	+5V
14	+3,3V	WRITE*	+1,8V (1)	AM5	D16 (1)
15	+3,3V	GND	+1,8V (1)	A23	D17 (1)
16	+3,3V	DTACK*	AM0	A22	D18 (1)
17	GND	GND	AM1	A21	D19 (1)
18	+2,5V (1)	AS*	AM2	A20	D20 (1)
19	+2,5V (1)	GND	AM3	A19	D21 (1)
20	+2,5V (1)	IACK*	GND	A18	D22 (1)
21	GND	IACKIN*	SERCLK (1)	A17	D23 (1)
22	+2,5V (1)	IACKOUT*	SERDAT* (1)	A16	GND
23	+2,5V (1)	AM4	GND	A15	D24 (1)
24	+2,5V (1)	A07	GA0*	A14	D25 (1)
25	GND	A06	GA1*	A13	D26 (1)
26	+2,5V (1)	A05	GA2*	A12	D27 (1)
27	+2,5V (1)	A04	GA3*	A11	D28 (1)
28	+2,5V (1)	A03	GA4*	A10	D29 (1)
29	+2,5V (1)	A02	GAP*	A09	D30 (1)
30	GND	A01	IRQ1*	A08	D31 (1)
31	+5V	-12V (1)	+5V STBY (1)	+12V (1)	GND
32	+5V	+5V	+5V	+5V	+5V BIAS

(1) not used on GTL-9U Module.

Table 3.1: VME64_P12 Pin assignment (VME64x-connector with 160 pins)

4 Firmware

4.1 Definitions of conditions in condition-chips

4.1.1 Calorimeter conditions

Calorimeter object definition:
Isolated electron/photon objects
Non-isolated electron/photon objects
Central jet objects
Forward jet objects
Tau-flagged jet objects
(Energy summary information conditions and Ring Rapidity conditions are described in chapters below)

The calorimeter trigger processing identifies and sorts electron/photon and jet candidates. The four highest ranked candidates in each category are passed to the GT for each event. For each selected candidate, the GCT sends rank and position information encoded in fifteen bits: six bits rank, four bits pseudorapidity (η) position, five bits azimuth angle (φ) position. The rank information generally represents a coding of the object Et, with the definition of the rank assignments programmable within the calorimeter trigger logic. The objects are sorted by rank within the GCT, so that object 1 is the highest ranked object, object 2 the second highest ranked, and so on.
The φ position ranges from 0 to 17 and defines a 20° sector. The η position is coded as three bits value plus a sign bit. For objects other than forward jets, the η regions are of size $\Delta\eta \approx 0.35$ with regions 0-3 in the barrel part of CMS, 4-6 in the endcap. For forward jets, the η value ranges from 0-3. The size of the η regions is $\Delta\eta = 0.5$ and the range covered is $3 < |\eta| < 5$.

The selection of the rank-comparator (greater/equal or equal) and the Et-threshold-value are set in VME-registers. The ranges for η and φ are set in look-up-tables.

Because of the four candidates there are different types of conditions implemented, depending of how many candidates have to fulfil the templates (thresholds and ranges).
1. four particle condition (cond_4)
2. two particle condition, "simple" (cond_2_s)
3. two particle condition, with spatial correlation (cond_2_wsc)
4. one particle condition (cond_1_s)

The following equation is used for calorimeter conditions:

```
Et rank over threshold AND eta in range AND phi in range
```

Cond_4: every one of the four candidates has to fulfil the equation at least with one template, totally all four templates must be fulfilled.
Cond_2_s: two of the four candidates have to fulfil the equation at least with one, but different template.
Cond_2_wsc: two of the four candidates have to fulfil the equation at least with one, but different template. In addition the correlation in η and φ of the two candidates must be fulfilled.
Cond_1_s: one of the four candidates has to fulfil the equation at least with one template.

4.1.2 Muon conditions

The four muons are sorted by rank. The muon with the highest rank is sent on channel 1, the one with the lowest rank on channel 4. If fewer than 4 particles are found, the channels for

lower ranks are empty. Empty channels contain all 0 or at least pT=0. One muon candidate is represented by 26 bits:
Res = reserved for future use
SY_SIGN = sign of charge or synchronization code (2 bits)
MIP = Minimum Ionizing Particle bit (muon was confirmed by calorimeter)
ISO = Isolation bit (muon was isolated)
ETA = pseudorapidity: 6 bits (MSB is pseudo-sign)
QU = 3 quality bits
PT = transverse momentum, 5 bits
PHI = azimuthal angle, 8 bits
(For more details see: [4] CMS Internal Note, Specification of the Interface between the Global Muon Trigger and the Global Trigger, CMS IN 2004/006, January 12, 2004)

Because of the four candidates there are different types of conditions implemented, depending of how many candidates have to fulfil the templates (thresholds and ranges).
1. four particle condition (cond_4)
2. two particle condition, "simple" (cond_2_s)
3. two particle condition, with spatial correlation (cond_2_wsc)
4. one particle condition (cond_1_s)
5. three particle condition (cond_3)

The PT truth-table is used for all muon condition types.

muon_data				**condition bits**				
PT equal high threshold	**PT greater/equal high threshold**	**PT greater/equal high threshold**	**ISO_ bit of muon**	**greater/equal selection**	**request_iso**	**enable_iso**	**PT truth-table output**	**comments**
0	x	x	x	0	x	x	0	for tests
1	x	x	x	0	x	x	1	for tests
x	0	0	x	1	x	x	0	very low p_T muon
x	0	1	0	1	0	0	1	ignore isolation, take it
x	0	1	0	1	0	1	0	not isolated
x	0	1	0	1	1	x	0	not isolated
x	0	1	1	1	0	0	1	ignore isolation, take it
x	0	1	1	1	0	1	1	take isolated muon
x	0	1	1	1	1	x	1	take isolated muon
x	1	1	0	1	0	x	1	ignore isolation, take it
x	1	1	0	1	1	x	0 *)	requested but not isolated
x	1	1	1	1	x	x	1	take isolated muon
x	1	0	x	1	x	x	not used **)	must be inhibited by GUI

*) Because of request_iso = 1 do not trigger on a very high pT, but non isolated muon.
**) Low-threshold for pT must not be greater than high-threshold for pT.

Table 4.1: Muon PT truth-table

The following equation is used for calorimeter conditions cond_4, cond_2_s, cond_1_s and cond_3:

```
PT truth-table AND ETA in range AND PHI in range AND QU matched AND MIP
matched
```

Cond_4: every one of the four candidates has to fulfil the equation at least with one template, totally all four templates must be fulfilled, and in addition the charge condition must matched.

Cond_2_s: two of the four candidates have to fulfil the equation at least with one, but different template, and in addition the charge condition must matched.
Cond_2_wsc: two of the four candidates have to fulfil the equation at least with one, but different template. In addition the correlation in η and φ of the two candidates and the charge condition must be fulfilled.
Cond_1_s: one of the four candidates has to fulfil the equation at least with one template, and in addition the charge condition must matched.
Cond_3: three of the four candidates have to fulfil the equation at least with one, but different template, and in addition the charge condition must matched.

4.1.3 Energy summary information conditions

The energy sum information consists of the four quantities total Et, total calibrated Et in jets (Ht), missing Et and missing Ht.

4.1.3.1 Total Et and Ht condition (ett, htt)

Both total Et and Ht are sent as 12-bit value plus an overflow bit on a programmable, linear energy scale.
The selection of the magnitude-comparator (greater/equal or equal) and the threshold-value are set in VME-registers.

The following equation is used for total Et and Ht conditions:

```
(ET magnitude over threshold AND NOT ET magnitude overflow) OR (ET
magnitude overflow)
```

The implementation in VHDL-code was made with:

```
out_reg_1 <= (NOT ge_eq_sel AND out_aeqb AND NOT ov_bit) -- "equal trigger"
             OR
             (ge_eq_sel AND out_ageb AND NOT ov_bit) -- "greater-equal trigger"
             OR
             (ge_eq_sel AND ov_bit); -- "OV trigger"
```

4.1.3.2 EtMiss and HtMiss condition (etm, htm)

Missing Et is sent as a 2-vector with both magnitude and azimuthal direction. The magnitude is encoded in 12 bits plus an overflow bit; the direction is a 7-bit value between 0-71.
The zero and sense of rotation of the azimuth angle are the same as for the object data, with four bins of EtMiss_phi corresponding to one bin of Object_phi.
Missing Ht is sent as a 2-vector with both magnitude and azimuthal direction. The magnitude is encoded in 7 bits plus an overflow bit; the direction is a 5-bit value between 0-17.
The zero and sense of rotation of the azimuth angle and the number of bins are the same as for the object data.
The selection of the magnitude-comparator (greater/equal or equal) and the threshold-value are set in VME-registers. The range for phi is set in a look-up-table.

The following equation is used for missing Et and Ht conditions:

```
(ETM magnitude over threshold AND NOT ETM magnitude overflow AND ETM phi in
non-trivial range) OR (ETM magnitude overflow)
```

The implementation in VHDL-code is made with:

```
out_reg_1 <= (NOT ge_eq_sel AND out_aeqb AND phi_ok AND NOT ov_bit) -- "equal trigger"
             OR
             (ge_eq_sel AND out_ageb AND phi_ok AND NOT ov_bit) -- "greater-equal trigger"
             OR
             (ge_eq_sel AND ov_bit); -- "OV trigger"
```

4.1.4 Ring Rapidity conditions

Ring Rapidity is sent in 3 bits for eight rings (regions). The threshold-values are set in VME-registers. Comparators work on greater/equal only.
Ring Rapidity condition types:
ring_1_pos_rap_hf
ring_1_neg_rap_hf
ring_2_pos_rap_hf
ring_2_neg_rap_hf
ring_1_pos_rap_ etsums
ring_1_neg_rap_ etsums
ring_2_pos_rap_ etsums
ring_2_neg_rap_ etsums

4.1.5 Correlation conditions

The Correlation conditions consist of a combination of an “one particle condition” of two different calorimeter objects, or one calorimeter object and muon, or one calorimeter object and missing Et (etm), or one calorimeter object and missing Ht (htm), or muon and etm, or muon and htm, or etm and htm. In addition with both particle conditions there are correlations in η and φ (with etm and htm only in φ).
Correlation condition types:
muon_ieg
muon_eg
muon_cjet
muon_fjet
muon_tau
ieg_eg
ieg_cjet
ieg_fjet
ieg_tau
eg_cjet
eg_fjet
eg_tau
cjet_fjet
cjet_tau
fjet_tau
etm_muon
etm_ieg
etm_eg
etm_cjet
etm_fjet
etm_tau
htm_muon
htm_ieg
htm_eg
htm_cjet
htm_fjet
htm_tau
htm_etm

4.1.6 External conditions

The 64 External Conditions data arrive through the so-called "GT calorimeter input channel #10 (CA10)", which is physically represented by the Pipelined Synchronized Buffer (PSB) board in slot 15 of the Global Trigger crate.
The details of the bit mapping on the cables are shown on the ***twiki*** page
https://twiki.cern.ch/twiki/bin/viewauth/CMS/L1ExternalConditions

4.1.7 ALGO_BX_EN trigger

This feature allows to enable or disable triggers at every bunch-crossing and for all 96 algorithms. Therefore a memory (4096x96 bits) is available, where the bunch-crossing per one orbit (3564 bx) and 96 algorithms are seen like a matrix. Setting a bit in this matrix to '1', enables to trigger at the chosen bx of the selected algorithm, a setting to '0', disables it.
The default value of the bits in the memory is '1', which means all bx at all algorithms are enabled. These default values are defined in memory-initiation-files (i.e. algo_bx_en_table0.mif). The memory is seen as a 6x4096x16 bits by VME-bus, so 6 mif-files are necessary. The VME addresses of the memory-blocks one can see in the following chapters.

4.2 VME-addresses

4.2.1 VME64x-chip address spaces

A23-A19: Geographic address (=VME slot number) or '11110'=amnesia address
AM=**0x2F**, data access: **D08_O**

A18-A00		**Register-name**
0x00003 - 0x007FF	=>	512x8 bit Configuration ROM (read)
0x01003	=>	chip-id_3 (read)
0x01007	=>	chip-id_2 (read)
0x0100B	=>	chip-id_1 (read)
0x0100F	=>	chip-id_0 (read)
0x01013	=>	version_3 (read)
0x01017	=>	version_2 (read)
0x0101B	=>	version_1 (read)
0x0101F	=>	version_0 (read)
0x01023 - 0x01033	=>	5 bytes Serial Number [GTLxx] (read)
0x03003 - 0x037FF	=>	CRAM 512x8 bit RAM (not used!!) (read/write)
0x05003 - 0x05007	=>	TEST_OUT-selection in USER_CSR (read/write)
[0x7FC03 - 0x7FFFF	=>	Command/Status registers (read/write)]
0x7FF63	=>	ADER-F0_3 register (read/write)
0x7FF67	=>	ADER-F0_2 register (read/write)
0x7FF6B	=>	ADER-F0_1 register (read/write)
0x7FF6F	=>	ADER-F0_0 register (read/write)
0x7FF73	=>	ADER-F1_3 register (read/write)
0x7FF77	=>	ADER-F1_2 register (read/write)
0x7FF7B	=>	ADER-F1_1 register (read/write)
0x7FF7F	=>	ADER-F1_0 register (read/write)
0x7FFF7	=>	Bit Clear Register [BCR] (read/write)
0x7FFFB	=>	Bit Set Register [BSR] (read/write)
0x7FFFF	=>	BAR - Geographic address (read)

4.2.2 GTL9U-chips address spaces

Function 0 (F0) - base-address at **A31-A25**, AM=**0x0D** and **0x09**, data access: **D16**
Function 1 (F1) - base-address at **A31-A25**, AM=**0x0F** and **0x0B**, data access: **D16**

A24-A00 => Register-name

```
0x0000000 - 0x03FFFFE => see COND1-chip
0x0400000 - 0x07FFFFE => see COND2-chip
0x0800000 - 0x0BFFFFE => see REC1-chip
0x0C00000 - 0x0FFFFFE => see REC2-chip
0x1000000 - 0x13FFFFE => see REC3-chip
0x1400000 - 0x17FFFFE => see Broadcast to COND- and REC-chips
0x1800000 - 0x19FFFFE => see Cond-memory of COND1-chip
0x1A00000 - 0x1BFFFFE => see Cond-memory of COND2-chip
0x1C00000 - 0x1FFFFFE => see VME-chip
```

4.2.3 Addressdefinition of Condition-chips

A31..A25	**A24..A22**	**A21..A14**			**A13..A08**	**A07..A01,(00)**
7 bits	3 bits	8 bits			6 bits	7 bits
PARTICLE conditions:						
base address	chip name	0	particle name	condition type	condition index	register name
CORRELATION conditions:						
base address	chip name	1	0	condition type	condition index	register name
SPECIAL conditions:						
base address	chip name	1	1	condition type		register name
Chip ID and version registers:						
base address	chip name	1	1	0xFFF		register name

Table 4.2: Addressdefinition of condition-chips

4.2.3.1 Addresses for chip name

A24..A22	**chip name**
000	COND1-chip
001	COND2-chip
010	REC1-chip
011	REC2-chip
100	REC3-chip
101	Broadcast to COND- and REC-chips
110	Cond-memories of COND-chips
111	VME-chip

Table 4.3: Addresses to select FPGA-chips

4.2.3.2 Addresses for particle conditions

A21..A17	**particle name (objects)**

00000	Isolated electron/photon (IEG)
00001	Non-isolated electron/photon (EG)
00010	Central jet (cJET)
00011	Tau-flagged jet (TAU)
00100	Forward jet (fJET)
00101	Muon
00110	Ring rapidity
00111	"free"
01000	Energy summary information (esums)

Table 4.4: Addresses to select objects

4.2.3.3 Addresses for calorimeter-objects

A16..A14	**condition type**
000	four particle condition (cond_4)
001	two particle condition, "simple" (cond_2_s)
010	two particle condition, with spatial correlation (cond_2_wsc)
011	one particle condition (cond_1_s)

Table 4.5: Addresses to select calorimeter-objects condition types

A07..A01	**register name**
0000 000	E_T-threshold 1
0000 001	E_T-threshold 2
0000 010	E_T-threshold 3
0000 011	E_T-threshold 4

Table 4.6: Addresses of Et-threshold-register

register name	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
E_T-threshold 1..4	ge/eq	-	E_T-threshold					

Table 4.7: Content of Et-threshold-register

4.2.3.4 Addresses for muon-objects

A16..A14	**condition type**
000	four particle condition (cond_4)
001	two particle condition, "simple" (cond_2_s)
010	two particle condition, with spatial correlation (cond_2_wsc)
011	one particle condition (cond_1_s)
100	three particle condition (cond_3)

Table 4.8: Addresses to select muon condition types

A07..A01	**register name**
0000 000	high p_T-threshold 1
0000 001	high p_T-threshold 2
0000 010	high p_T-threshold 3
0000 011	high p_T-threshold 4
0000 100-0100 111	not used

0101 000	enable_quality 1
0101 001	enable_quality 2
0101 010	enable_quality 3
0101 011	enable_quality 4
0101 100	low p_T-threshold 1
0101 101	low p_T-threshold 2
0101 110	low p_T-threshold 3
0101 111	low p_T-threshold 4
0110 000-1000 100	not used
1000 101	en_charge_correlations

Table 4.9: Addresses of muon-register

register name	D7	D6	D5	D4	D3	D2	D1	D0
high p_T-threshold 1..4	ge/eq	-	-	high p_T-threshold				
enable quality 1..4	en_quality [7..0]							
low p_T-threshold 1..4	en_mip	en_iso	request_ iso	low p_T-threshold				

Table 4.10: Content of pt-threshold- and enable-quality-register

register name	D7..D3	D2	D1	D0
en_charge_correlations for cond_1_s	-	enable_pos	enable_neg	ignore
en_charge_correlations for cond_2_s, cond_2_wsc and cond_3	-	enable_equal	enable_not_equal	ignore
en_charge_correlations for cond_4	-	enable_equal	enable_pairs	ignore

Table 4.11: Content of enable-charge-correlations-register

4.2.3.5 Addresses for Ring rapidity

A16..A14	condition type
000	ring_1_pos_rap_hf
001	ring_1_neg_rap_hf
010	ring_2_pos_rap_hf
011	ring_2_neg_rap_hf
100	ring_1_pos_rap_ etsums
101	ring_1_neg_rap_ etsums
110	ring_2_pos_rap_ etsums
111	ring_2_neg_rap_ etsums

Table 4.12: Addresses of ring-rapidity-register

A07..A01	register name
0000 000	ring_rap_threshold

Table 4.13: Address of ring-rapidity-threshold-register

register name	D7..D3	D2	D1	D0
ring_rap_threshold	-	threshold [2..0]		

Table 4.14: Content of ring-rapidity-threshold-register

4.2.3.6 Addresses for Energy summary information

A16..A14	condition type
000	total Et (ett)
001	missing Et (etm)
010	total Ht (htt)
011	missing Ht (htm)

Table 4.15: Addresses of ring-rapidity-register

4.2.3.6.1 Addresses for register of ett, htt and etm

A07..A01	register name
0000 000	threshold lsb
0000 001	threshold msb

Table 4.16: Addresses of esums-threshold-register

register name	D7	D6	D5	D4	D3	D2	D1	D0
threshold lsb	threshold [7..0]							
threshold msb	ge/eq	-	-	-	threshold [11..8]			

Table 4.17: Content of esums-threshold-register

4.2.3.6.2 Addresses for register of htm

A07..A01	register name
0000 000	threshold

Table 4.18: Addresses of htm-threshold-register

register name	D7	D6	D5	D4	D3	D2	D1	D0
threshold	ge/eq	threshold [6..0]						

Table 4.19: Content of htm-threshold-register

4.2.3.7 Addresses for correlation conditions

A21..A14	condition type
1000 0000	Muon_Isolated electron/photon (muon_ieg)
1000 0001	Muon_Non-isolated electron/photon (muon_eg)
1000 0010	Muon_Central jet (muon_cjet)
1000 0011	Muon_Forward jet (muon_fjet)
1000 0100	Muon_Tau-flagged jet (muon_tau)
1000 0101	Isolated electron/photon_Non-isolated electron/photon (ieg_eg)
1000 0110	Isolated electron/photon_Central jet (ieg_cjet)
1000 0111	Isolated electron/photon_Forward jet (ieg_fjet)
1000 1000	Isolated electron/photon_Tau-flagged jet (ieg_tau)

1000 1001	Non-isolated electron/photon_Central jet (eg_cjet)
1000 1010	Non-isolated electron/photon_Forward jet (eg_fjet)
1000 1011	Non-isolated electron/photon_Tau-flagged jet (eg_tau)
1000 1100	Central jet_Forward jet (cjet_fjet)
1000 1101	Central jet_Tau-flagged jet (cjet_tau)
1000 1110	Forward jet_Tau-flagged jet (fjet_tau)
1000 1111	(not use)
1001 0000	missing Et_Muon (etm_muon)
1001 0001	missing Et_Isolated electron/photon (etm_ieg)
1001 0010	missing Et_Non-isolated electron/photon (etm_eg)
1001 0011	missing Et_Central jet (etm_cjet)
1001 0100	missing Et_Forward jet (etm_fjet)
1001 0101	missing Et_Tau-flagged jet (etm_tau)
1001 0110	missing Ht_Muon (htm_muon)
1001 0111	missing Ht_Isolated electron/photon (htm_ieg)
1001 1000	missing Ht_Non-isolated electron/photon (htm_eg)
1001 1001	missing Ht_Central jet (htm_cjet)
1001 1010	missing Ht_Forward jet (htm_fjet)
1001 1011	missing Ht_Tau-flagged jet (htm_tau)
1001 1100	missing Ht_missing Et (htm_etm)

Table 4.20: Addresses of correlation condition types

A07..A01	**register name**
0010 000	calo 1 E_T-threshold
0100 000	calo 2 E_T-threshold
0110 000	muon high p_T-threshold
0111 001	muon enable_quality
0111 010	muon low p_T-threshold
0111 011	muon en_charge_correlations
1000 000	etm threshold lsb
1000 001	etm threshold msb
1001 000	htm threshold lsb

Table 4.21: Addresses of register for correlation conditions

The contents of the register one can find in the chapters above.

4.2.4 Addresstable of COND1-chip

4.2.4.1 Condition registers

`0x0000000 - 0x03FFEFE` => see tables in 4.2.3 Addressdefinition of Cond-chips

4.2.4.2 Selection register

`0x03FFF00` => selection_register (write/read, 8 bit)

4.2.4.3 Chip ID and version registers

`0x03FFFF0` => chip_id_register_3 (chip_ID [31..24]) (read, 8 bit)
`0x03FFFF2` => chip_id_register_2 (chip_ID [23..16]) (read, 8 bit)
`0x03FFFF4` => chip_id_register_1 (chip_ID [15..8]) (read, 8 bit)

0x03FFFF6 => chip_id_register_0 (chip_ID [7..0]) (read, 8 bit)
0x03FFFF8 => version_register_3 (version [31..24]) (read, 8 bit)
0x03FFFFA => version_register_2 (version [23..16]) (read, 8 bit)
0x03FFFFC => version_register_1 (version [15..8]) (read, 8 bit)
0x03FFFFE => version_register_0 (version [7..0]) (read, 8 bit)

4.2.4.4 Condition-memory registers

0x1800000 => Bx-nr-register low (write/read, 8 bit)
0x1800002 => Bx-nr-register high (write/read, 8 bit)
0x1800004 => BCNTRES-delay-register (write/read, 8 bit)
0x1800006 => MODE-register (write/read, 8 bit)
0x1800008 => START_BCNTNR (write only, pulse, 1 bit)

4.2.4.5 Condition-memory addresses

Memory size: 6 x 1024 x 16 bits
0x1900000 - 0x19007FE => ALGO [111..96] (write/read, 16 bit)
0x1900800 - 0x1900FFE => ALGO [127..112] (write/read, 16 bit)
0x1901000 - 0x19017FE => ALGO [143..128] (write/read, 16 bit)
0x1901800 - 0x1901FFE => ALGO [159..144] (write/read, 16 bit)
0x1902000 - 0x19027FE => ALGO [175..160] (write/read, 16 bit)
0x1902800 - 0x1902FFE => ALGO [191..176] (write/read, 16 bit)

4.2.4.6 ALGO_BX_EN-memory addresses

Memory size: 6 x 4096 x 16 bits
0x1910000-0x1911FFE => ALGO [111..96] (w/r, 16 bit) – ALGO_BX_EN_0_COND1
0x1912000-0x1913FFE => ALGO [127..112] (w/r, 16 bit) – ALGO_BX_EN_1_COND1
0x1914000-0x1915FFE => ALGO [143..128] (w/r, 16 bit) – ALGO_BX_EN_2_COND1
0x1916000-0x1917FFE => ALGO [159..144] (w/r, 16 bit) – ALGO_BX_EN_3_COND1
0x1918000-0x1919FFE => ALGO [175..160] (w/r, 16 bit) – ALGO_BX_EN_4_COND1
0x191A000-0x191AFFE => ALGO [191..176] (w/r, 16 bit) – ALGO_BX_EN_5_COND1

4.2.5 Addresstable of COND2-chip

4.2.5.1 Condition registers

0x0400000 - 0x07FFEFE => see tables in 4.2.3 Addressdefinition of Cond-chips

4.2.5.2 Selection register

0x07FFF00 => selection_register (write/read, 8 bit)

4.2.5.3 Chip ID and version registers

0x07FFFF0 => chip_id_register_3 (chip_ID [31..24]) (read, 8 bit)
0x07FFFF2 => chip_id_register_2 (chip_ID [23..16]) (read, 8 bit)
0x07FFFF4 => chip_id_register_1 (chip_ID [15..8]) (read, 8 bit)
0x07FFFF6 => chip_id_register_0 (chip_ID [7..0]) (read, 8 bit)
0x07FFFF8 => version_register_3 (version [31..24]) (read, 8 bit)
0x07FFFFA => version_register_2 (version [23..16]) (read, 8 bit)
0x07FFFFC => version_register_1 (version [15..8]) (read, 8 bit)
0x07FFFFE => version_register_0 (version [7..0]) (read, 8 bit)

4.2.5.4 Condition-memory registers

0x1A00000 => Bx-nr-register low (write/read, 8 bit)
0x1A00002 => Bx-nr-register high (write/read, 8 bit)
0x1A00004 => BCNTRES-delay-register (write/read, 8 bit)
0x1A00006 => MODE-register (write/read, 8 bit)
0x1A00008 => START_BCNTNR (write only, pulse, 1 bit)

4.2.5.5 Condition-memory addresses

Memory size: 6 x 1024 x 16 bits
0x1B00000 - 0x1B007FE => ALGO [15..0] (write/read, 16 bit)
0x1B00800 - 0x1B00FFE => ALGO [31..16] (write/read, 16 bit)
0x1B01000 - 0x1B017FE => ALGO [47..32] (write/read, 16 bit)
0x1B01800 - 0x1B01FFE => ALGO [63..48] (write/read, 16 bit)
0x1B02000 - 0x1B027FE => ALGO [79..64] (write/read, 16 bit)
0x1B02800 - 0x1B02FFE => ALGO [95..80] (write/read, 16 bit)

4.2.5.6 ALGO_BX_EN-memory addresses

Memory size: 6 x 4096 x 16 bits
0x1B10000-0x1B11FFE => ALGO [15..0] (w/r, 16 bit) – ALGO_BX_EN_0_COND2
0x1B12000-0x1B13FFE => ALGO [31..16] (w/r, 16 bit) – ALGO_BX_EN_1_COND2
0x1B14000-0x1B15FFE => ALGO [47..32] (w/r, 16 bit) – ALGO_BX_EN_2_COND2
0x1B16000-0x1B17FFE => ALGO [63..48] (w/r, 16 bit) – ALGO_BX_EN_3_COND2
0x1B18000-0x1B19FFE => ALGO [79..64] (w/r, 16 bit) – ALGO_BX_EN_4_COND2
0x1B1A000-0x1B1AFFE => ALGO [95..80] (w/r, 16 bit) – ALGO_BX_EN_5_COND2

4.2.6 REC1-chip

4.2.6.1 Register overview

0x0800000 => VERSION_NR_L (read, 16 bit)
0x0800002 => VERSION_NR_H (read, 16 bit)
0x0800004 => CHIP_IDL (read, 16 bit)
0x0800006 => CHIP_IDH (read, 16 bit)
0x0800008 => REC_STATUS (read, 16 bit)
0x080000A => BC_ERRORS (read, 16 bit)
0x0800010 => BCRES_DELAY (write/read, 16 bit)
0x0800012 => MAX_BC_NUMBER (write/read, 16 bit)
0x0800014 => TESTMASK0 (write/read, 16 bit)
0x0800016 => TESTMASK1 (write/read, 16 bit)
0x0800018 => TESTMASK2 (write/read, 16 bit)
0x080001A => TESTMASK3 (write/read, 16 bit)
0x080001C => CMD_REG (write/read, 16 bit)
0x080001E => CMD_PULSE (write, 16 bit)
0x08000F0 => run_v (write)
0x08000F2 => run_v_until_end (write)
0x08000F4 => run_sync (write)
0x08000F6 => run_sync_until_end (write)
0x08000F8 => stop_v (write)
0x08000FA => stop_sync (write)

4.2.6.2 REC1 Sim Spy Memories

0x0820000 - 0x0823FFE => SIM_SPY_MU12_L (write/read, 16 bit)
0x0824000 - 0x0827FFE => SIM_SPY_MU12_H (write/read, 16 bit)
0x0828000 - 0x082BFFE => SIM_SPY_MU34_L (write/read, 16 bit)
0x082C000 - 0x082FFFE => SIM_SPY_MU34_H (write/read, 16 bit)
0x0830000 - 0x0833FFE => SIM_SPY_CA1_13 (write/read, 16 bit)
0x0834000 - 0x0837FFE => SIM_SPY_CA1_24 (write/read, 16 bit)
0x0838000 - 0x083BFFE => SIM_SPY_CA2_13 (write/read, 16 bit)
0x083C000 - 0x083FFFE => SIM_SPY_CA2_24 (write/read, 16 bit)

4.2.7 REC2-chip

4.2.7.1 Register overview

0x0C00000 => VERSION_NR_L (read, 16 bit)
0x0C00002 => VERSION_NR_H (read, 16 bit)
0x0C00004 => CHIP_IDL (read, 16 bit)
0x0C00006 => CHIP_IDH (read, 16 bit)
0x0C00008 => REC_STATUS (read, 16 bit)
0x0C0000A => BC_ERRORS (read, 16 bit)
0x0C00010 => BCRES_DELAY (write/read, 16 bit)
0x0C00012 => MAX_BC_NUMBER (write/read, 16 bit)
0x0C00014 => TESTMASK0 (write/read, 16 bit)
0x0C00016 => TESTMASK1 (write/read, 16 bit)
0x0C00018 => TESTMASK2 (write/read, 16 bit)
0x0C0001A => TESTMASK3 (write/read, 16 bit)
0x0C0001C => CMD_REG (write/read, 16 bit)
0x0C0001E => CMD_PULSE (write, 16 bit)
0x0C000F0 => run_v (write)
0x0C000F2 => run_v_until_end (write)
0x0C000F4 => run_sync (write)
0x0C000F6 => run_sync_until_end (write)
0x0C000F8 => stop_v (write)
0x0C000FA => stop_sync (write)

4.2.7.2 REC2 Sim Spy Memories

0x0C20000 - 0x0C23FFE => SIM_SPY_CA3_13 (write/read, 16 bit)
0x0C24000 - 0x0C27FFE => SIM_SPY_CA3_24 (write/read, 16 bit)
0x0C28000 - 0x0C2BFFE => SIM_SPY_CA4_13 (write/read, 16 bit)
0x0C2C000 - 0x0C2FFFE => SIM_SPY_CA4_24 (write/read, 16 bit)
0x0C30000 - 0x0C33FFE => SIM_SPY_CA5_13 (write/read, 16 bit)
0x0C34000 - 0x0C37FFE => SIM_SPY_CA5_24 (write/read, 16 bit)
0x0C38000 - 0x0C3BFFE => SIM_SPY_CA6_13 (write/read, 16 bit)
0x0C3C000 - 0x0C3FFFE => SIM_SPY_CA6_24 (write/read, 16 bit)

4.2.8 REC3-chip

4.2.8.1 Register overview

0x1000000 => VERSION_NR_L (read, 16 bit)
0x1000002 => VERSION_NR_H (read, 16 bit)
0x1000004 => CHIP_IDL (read, 16 bit)
0x1000006 => CHIP_IDH (read, 16 bit)
0x1000008 => REC_STATUS (read, 16 bit)

0x100000A => BC_ERRORS (read, 16 bit)
0x1000010 => BCRES_DELAY (write/read, 16 bit)
0x1000012 => MAX_BC_NUMBER (write/read, 16 bit)
0x1000014 => TESTMASK0 (write/read, 16 bit)
0x1000016 => TESTMASK1 (write/read, 16 bit)
0x1000018 => TESTMASK2 (write/read, 16 bit)
0x100001A => TESTMASK3 (write/read, 16 bit)
0x100001C => CMD_REG (write/read, 16 bit)
0x100001E => CMD_PULSE (write, 16 bit)
0x10000F0 => run_v (write)
0x10000F2 => run_v_until_end (write)
0x10000F4 => run_sync (write)
0x10000F6 => run_sync_until_end (write)
0x10000F8 => stop_v (write)
0x10000FA => stop_sync (write)

4.2.8.2 REC3 Sim Spy Memories

0x1020000 - 0x1023FFE => SIM_SPY_CA7_13 (write/read, 16 bit)
0x1024000 - 0x1027FFE => SIM_SPY_CA7_24 (write/read, 16 bit)
0x1028000 - 0x102BFFE => SIM_SPY_CA8_13 (write/read, 16 bit)
0x102C000 - 0x102FFFE => SIM_SPY_CA8_24 (write/read, 16 bit)
0x1030000 - 0x1033FFE => SIM_SPY_CA9_13 (write/read, 16 bit)
0x1034000 - 0x1037FFE => SIM_SPY_CA9_24 (write/read, 16 bit)
0x1038000 - 0x103BFFE => SIM_SPY_CA10_13 (write/read, 16 bit)
0x103C000 - 0x103FFFE => SIM_SPY_CA10_24 (write/read, 16 bit)

4.2.9 Broadcast to REC- and COND-chips

4.2.9.1 RUN/STOP Registers:

0x14000F0 => run_v (write)
0x14000F2 => run_v_until_end (write)
0x14000F4 => run_sync (write)
0x14000F6 => runsyn_until_end (write)
0x14000F8 => stop_v (write)
0x14000FA => stop_sync (write)

4.2.10 VME-chip

4.2.10.1 Registers for Programmable-chips-configuration:

0x1C00000 => CMD_ENPROG-register (write/read, 8-bit)
0x1C00002 => CMD_NPROG-register (write/read, 8-bit)
0x1C00004 => CMD_INIT-register (write/read, 8-bit)
0x1C00006 => STAT_INIT-register (read, 8-bit)
0x1C00008 => STAT_DONE-register (read, 8-bit)

4.2.10.2 Configuration of Programmable-chips:

0x1C0000A => Configuration register REC1-chip (write, 1-bit)
0x1C0000C => Configuration register REC2-chip (write, 1-bit)
0x1C0000E => Configuration register REC3-chip (write, 1-bit)
0x1C00010 => Configuration register COND1-chip (write, 8-bit)
0x1C00012 => Configuration register COND2-chip (write, 8-bit)

4.2.10.3 General pulse registers:

`0x1C00014` => Command pulse register (write, 8-bit)
`0x1C00016` => Status pulse register (read, 8-bit)

4.2.10.4 General registers:

`0x1C00018` => Command register (write/read, 8-bit)
`0x1C0001A` => Status register (read, 8-bit)

4.2.10.5 TEST-OUT registers:

`0x1C0001C` => TEST-OUT-10 register (write/read, 8-bit)
`0x1C0001E` => TEST-OUT-32 register (write/read, 8-bit)

4.2.10.6 Chip ID and version registers:

`0x1C00020` => chip_id_register_3 (read, 8-bit)
`0x1C00022` => chip_id_register_2 (read, 8-bit)
`0x1C00024` => chip_id_register_1 (read, 8-bit)
`0x1C00026` => chip_id_register_0 (read, 8-bit)
`0x1C00028` => version_register_3 (read, 8-bit)
`0x1C0002A` => version_register_2 (read, 8-bit)
`0x1C0002C` => version_register_1 (read, 8-bit)
`0x1C0002E` => version_register_0 (read, 8-bit)

4.2.10.7 JTAG registers:

`0x1C00030` => tdo_register (write/read, 8-bit)
`0x1C00032` => tdi_register (write/read, 8-bit)
`0x1C00034` => tms0_register (write/read, 8-bit)
`0x1C00036` => tms1_register (write/read, 8-bit)
`0x1C00038` => cnt32_register (write/read, 8-bit)
`0x1C0003A` => mode0_register (write/read, 8-bit)
`0x1C0003C` => mode1_register (write/read, 8-bit)
`0x1C0003E` => mode2_register (write/read, 8-bit)

4.2.10.8 Trigger-control registers:

`0x1C00040` => Trigger-control-command register 0 (write, 8-bit)
`0x1C00042` => Trigger-control-command register 1 (write, 8-bit)
`0x1C00044` => Trigger-control-status register REC (read, 8-bit)
`0x1C00046` => Trigger-control-status register COND (read, 8-bit)

4.2.10.9 Read-out-bus registers:

`0x1C00048` => Read-out-bus register 0 (read, 8-bit)
`0x1C0004A` => Read-out-bus register 1 (read, 8-bit)

5 Software

5.1 Overview

There are two software packages to work with the GTL-9U-module.
The L1-Trigger-Menu-Editor (TME) is a GUI-based packages in the Trigger-Supervisor environment of CMS and is used to create trigger-menus (firmware of condition-chips).
The GTL9Ustandalone software package is the communication platform with the GTL-9U-module via VME-bus.

6 Appendices

6.1 Definition of Calorimeter channels in GT-system

Status of definition on April 20, 2010.

For details of definition see CMS Level-1 Global Calorimeter Trigger to Global Trigger and Global Muon Trigger Interfaces [3].

Calorimeter channel	Cable Content	Connector on PSB [present use]	Connector on PSB [future use]
CA1	Isolated electron/photon objects	PSB_V2 slot #13 IN 6-7 used	PSB_OPT slot #13 fiber U3 (OGTI) used
CA2	Non-isolated electron/photon objects	PSB_V2 slot #13 IN 4-5 used	PSB_OPT slot #13 fiber U2 (OGTI) used
CA3	Central jet objects	PSB_V2 slot #13 IN 2-3 used	PSB_OPT slot #13 fiber U1 (OGTI) used
CA4	Forward jet objects	PSB_V2 slot #13 IN 0-1 used	PSB_OPT slot #13 fiber U0 (OGTI) used
CA5	Tau-flagged jet objects	PSB_V2 slot #14 IN 6-7 used	PSB_OPT slot #14 fiber U3 (OGTI) used
CA6	Energy summary information (total Et, Ht and EtMiss)	PSB_V2 slot #14 IN 4-5 used	PSB_OPT slot #14 fiber U2 (OGTI) used
CA7	Ring rapidity HF/Et-sums, HtMiss	PSB_V2 slot #14 IN 2-3 used	PSB_OPT slot #14 fiber U1 (OGTI) used
CA8	TBD (free)	PSB_V2 slot #14 IN 0-1 or 16xRJ45 [63-0] free	PSB_OPT slot #14 fiber U0 (OGTI) or 8xRJ45 [31-0] free
CA9	TBD (free)	PSB_V2 slot #15 IN 2-3 free	PSB_OPT slot #15 fiber U1 (OGTI) free
CA10	External Conditions data	PSB_V2 slot #15 3xRJ45 used [12 bits, 11-0] 13xRJ45 free [52 bits, 63-12]	PSB_OPT slot #15 3xRJ45 used [12 bits, 11-0] 5xRJ45 free [20 bits, 31-12]
There is an option for CA9 and CA10 - using PSB_V2 for future use:			
CA9	not useable	-	PSB_V2 in slot #15 with infiniband inputs
CA10	External Conditions data	-	PSB_V2 slot #15 3xRJ45 used [12 bits, 11-0] 13xRJ45 free [52 bits, 63-12]

TBD means “to be defined”

Table 6.1: Calorimeter channels in GT-system

Bit assignments on GT Calorimeter channels 1-5 (CA1..CA5)

Bit no.	CAx13 *)		CAx24	
	object 1	object 3	object 2	object 4
0	Object 1 rank #0	Object 3 rank #0	Object 2 rank #0	Object 4 rank #0
1	Object 1 rank #1	Object 3 rank #1	Object 2 rank #1	Object 4 rank #1
2	Object 1 rank #2	Object 3 rank #2	Object 2 rank #2	Object 4 rank #2
3	Object 1 rank #3	Object 3 rank #3	Object 2 rank #3	Object 4 rank #3
4	Object 1 rank #4	Object 3 rank #4	Object 2 rank #4	Object 4 rank #4
5	Object 1 rank #5	Object 3 rank #5	Object 2 rank #5	Object 4 rank #5
6	Object 1 eta #0	Object 3 eta #0	Object 2 eta #0	Object 4 eta #0
7	Object 1 eta #1	Object 3 eta #1	Object 2 eta #1	Object 4 eta #1
8	Object 1 eta #2	Object 3 eta #2	Object 2 eta #2	Object 4 eta #2
9	Object 1 eta_sign	Object 3 eta_sign	Object 2 eta_sign	Object 4 eta_sign
10	Object 1 phi #0	Object 3 phi #0	Object 2 phi #0	Object 4 phi #0

11	Object 1 phi #1	Object 3 phi #1	Object 2 phi #1	Object 4 phi #1
12	Object 1 phi #2	Object 3 phi #2	Object 2 phi #2	Object 4 phi #2
13	Object 1 phi #3	Object 3 phi #3	Object 2 phi #3	Object 4 phi #3
14	Object 1 phi #4	Object 3 phi #4	Object 2 phi #4	Object 4 phi #4
15	Always '1'	'1'=BC0 else '0'	Always '1'	'1'=BC0 else '0'

*) x runs from 1 to 5

Table 6.2: Bit assignments on GT Calorimeter channels 1-5 (CA1..CA5)

Bit assignments on GT Calorimeter channel 6 (CA6)

Bit no.	CA613		CA624	
	object 1	object 3	object 2	object 4
0	Total_Et #0	Ht #0	EtMiss_mag #0	EtMiss_phi #0
1	Total_Et #1	Ht #1	EtMiss_mag #1	EtMiss_phi #1
2	Total_Et #2	Ht #2	EtMiss_mag #2	EtMiss_phi #2
3	Total_Et #3	Ht #3	EtMiss_mag #3	EtMiss_phi #3
4	Total_Et #4	Ht #4	EtMiss_mag #4	EtMiss_phi #4
5	Total_Et #5	Ht #5	EtMiss_mag #5	EtMiss_phi #5
6	Total_Et #6	Ht #6	EtMiss_mag #6	EtMiss_phi #6
7	Total_Et #7	Ht #7	EtMiss_mag #7	Always '0'
8	Total_Et #8	Ht #8	EtMiss_mag #8	Always '0'
9	Total_Et #9	Ht #9	EtMiss_mag #9	Always '0'
10	Total_Et #10	Ht #10	EtMiss_mag #10	Always '0'
11	Total_Et #11	Ht #11	EtMiss_mag #11	Always '0'
12	Total_Et_OV	Ht_OV	EtMiss_mag_OV	Always '0'
13	Always '0'	Always '0'	Always '0'	Always '0'
14	Always '0'	Always '0'	Always '0'	Always '0'
15	Always '1'	'1'=BC0 else '0'	Always '1'	'1'=BC0 else '0'

Table 6.3: Bit assignments on GT Calorimeter channel 6 (CA6)

Bit assignments on GT Calorimeter channels 7 (CA7)

Bit no.	CA713		CA724	
	object 1	object 3	object 2	object 4
0	Ring 1 Pos. Rap. HF #0	Ring 1 Neg. Rap. Et-sums #0	HtMiss_phi #0	Always '1'
1	Ring 1 Pos. Rap. HF #1	Ring 1 Neg. Rap. Et-sums #1	HtMiss_phi #1	Always '0'
2	Ring 1 Pos. Rap. HF #2	Ring 1 Neg. Rap. Et-sums #2	HtMiss_phi #2	Always '1'
3	Ring 1 Neg. Rap. HF #0	Ring 2 Pos. Rap. Et-sums #0	HtMiss_phi #3	Always '0'
4	Ring 1 Neg. Rap. HF #1	Ring 2 Pos. Rap. Et-sums #1	HtMiss_phi #4	Always '1'
5	Ring 1 Neg. Rap. HF #2	Ring 2 Pos. Rap. Et-sums #2	HtMiss_mag #0	Always '0'
6	Ring 2 Pos. Rap. HF #0	Ring 2 Neg. Rap. Et-sums #0	HtMiss_mag #1	Always '1'
7	Ring 2 Pos. Rap. HF #1	Ring 2 Neg. Rap. Et-sums #1	HtMiss_mag #2	Always '0'
8	Ring 2 Pos. Rap. HF #2	Ring 2 Neg. Rap. Et-sums #2	HtMiss_mag #3	Always '1'
9	Ring 2 Neg. Rap. HF #0	Always '0'	HtMiss_mag #4	Always '0'
10	Ring 2 Neg. Rap. HF #1	Always '1'	HtMiss_mag #5	Always '1'
11	Ring 2 Neg. Rap. HF #2	Always '0'	HtMiss_mag #6	Always '0'
12	Ring 1 Pos. Rap. Et-sums #0	Always '1'	HtMiss_mag_OV	Always '1'
13	Ring 1 Pos. Rap. Et-sums #1	Always '0'	Always '0'	Always '0'
14	Ring 1 Pos. Rap. Et-sums #2	Always '1'	Always '1'	Always '1'
15	Always '1'	'1'=BC0 else '0'	Always '1'	'1'=BC0 else '0'

Pos. means Positive
Neg. means Negative
Rap. means Rapidity

Table 6.4: Bit assignments on GT Calorimeter channel 7 (CA7)

Bit assignments on GT Calorimeter channel 8 (CA8)

Bit no.	CA813		CA824	
	object 1	object 3	object 2	object 4
0	TBD	TBD	TBD	TBD
1	TBD	TBD	TBD	TBD
2	TBD	TBD	TBD	TBD
3	TBD	TBD	TBD	TBD
4	TBD	TBD	TBD	TBD
5	TBD	TBD	TBD	TBD
6	TBD	TBD	TBD	TBD
7	TBD	TBD	TBD	TBD
8	TBD	TBD	TBD	TBD
9	TBD	TBD	TBD	TBD
10	TBD	TBD	TBD	TBD
11	TBD	TBD	TBD	TBD
12	TBD	TBD	TBD	TBD
13	TBD	TBD	TBD	TBD
14	TBD	TBD	TBD	TBD
15	Always ‘1’	‘1’=BC0 else ‘0’	Always ‘1’	‘1’=BC0 else ‘0’

TBD means “to be defined”

Table 6.5: Bit assignments on GT Calorimeter channel 8 (CA8)

Bit assignments on GT Calorimeter channel 9 (CA9)

Bit no.	CA913		CA924	
	object 1	object 3	object 2	object 4
0	TBD	TBD	TBD	TBD
1	TBD	TBD	TBD	TBD
2	TBD	TBD	TBD	TBD
3	TBD	TBD	TBD	TBD
4	TBD	TBD	TBD	TBD
5	TBD	TBD	TBD	TBD
6	TBD	TBD	TBD	TBD
7	TBD	TBD	TBD	TBD
8	TBD	TBD	TBD	TBD
9	TBD	TBD	TBD	TBD
10	TBD	TBD	TBD	TBD
11	TBD	TBD	TBD	TBD
12	TBD	TBD	TBD	TBD
13	TBD	TBD	TBD	TBD
14	TBD	TBD	TBD	TBD
15	Always ‘1’	‘1’=BC0 else ‘0’	Always ‘1’	‘1’=BC0 else ‘0’

TBD means “to be defined”

Table 6.6: Bit assignments on GT Calorimeter channel 9 (CA9)

Bit assignments on GT Calorimeter channels 10 (CA10)

The details of the bit mapping on the cables are shown on the ***twiki*** page
https://twiki.cern.ch/twiki/bin/viewauth/CMS/L1ExternalConditions

Bit no.	CA1013			
	conn. obj. 1	object 1	conn. obj. 3	object 3
0	RJ45 3-0	reserved for CASTOR	RJ45 35-32	TBD
1		reserved for CASTOR		TBD
2		reserved for CASTOR		TBD
3		reserved for CASTOR		TBD
4	RJ45 7-4	reserved for CASTOR	RJ45 39-36	TBD
5		reserved for CASTOR		TBD
6		reserved for CASTOR		TBD
7		reserved for CASTOR		TBD
8	RJ45 11-8	reserved for BPTX	RJ45 43-40	TBD
9		reserved for BPTX		TBD
10		reserved for BPTX		TBD
11		reserved for BPTX		TBD
12	RJ45 15-12	reserved for BSC	RJ45 47-44	TBD
13		reserved for BSC		TBD
14		reserved for BSC		TBD
15		reserved for BSC		TBD

TBD means “to be defined”

Table 6.7: Bit assignments on GT Calorimeter channel 10 (CA10), obj. 1 and 3

Bit no.	CA1024			
	conn. obj. 2	object 2	conn. obj. 4	object 4
0	RJ45 19-16	reserved for ZDC	RJ45 51-48	TBD
1		reserved for ZDC		TBD
2		reserved for ZDC		TBD
3		reserved for ZDC		TBD
4	RJ45 23-20	reserved for RPC	RJ45 55-52	TBD
5		reserved for RPC		TBD
6		reserved for RPC		TBD
7		reserved for RPC		TBD
8	RJ45 27-24	reserved for BSC	RJ45 59-56	TBD
9		reserved for BSC		TBD
10		TBD		TBD
11		TBD		TBD
12	RJ45 31-28	TBD	RJ45 63-60	TBD
13		TBD		TBD
14		TBD		TBD
15		TBD		TBD

TBD means “to be defined”

Table 6.8: Bit assignments on GT Calorimeter channel 10 (CA10), obj. 2 and 4

6.2 Definition of Muon channels in GT-system

Status of definition on March 10, 2009.

For details of definition see Specification of the Interface between the Global Muon Trigger and the Global Trigger [4].

Bit assignments on GT for Muon objects

Bit no.	MUON12		MUON34	
	object 1	object 2	object 3	object 4
0	Object 1 phi #0	Object 2 phi #0	Object 3 phi #0	Object 4 phi #0
1	Object 1 phi #1	Object 2 phi #1	Object 3 phi #1	Object 4 phi #1
2	Object 1 phi #2	Object 2 phi #2	Object 3 phi #2	Object 4 phi #2
3	Object 1 phi #3	Object 2 phi #3	Object 3 phi #3	Object 4 phi #3
4	Object 1 phi #4	Object 2 phi #4	Object 3 phi #4	Object 4 phi #4
5	Object 1 phi #5	Object 2 phi #5	Object 3 phi #5	Object 4 phi #5
6	Object 1 phi #6	Object 2 phi #6	Object 3 phi #6	Object 4 phi #6
7	Object 1 phi #7	Object 2 phi #7	Object 3 phi #7	Object 4 phi #7
8	Object 1 pt #0	Object 2 pt #0	Object 3 pt #0	Object 4 pt #0
9	Object 1 pt #1	Object 2 pt #1	Object 3 pt #1	Object 4 pt #1
10	Object 1 pt #2	Object 2 pt #2	Object 3 pt #2	Object 4 pt #2
11	Object 1 pt #3	Object 2 pt #3	Object 3 pt #3	Object 4 pt #3
12	Object 1 pt #4	Object 2 pt #4	Object 3 pt #4	Object 4 pt #4
13	Object 1 qu #0	Object 2 qu #0	Object 3 qu #0	Object 4 qu #0
14	Object 1 qu #1	Object 2 qu #1	Object 3 qu #1	Object 4 qu #1
15	Object 1 qu #2	Object 2 qu #2	Object 3 qu #2	Object 4 qu #2
16	Object 1 eta #0	Object 2 eta #0	Object 3 eta #0	Object 4 eta #0
17	Object 1 eta #1	Object 2 eta #1	Object 3 eta #1	Object 4 eta #1
18	Object 1 eta #2	Object 2 eta #2	Object 3 eta #2	Object 4 eta #2
19	Object 1 eta #3	Object 2 eta #3	Object 3 eta #3	Object 4 eta #3
20	Object 1 eta #4	Object 2 eta #4	Object 3 eta #4	Object 4 eta #4
21	Object 1 eta_sign	Object 2 eta_sign	Object 3 eta_sign	Object 4 eta_sign
22	Object 1 iso	Object 2 iso	Object 3 iso	Object 4 iso
23	Object 1 mip	Object 2 mip	Object 3 mip	Object 4 mip
24	Object 1 sy_sign #0	Object 2 sy_sign #0	Object 3 sy_sign #0	Object 4 sy_sign #0
25	Object 1 sy_sign #1	Object 2 sy_sign #1	Object 3 sy_sign #1	Object 4 sy_sign #1
26	Reserved	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved	Reserved

Table 6.9: Bit assignments on GT for Muon objects

6.3 Jumper settings on GTL-9U-module

JP38 (top side)**:** jumper for "SEL_CABLE_JTAG"; selection of sources of JTAG-chains.
OFF ➔ source selection via VME (see Command register of VME-chip).
ON ➔ ALTERA and XILINX programming cables are selected as sources.

6.3.1 Fixed "jumpers"

JP1, JP2 and JP3 (top side)**:** jumper for LV1V5_COND1
(default)➔ solder-bridges after voltage-testing.
JP4, JP5, JP6 and JP93 (top side)**:** jumper for LV1V5_XIL
(default)➔ solder-bridges after voltage-testing.
JP7 (SMD, bottom side)**:** jumper for "CLK_FBIN_REC1"
(default)➔ not inserted.
JP8 (SMD, bottom side)**:** HSWAP_EN input of REC1-chip
1-2 ➔ HSWAP_EN=LV3V3, keeps jumper in OFF-position (I/O-pins in high-Z before configuration). In this position **configuration of PSB-chip** via **VME not possible**.
2-3 (default)➔ HSWAP_EN=GND, enables pull-up-Rs of all I/O-pins in PSB-chip before configuration. In this position **configuration of PSB-chip via VME possible**.
JP9 (SMD, bottom side)**:** HSWAP_EN input of REC2-chip
1-2 ➔ HSWAP_EN=LV3V3, keeps jumper in OFF-position (I/O-pins in high-Z before configuration).

In this position **configuration of PSB-chip** via **VME not possible**.

2-3 (default)➔ HSWAP_EN=GND, enables pull-up-Rs of all I/O-pins in PSB-chip before configuration. In this position **configuration of PSB-chip via VME possible**.

JP10 (SMD, bottom side)**:** jumper for "CLK_FBIN_REC2"

(default)➔ not inserted.

JP11 (SMD, bottom side)**:** HSWAP_EN input of REC3-chip

1-2 ➔ HSWAP_EN=LV3V3, keeps jumper in OFF-position (I/O-pins in high-Z before configuration). In this position **configuration of PSB-chip** via **VME not possible**.

2-3 (default)➔ HSWAP_EN=GND, enables pull-up-Rs of all I/O-pins in PSB-chip before configuration. In this position **configuration of PSB-chip via VME possible**.

JP12, JP14 and JP15 (top side)**:** jumper for LV1V5_COND2

(default)➔ solder-bridges after voltage-testing.

JP13 (SMD, bottom side)**:** jumper for "CLK_FBIN_REC3"

(default)➔ not inserted.

JP16 (SMD, top side)**:** VREF for Parallel-Cable-IV

(default)➔ nothing inserted.

JP17 (SMD, top side)**:** selection of VIO of masterblaster

(default)➔ 0Ω inserted.

JP18, JP19, JP20 and JP21 (SMD, top side)**:** jumper for "TMS-signals" for PROMs and VME-chips. These jumpers are set in the same way as JP40-JP43.

OFF ➔ chip **not** in JTAG-chain.

ON (default)➔ chip in JTAG-chain.

JP18 => JP40: VME64x-chip

JP19 => JP41: PROM of VME64x-chip

JP20 => JP42: VME-chip

JP21 => JP43: PROM of VME-chip

JP22, JP23, JP24 and JP25 (SMD, top side)**:** jumper for "TMS-signals" for PROMs and COND-chips. These jumpers are set in the same way as JP44-JP47.

OFF ➔ chip **not** in JTAG-chain.

ON (default)➔ chip in JTAG-chain.

JP22 => JP44: PROM of COND1-chip

JP24 => JP45: COND1-chip

JP23 => JP46: PROM of COND2-chip

JP25 => JP47: COND2-chip

JP26, JP27, JP28 and JP29 (SMD, bottom side)**:** jumper for "TMS-signals" for PROMs of REC1-chip. These jumpers are set in the same way as JP49-JP52.

OFF ➔ chip **not** in JTAG-chain.

ON (default)➔ chip in JTAG-chain.

JP26 => JP49: PROM1 of REC1-chip

JP27 => JP50: PROM2 of REC1-chip

JP28 => JP51: PROM3 of REC1-chip

JP29 => JP52: PROM4 of REC1-chip

JP30, JP31, JP32 and JP33 (SMD, bottom side)**:** jumper for "TMS-signals" for PROMs of REC2-chip. These jumpers are set in the same way as JP53-JP56.

OFF ➔ chip **not** in JTAG-chain.

ON (default)➔ chip in JTAG-chain.

JP30 => JP53: PROM1 of REC2-chip

JP31 => JP54: PROM2 of REC2-chip

JP32 => JP55: PROM3 of REC2-chip

JP33 => JP56: PROM4 of REC2-chip

JP34, JP35, JP36 and JP37 (SMD, bottom side)**:** jumper for "TMS-signals" for PROMs of REC3-chip. These jumpers are set in the same way as JP59-JP62.

OFF ➔ chip **not** in JTAG-chain.

ON (default)➔ chip in JTAG-chain.

JP34 => JP59: PROM1 of REC3-chip

JP35 => JP60: PROM2 of REC3-chip

JP36 => JP61: PROM3 of REC3-chip

JP37 => JP62: PROM4 of REC3-chip

JP38 (top side)**:** see 6.2 Jumper settings **on GTL-9U-module**

JP39 (SMD, top side)**:** voltage selection for masterblaster
1-2 (default)➔ LV3V3.
2-3 ➔ VCC.
JP40 (SMD, bottom side)**:** VME64x-chip in JTAG-chain
1-2 ➔ VME64x-chip in JTAG-chain.
2-3 (default)➔ VME64x-chip **not** in JTAG-chain.
JP41 (SMD, top side)**:** PROM of VME64x-chip in JTAG-chain
1-2 (default)➔ PROM of VME64x-chip in JTAG-chain.
2-3 ➔ PROM of VME64x-chip **not** in JTAG-chain.
JP42 (SMD, bottom side)**:** VME-chip in JTAG-chain
1-2 ➔ VME-chip in JTAG-chain.
2-3 (default)➔ VME-chip **not** in JTAG-chain.
JP43 (SMD, top side)**:** PROM of VME-chip in JTAG-chain
1-2 (default)➔ PROM of VME-chip in JTAG-chain.
2-3 ➔ PROM of VME-chip **not** in JTAG-chain.
JP44 (SMD, top side)**:** PROM of COND1-chip in JTAG-chain
1-2 (default)➔ PROM of COND1-chip in JTAG-chain.
2-3 ➔ PROM of COND1-chip **not** in JTAG-chain.
JP45 (SMD, top side)**:** COND1-chip in JTAG-chain
1-2 ➔ COND1-chip in JTAG-chain.
2-3 (default)➔ COND1-chip **not** in JTAG-chain.
JP46 (SMD, top side)**:** PROM of COND2-chip in JTAG-chain
1-2 (default)➔ PROM of COND2-chip in JTAG-chain.
2-3 ➔ PROM of COND2-chip **not** in JTAG-chain.
JP47 (SMD, top side)**:** COND2-chip in JTAG-chain
1-2 ➔ COND2-chip in JTAG-chain.
2-3 (default)➔ COND2-chip **not** in JTAG-chain.
JP48 (SMD, bottom side)**:** REC1-chip in JTAG-chain
1-2 (default)*➔ REC1-chip in JTAG-chain.
2-3 ➔ REC1-chip **not** in JTAG-chain.
* REC1-chip should be always in JTAG-chain, because TMS-line could not be disabled – no jumper in TMS-line for REC1-chip.
JP49 (SMD, bottom side)**:** 1st PROM of REC1-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP50 (SMD, bottom side)**:** 2nd PROM of REC1-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP51 (SMD, bottom side)**:** 3rd PROM of REC1-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP52 (SMD, bottom side)**:** 4th PROM of REC1-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP53 (SMD, bottom side)**:** 1st PROM of REC2-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP54 (SMD, bottom side)**:** 2nd PROM of REC2-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP55 (SMD, bottom side)**:** 3rd PROM of REC2-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP56 (SMD, bottom side)**:** 4th PROM of REC2-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP57 (SMD, bottom side)**:** REC2-chip in JTAG-chain
1-2 (default)*➔ REC2-chip in JTAG-chain.
2-3 ➔ REC2-chip **not** in JTAG-chain.
* REC2-chip should be always in JTAG-chain, because TMS-line could not be disabled – no jumper in TMS-line for REC2-chip.

JP58 (SMD, bottom side)**:** REC3-chip in JTAG-chain
1-2 (default)*➔ REC3-chip in JTAG-chain.
2-3 ➔ REC3-chip **not** in JTAG-chain.
* REC3-chip should be always in JTAG-chain, because TMS-line could not be disabled – no jumper in TMS-line for REC3-chip.
JP59 (SMD, bottom side)**:** 1st PROM of REC3-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP60 (SMD, bottom side)**:** 2nd PROM of REC3-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP61 (SMD, bottom side)**:** 3rd PROM of REC3-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP62 (SMD, bottom side)**:** 4th PROM of REC3-chip in JTAG-chain
1-2 (default)➔ in JTAG-chain.
2-3➔ not in JTAG-chain.
JP63 (SMD, top side)**:** BIASV for IC32
(default)➔ 0Ω inserted.
JP64 (SMD, top side)**:** V_DONE_COND1
(default)➔ 0Ω inserted.
JP65 (SMD, top side)**:** BIASV for IC33
(default)➔ 0Ω inserted.
JP66 (SMD, top side)**:** V_DONE_COND2
(default)➔ 0Ω inserted.
JP67 (SMD, top side)**: "**emergency-jumper" for PORSEL of IC10
(default)➔ nothing inserted.
JP68 (SMD, top side)**: "**emergency-jumper" for PORSEL of IC9
(default)➔ nothing inserted.
JP69 (SMD, top side)**: "**emergency-jumper" for NSYSRES_COND
(default)➔ nothing inserted.
JP70 (SMD, top side)**:** selection of CLK_TO_PLL
1-2 ➔ oscillator-clock (CLK_OSC) selected.
2-3 ➔ clock from backplane (CLK_TIM) selected.
JP71 (SMD, top side)**: "**emergency-jumper" for NSYSRES_REC
(default)➔ nothing inserted.
JP72 and JP73 (SMD, bottom side)**:** not used
(default)➔ nothing inserted.
JP74 (SMD, bottom side)**:** INIT_DONE_FB
R0805 with 1kΩ on 1-2 and connection of JP74/pin 2 with JP75/pin 2.
JP76, JP77, JP78 and JP79 (SMD, bottom side)**:** setting as CARD NUMBER, see following table:

#	JP78	JP79	JP77	JP76
1	0Ω auf 2-3	0Ω auf 2-3	0Ω auf 2-3	10kΩ auf 1-2
2	0Ω auf 2-3	0Ω auf 2-3	10kΩ auf 1-2	0Ω auf 2-3
3	0Ω auf 2-3	0Ω auf 2-3	10kΩ auf 1-2	10kΩ auf 1-2
4	0Ω auf 2-3	10kΩ auf 1-2	0Ω auf 2-3	0Ω auf 2-3

Table 6.10: Jumpers for CARD NUMBER

JP80 (SMD, bottom side)**:** N_IACKIN/N_IACKOUT
ON ➔ always on, no interrupt.
JP81 and JP82 (top side)**:** jumper for LV2V5_VME
(default)➔ solder-bridges after voltage-testing.
JP83 and JP84 (SMD, top side)**:** SEL0 and SEL1 for CDC586
(default)➔ nothing inserted.
JP85 (SMD, top side)**: "**emergency-jumper" for OE# of IC10
(default)➔ nothing inserted.
JP86 (SMD, top side)**: "**emergency-jumper" for CE# of IC10
(default)➔ nothing inserted.
JP87 (SMD, top side)**: "**emergency-jumper" for OE# of IC9

(default)➔ nothing inserted.
JP88 (SMD, top side)**: "**emergency-jumper" for CE# of IC9
(default)➔ nothing inserted.
JP89 and JP90 (SMD, bottom side)**:** VCCO_REC2 selection
1-2 (default)➔ LV1V5_XIL.
2-3➔ LV3V3.
JP91 and JP92 (SMD, bottom side)**:** VCCO_REC3 selection
1-2 (default)➔ LV1V5_XIL.
2-3➔ LV3V3.
JP93 see JP4.
JP94 and JP95 (SMD, bottom side)**:** VCCO_REC1 selection
1-2 (default)➔ LV1V5_XIL.
2-3➔ LV3V3.
X1 and X2: not used in design for jumpers.
X3-X8 (SMD, top side)**:** jumper for SCANPSC
(default)➔ nothing inserted.
X9 (SMD, top side)**:** V_SEL_CABLES
1-2 (default)➔ 0Ω inserted (V_SEL_CABLES to VME-chip).
X10 (SMD, top side)**:** V_SEL_BACKPL
1-2 (default)➔ 0Ω inserted (V_SEL_ BACKPL to VME-chip).
X11: not used in design for jumpers.

7 References

[1] American National Standard for VME64
ANSI/VITA 1-1994, Approved April 10, 1995

[2] American National Standard for VME64 Extensions
ANSI/VITA 1.1-1997, Approved October 7, 1998

[3] CMS Internal Note
CMS Level-1 Global Calorimeter Trigger to Global Trigger and Global Muon Trigger Interfaces, CMS NOTE 2002/069, December 13, 2002

[4] CMS Internal Note
Specification of the Interface between the Global Muon Trigger and the Global Trigger, CMS NOTE 2004/006, January 12, 2004

[5] VMEbus Specification Manual
ANSI/IEEE STD 1014-1987, IEC 821 and 297,
IEEE Standards Board, Approved March 12, 1997