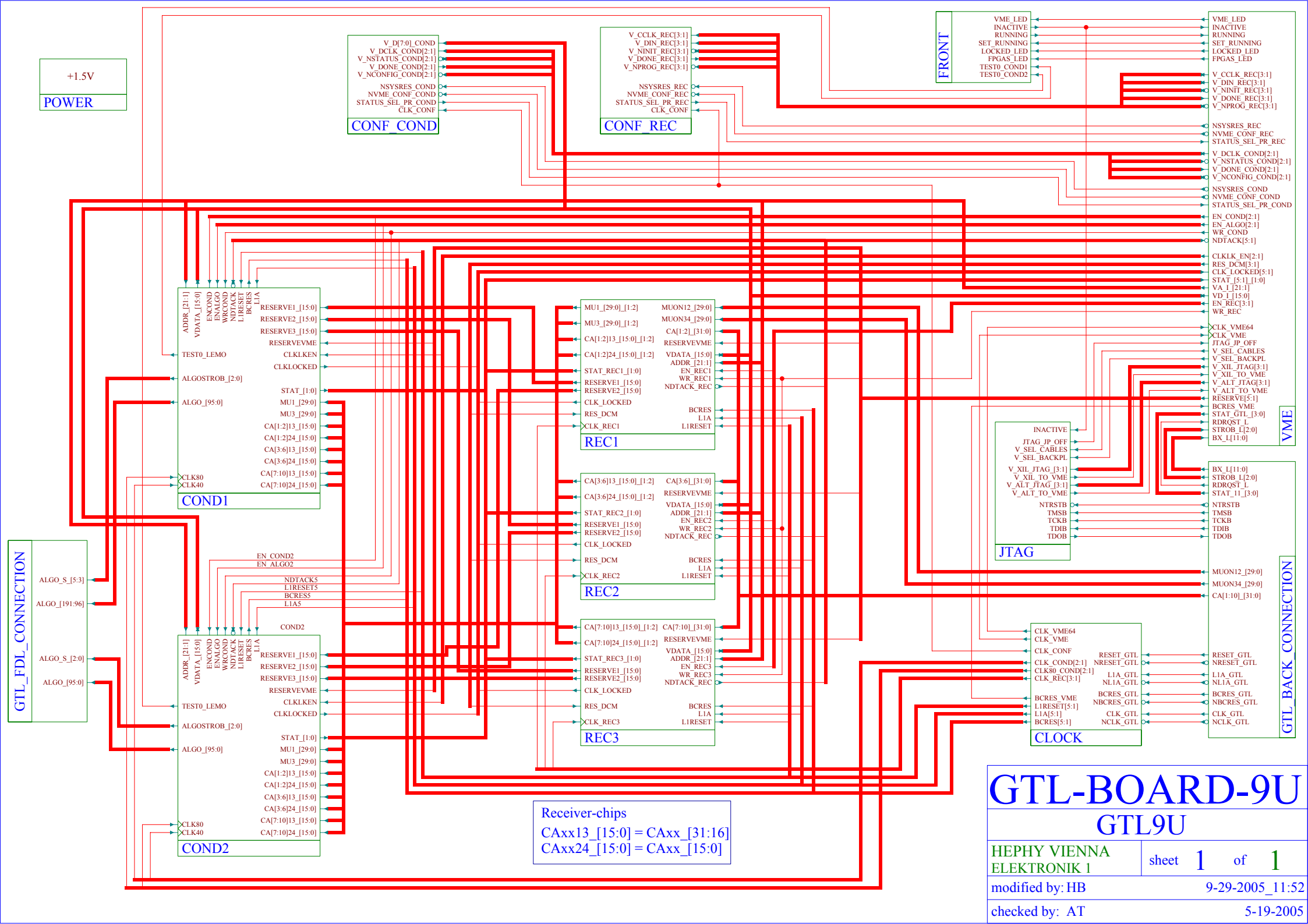
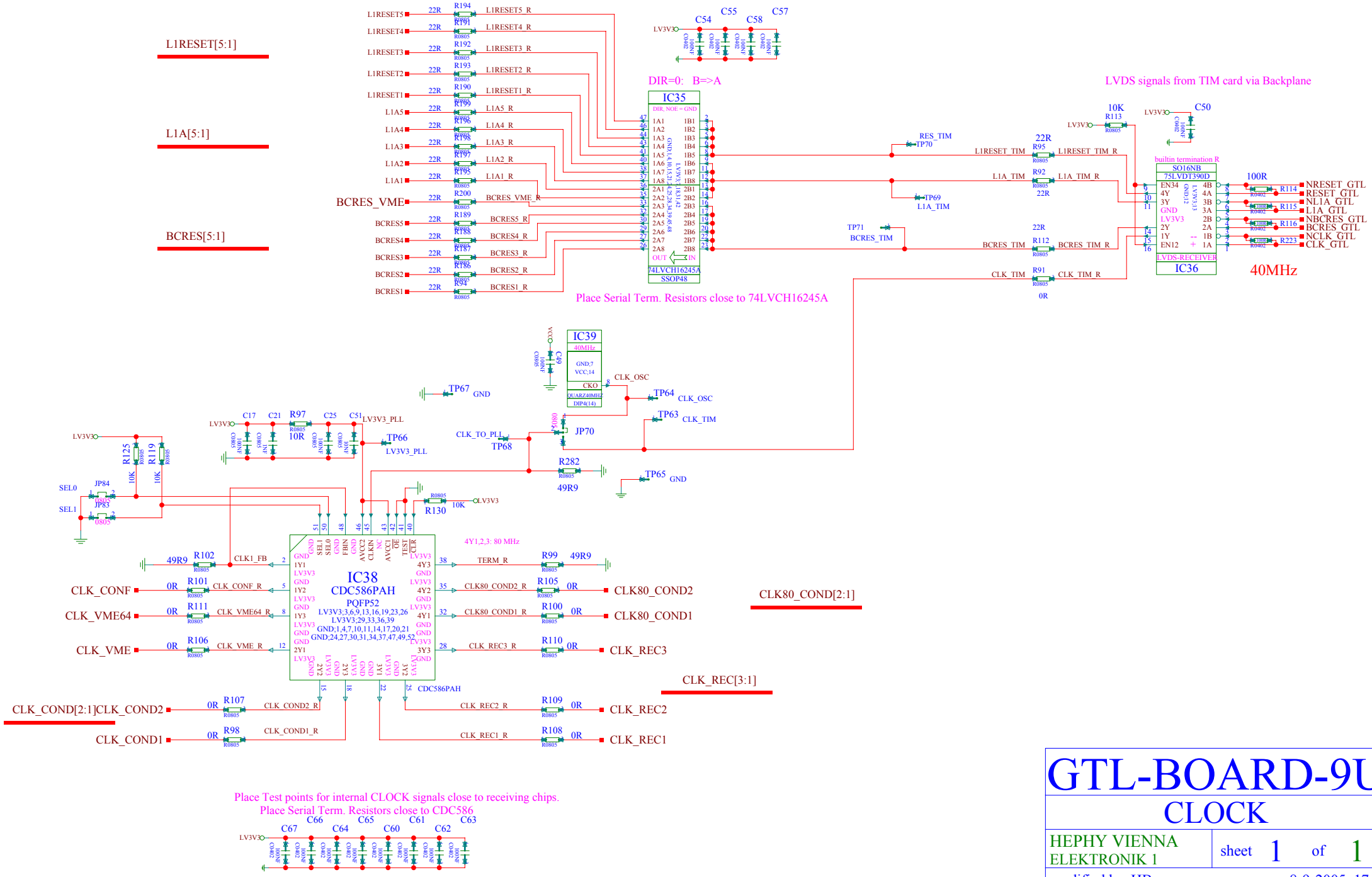

+1.5V
POWER
CONF_COND
V_D[7:0]_COND
V_DCLK_COND[2:1]
V_NSTATUS_COND[2:1]
V_DONE_COND[2:1]
V_NCONFIG_COND[2:1]
NSYSRES_COND
NVME_CONF_COND
STATUS_SEL_PR_COND
CLK_CONF
CONF_REC
V_CCLK_REC[3:1]
V_DIN_REC[3:1]
V_NINIT_REC[3:1]
V_DONE_REC[3:1]
V_NPROG_REC[3:1]
NSYSRES_REC
NVME_CONF_REC
STATUS_SEL_PR_REC
CLK_CONF
FRONT
VME_LED
INACTIVE
RUNNING
SET_RUNNING
LOCKED_LED
FPGAS_LED
TEST0_COND1
TEST0_COND2
VME
COND1
ADDR_[21:1]
VDATA_[15:0]
ENCOND
ENALGO
WRCOND
NDTACK
L1RESET
BCRES
L1A
RESERVE1_[15:0]
RESERVE2_[15:0]
RESERVE3_[15:0]
RESERVEVME
CLKLKEN
CLKLOCKED
TEST0_LEMO
ALGOSTROB_[2:0]
STAT_[1:0]
ALGO_[95:0]
MU1_[29:0]
MU3_[29:0]
CA[1:2]13_[15:0]
CA[1:2]24_[15:0]
CA[3:6]13_[15:0]
CA[3:6]24_[15:0]
CA[7:10]13_[15:0]
CA[7:10]24_[15:0]
CLK80
CLK40
REC1
MU1_[29:0]_[1:2]
MU3_[29:0]_[1:2]
CA[1:2]13_[15:0]_[1:2]
CA[1:2]24_[15:0]_[1:2]
STAT_REC1_[1:0]
RESERVE1_[15:0]
RESERVE2_[15:0]
CLK_LOCKED
RES_DCM
CLK_REC1
MUON12_[29:0]
MUON34_[29:0]
CA[1:2]_[31:0]
RESERVEVME
VDATA_[15:0]
ADDR_[21:1]
EN_REC1
WR_REC1
NDTACK_REC
BCRES
L1A
L1RESET
REC2
CA[3:6]13_[15:0]_[1:2]
CA[3:6]24_[15:0]_[1:2]
STAT_REC2_[1:0]
RESERVE1_[15:0]
RESERVE2_[15:0]
CLK_LOCKED
RES_DCM
CLK_REC2
CA[3:6]_[31:0]
RESERVEVME
VDATA_[15:0]
ADDR_[21:1]
EN_REC2
WR_REC2
NDTACK_REC
BCRES
L1A
L1RESET
REC3
CA[7:10]13_[15:0]_[1:2]
CA[7:10]24_[15:0]_[1:2]
STAT_REC3_[1:0]
RESERVE1_[15:0]
RESERVE2_[15:0]
CLK_LOCKED
RES_DCM
CLK_REC3
CA[7:10]_[31:0]
RESERVEVME
VDATA_[15:0]
ADDR_[21:1]
EN_REC3
WR_REC3
NDTACK_REC
BCRES
L1A
L1RESET
JTAG
INACTIVE
JTAG_JP_OFF
V_SEL_CABLES
V_SEL_BACKPL
V_XIL_JTAG_[3:1]
V_XIL_TO_VME
V_ALT_JTAG_[3:1]
V_ALT_TO_VME
NTRSTB
TMSB
TCKB
TDIB
TDOB
CLOCK
CLK_VME64
CLK_VME
CLK_CONF
CLK_COND[2:1]
CLK80_COND[2:1]
CLK_REC[3:1]
BCRES_VME
L1RESET[5:1]
L1A[5:1]
BCRES[5:1]
RESET_GTL
NRESET_GTL
L1A_GTL
NL1A_GTL
BCRES_GTL
NBCRES_GTL
CLK_GTL
NCLK_GTL
GTL_FDL_CONNECTION
ALGO_S_[5:3]
ALGO_[191:96]
ALGO_S_[2:0]
ALGO_[95:0]
EN_COND2
EN_ALGO2
NDTACK5
L1RESET5
BCRES5
L1A5
COND2
GTL_BACK_CONNECTION
CLK_VME64
CLK_VME
JTAG_JP_OFF
V_SEL_CABLES
V_SEL_BACKPL
V_XIL_JTAG[3:1]
V_XIL_TO_VME
V_ALT_JTAG[3:1]
V_ALT_TO_VME
RESERVE[5:1]
BCRES_VME
STAT_GTL_[3:0]
RDRQST_L
STROB_L[2:0]
BX_L[11:0]
STAT_11_[3:0]
NTRSTB
TMSB
TCKB
TDIB
TDOB
MUON12_[29:0]
MUON34_[29:0]
CA[1:10]_[31:0]
RESET_GTL
NRESET_GTL
L1A_GTL
NL1A_GTL
BCRES_GTL
NBCRES_GTL
CLK_GTL
NCLK_GTL
EN_COND[2:1]
EN_ALGO[2:1]
WR_COND
NDTACK[5:1]
CLKLK_EN[2:1]
RES_DCM[3:1]
CLK_LOCKED[5:1]
STAT_[5:1]_[1:0]
VA_I_[21:1]
VD_I_[15:0]
EN_REC[3:1]
WR_REC
Receiver-chips
CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]
GTL-BOARD-9U
GTL9U
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by: HB
9-29-2005_11:52
checked by: AT
5-19-2005

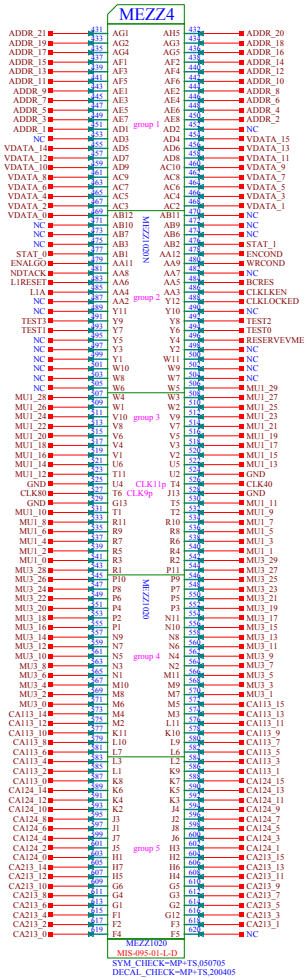


GTL-BOARD-9U

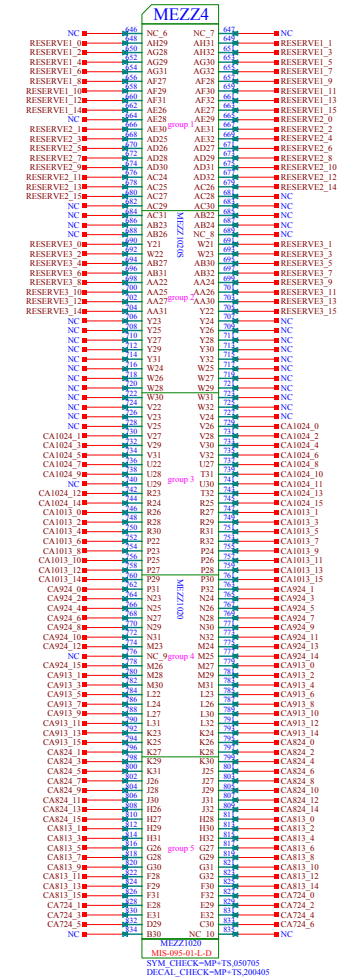
CLOCK

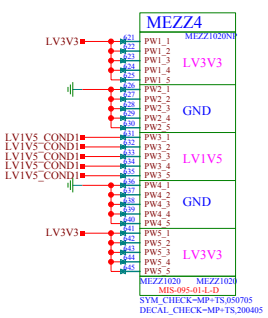
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: HB	8-9-2005_17:40
checked by: AT	8-8-2005_13:41

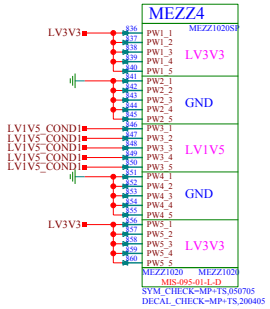
NORD MIS_095 connector



SOUTH MIS_095 connector





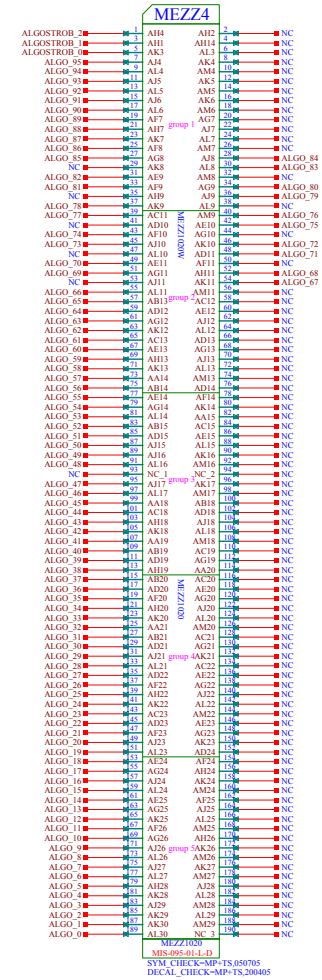


MEZZ1020

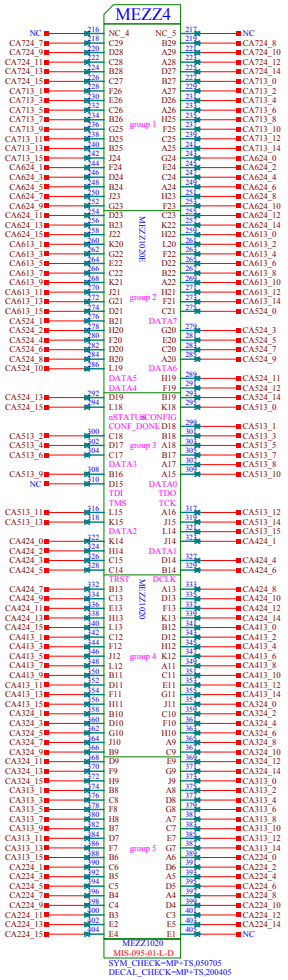
COND1

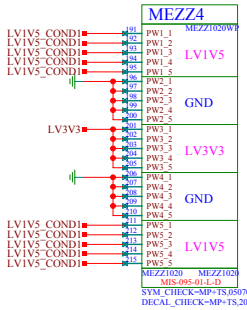
HEPHY VIENNA ELEKTRONIK 1	sheet	1	of 3
modified by: HB280604			7-5-2005_11:15
checked by: CHECKER			0-00-0000_00:00

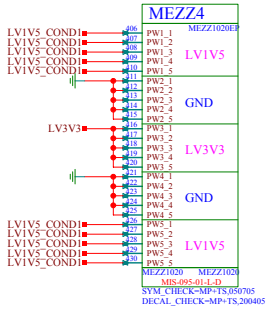
WEST MIS_095 connector



EAST MIS_095 connector



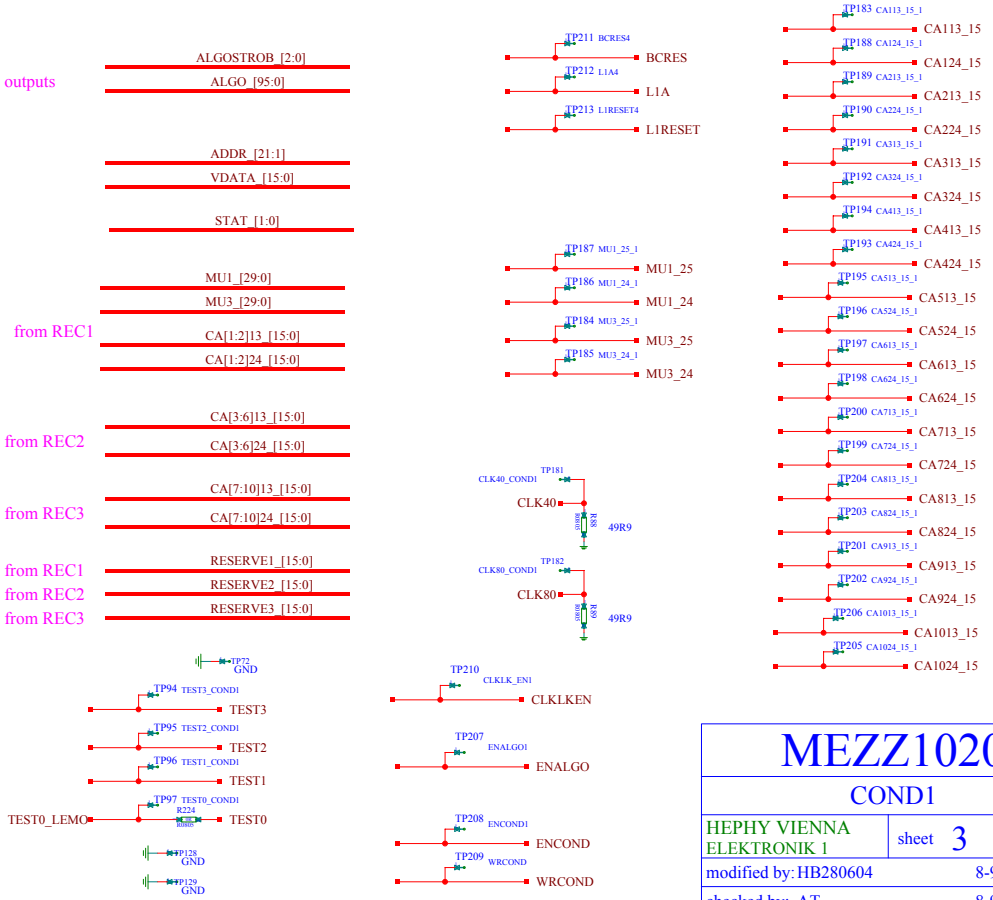




MEZZ1020

COND1

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB280604	7-5-2005_11:09
checked by: CHECKER	0-00-0000_00:00

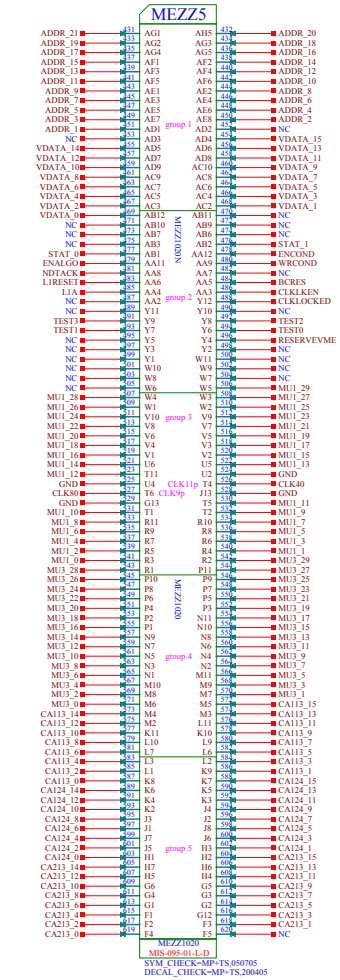


MEZZ1020

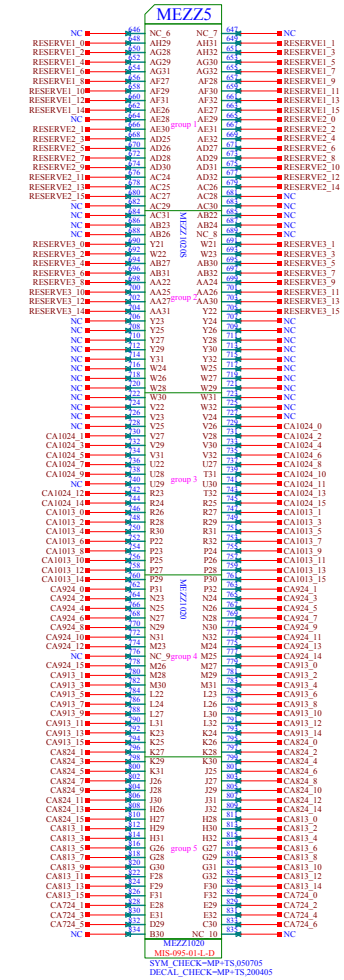
COND1

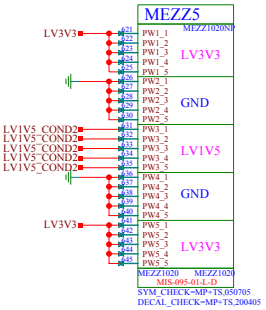
HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB280604	8-9-2005_16:52
checked by: AT	8-9-2005_16:42

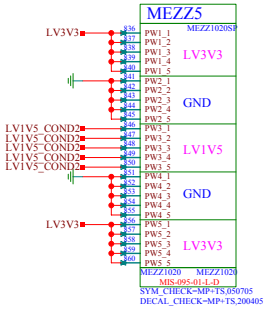
NORD MIS_095 connector



SOUTH MIS_095 connector





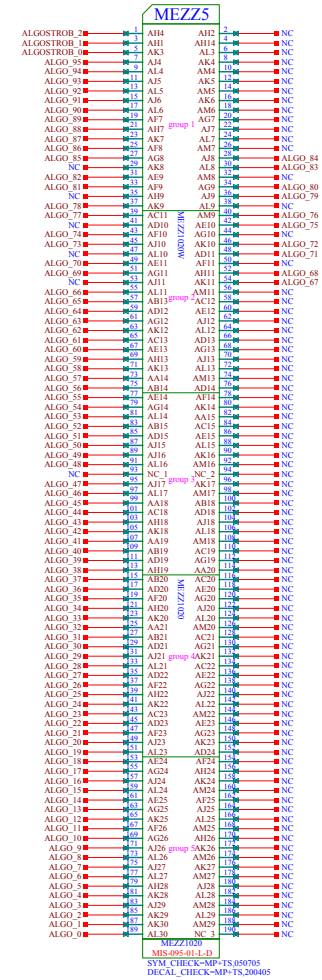


MEZZ1020

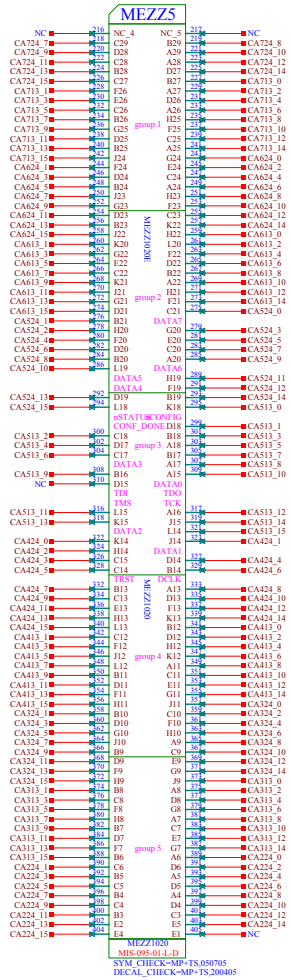
COND2

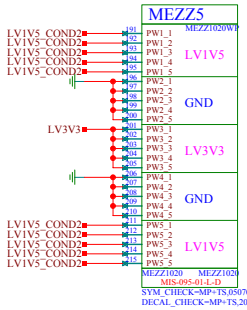
HEPHY VIENNA ELEKTRONIK 1	sheet	1	of 3
modified by: HB280604			7-5-2005_11:09
checked by: CHECKER			0-00-0000_00:00

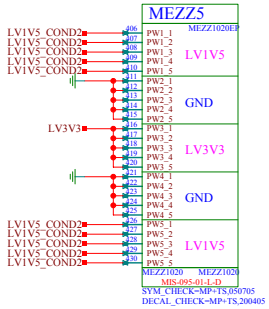
WEST MIS_095 connector



EAST MIS_095 connector



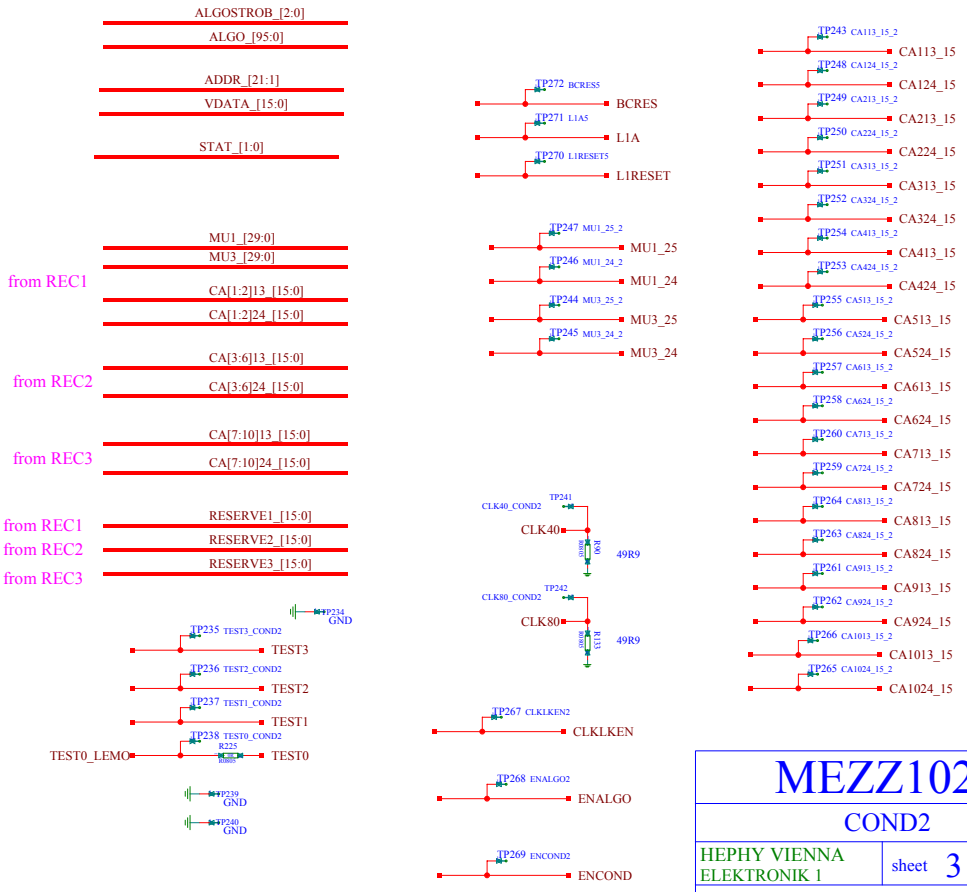




MEZZ1020

COND2

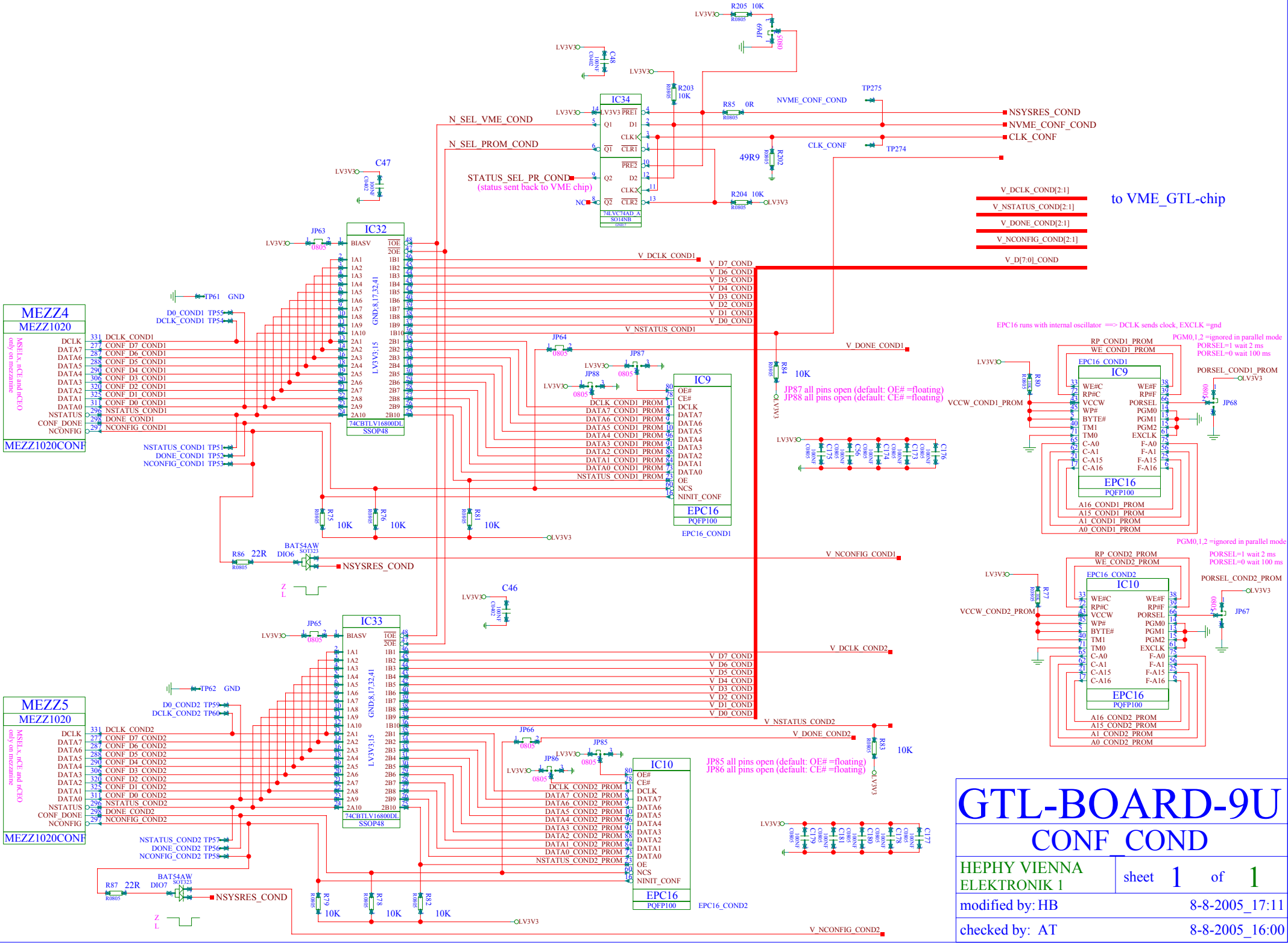
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB280604	7-5-2005_11:09
checked by: CHECKER	0-00-0000_00:00

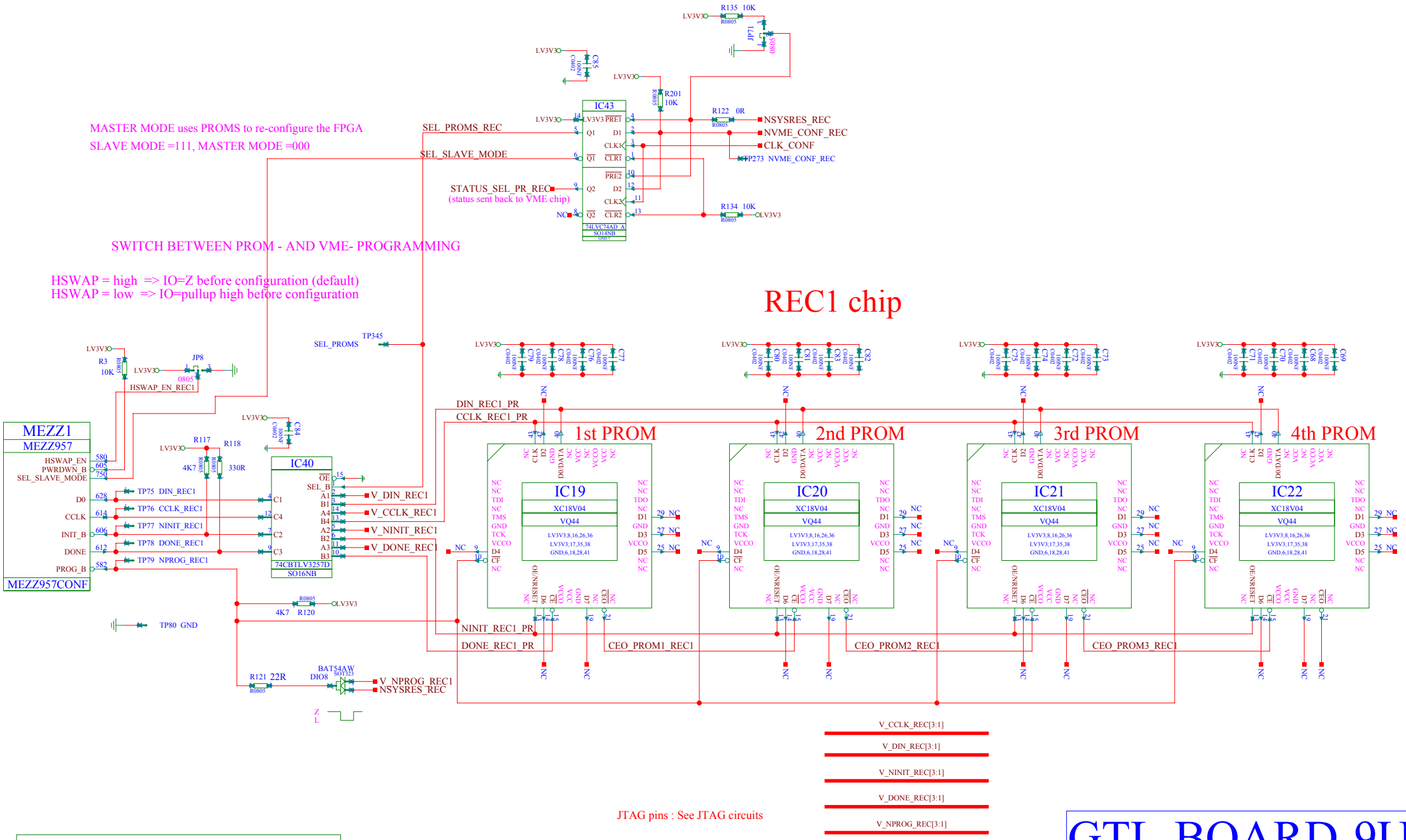


MEZZ1020

COND2

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB280604	8-9-2005_16:49
checked by: CHECKER	0-00-0000_00:00


R205 10K
JP69
NVME_CONF_COND
TP275
R85 0R
NSYSRES_COND
NVME_CONF_COND
CLK_CONF
TP274
R203 10K
IC34
74LVC74AD_A
SO14NB
49R9
R202
R204 10K
N_SEL_VME_COND
N_SEL_PROM_COND
STATUS_SEL_PR_COND
(status sent back to VME chip)
C47
C48
C46
V_DCLK_COND[2:1]
V_NSTATUS_COND[2:1]
V_DONE_COND[2:1]
V_NCONFIG_COND[2:1]
V_D[7:0]_COND
to VME_GTL-chip
IC32
IC33
JP63
JP64
JP65
JP66
JP87
JP88
JP85
JP86
V_DCLK_COND1
V_D7_COND
V_D6_COND
V_D5_COND
V_D4_COND
V_D3_COND
V_D2_COND
V_D1_COND
V_D0_COND
V_NSTATUS_COND1
V_DONE_COND1
V_NCONFIG_COND1
V_DCLK_COND2
V_NSTATUS_COND2
V_DONE_COND2
V_NCONFIG_COND2
JP87 all pins open (default: OE# =floating)
JP88 all pins open (default: CE# =floating)
JP85 all pins open (default: OE# =floating)
JP86 all pins open (default: CE# =floating)
MEZZ4
MEZZ1020
MEZZ1020CONF
MEZZ5
MEZZ1020
MEZZ1020CONF
MSELx, nCE and nCEO only on mezzanine
D0_COND1 TP55
DCLK_COND1 TP54
NSTATUS_COND1 TP51
DONE_COND1 TP52
NCONFIG_COND1 TP53
D0_COND2 TP59
DCLK_COND2 TP60
NSTATUS_COND2 TP57
DONE_COND2 TP56
NCONFIG_COND2 TP58
TP61 GND
TP62 GND
R75 10K
R76 10K
R81 10K
R79 10K
R78 10K
R82 10K
R84 10K
R83 10K
R86 22R
R87 22R
BAT54AW
DIO6
DIO7
NSYSRES_COND
IC9
IC10
EPC16
PQFP100
EPC16_COND1
EPC16_COND2
EPC16 runs with internal oscillator ==> DCLK sends clock, EXCLK =gnd
PGM0,1,2 =ignored in parallel mode
PORSEL=1 wait 2 ms
PORSEL=0 wait 100 ms
RP_COND1_PROM
WE_COND1_PROM
EPC16_COND1
PORSEL_COND1_PROM
VCCW_COND1_PROM
JP68
A16_COND1_PROM
A15_COND1_PROM
A1_COND1_PROM
A0_COND1_PROM
RP_COND2_PROM
WE_COND2_PROM
EPC16_COND2
PORSEL_COND2_PROM
VCCW_COND2_PROM
JP67
A16_COND2_PROM
A15_COND2_PROM
A1_COND2_PROM
A0_COND2_PROM
GTL-BOARD-9U
CONF_COND
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by: HB 8-8-2005_17:11
checked by: AT 8-8-2005_16:00



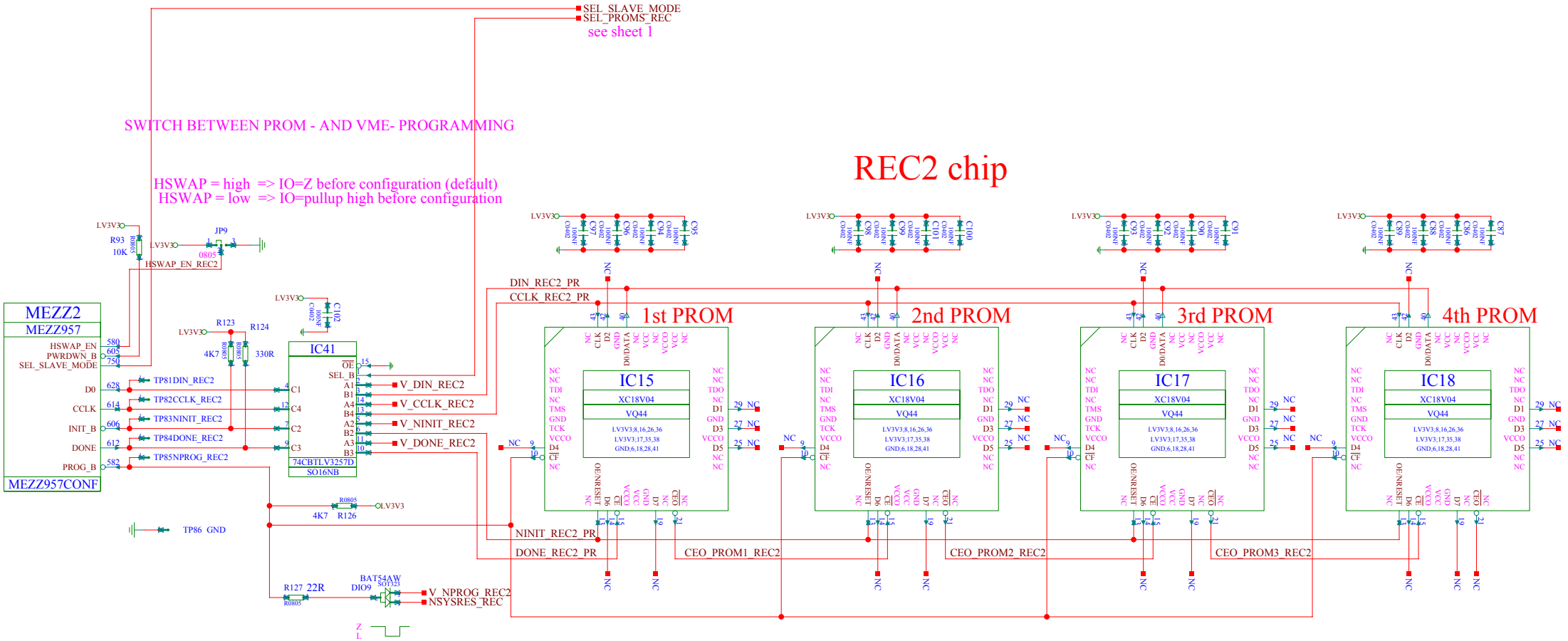
See CHIP schematic to find:
HSWAP_EN_xxx
NPWRDWN_B
DOUT_xxx
On Mezzanine boards you find: M0,M1,M2

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

GTL-BOARD-9U

CONF_REC

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3
modified by: HB	8-10-2005_9:03
checked by: AT	8-8-2005_17:34



JTAG pins : See JTAG circuits

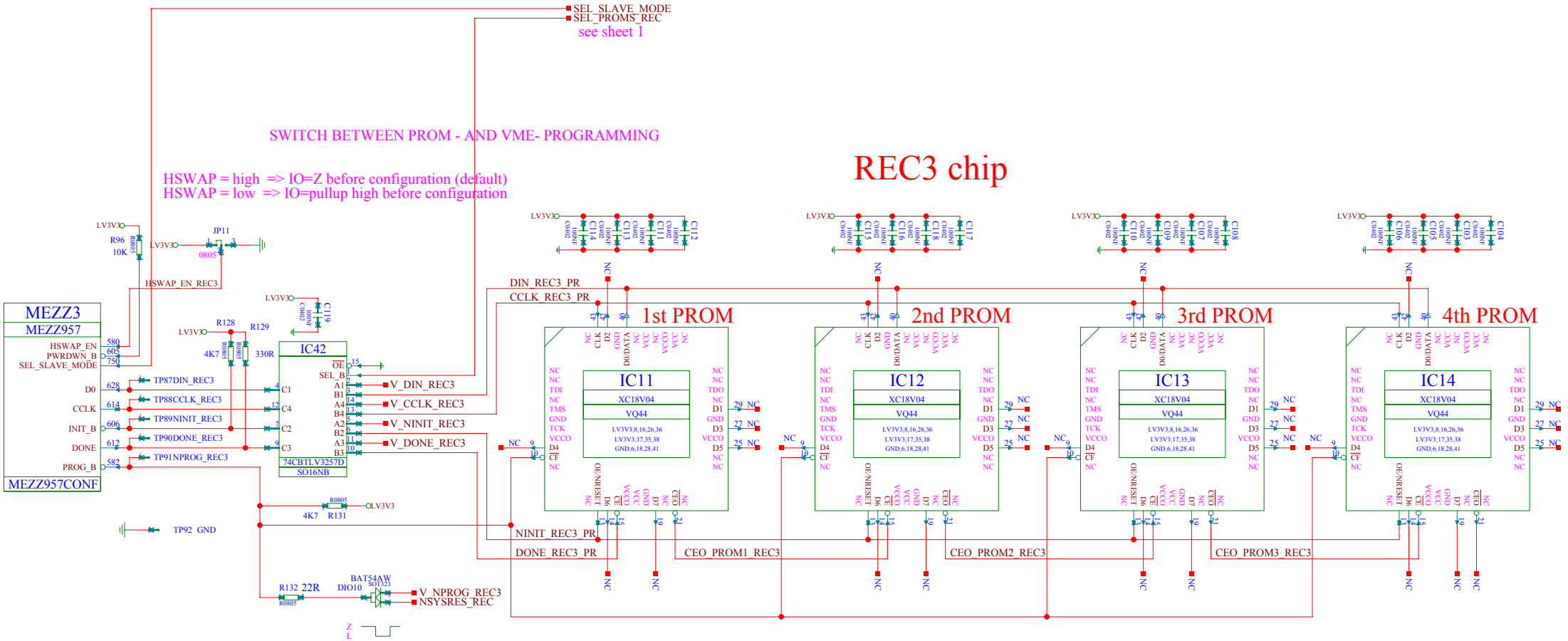
See CHIP schematic to find:
HSWAP_EN_xxx
NPWRDWN_B
DOUT_xxx
On Mezzanine boards you find: M0,M1,M2

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

GTL-BOARD-9U

CONF_REC

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB	8-8-2005_17:38
checked by: AT	8-8-2005_17:34



JTAG pins : See JTAG circuits

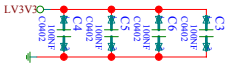
See CHIP schematic to find:
HSWAP_EN_xxx
NPWRDWN_B
DOUT_xxx
On Mezzanine boards you find: M0,M1,M2

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

GTL-BOARD-9U

CONF_REC

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB	8-8-2005_17:39
checked by: AT	8-8-2005_17:34



DISPLAY

leds mounted above all connectors on frontpanel

Front Panel Text

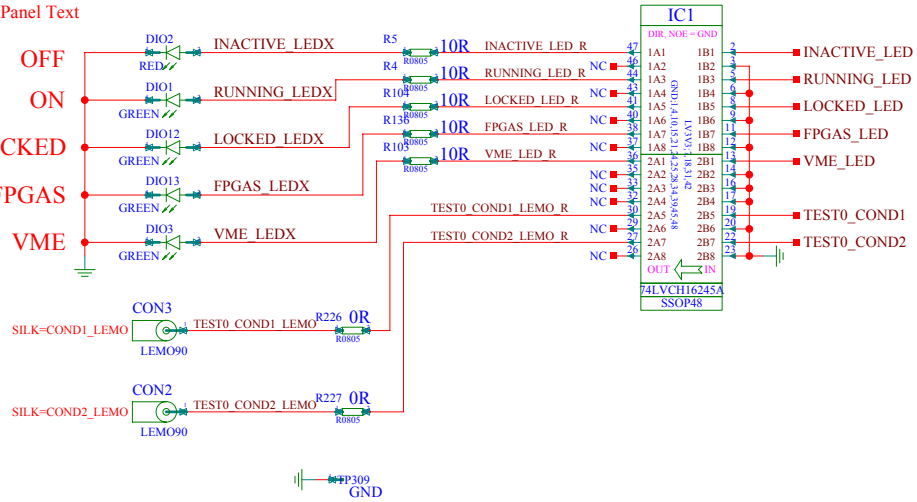
OFF

ON

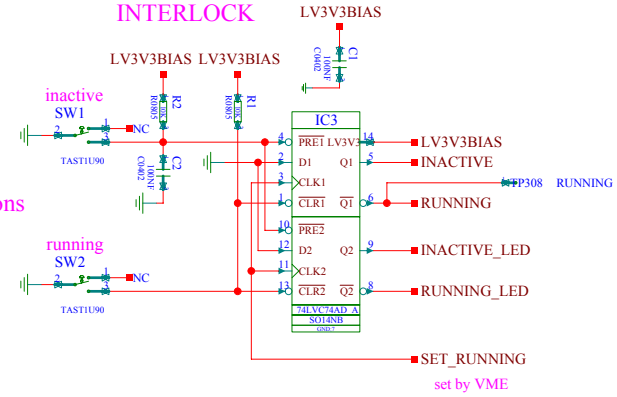
LOCKED

FPGAS

VME



INTERLOCK



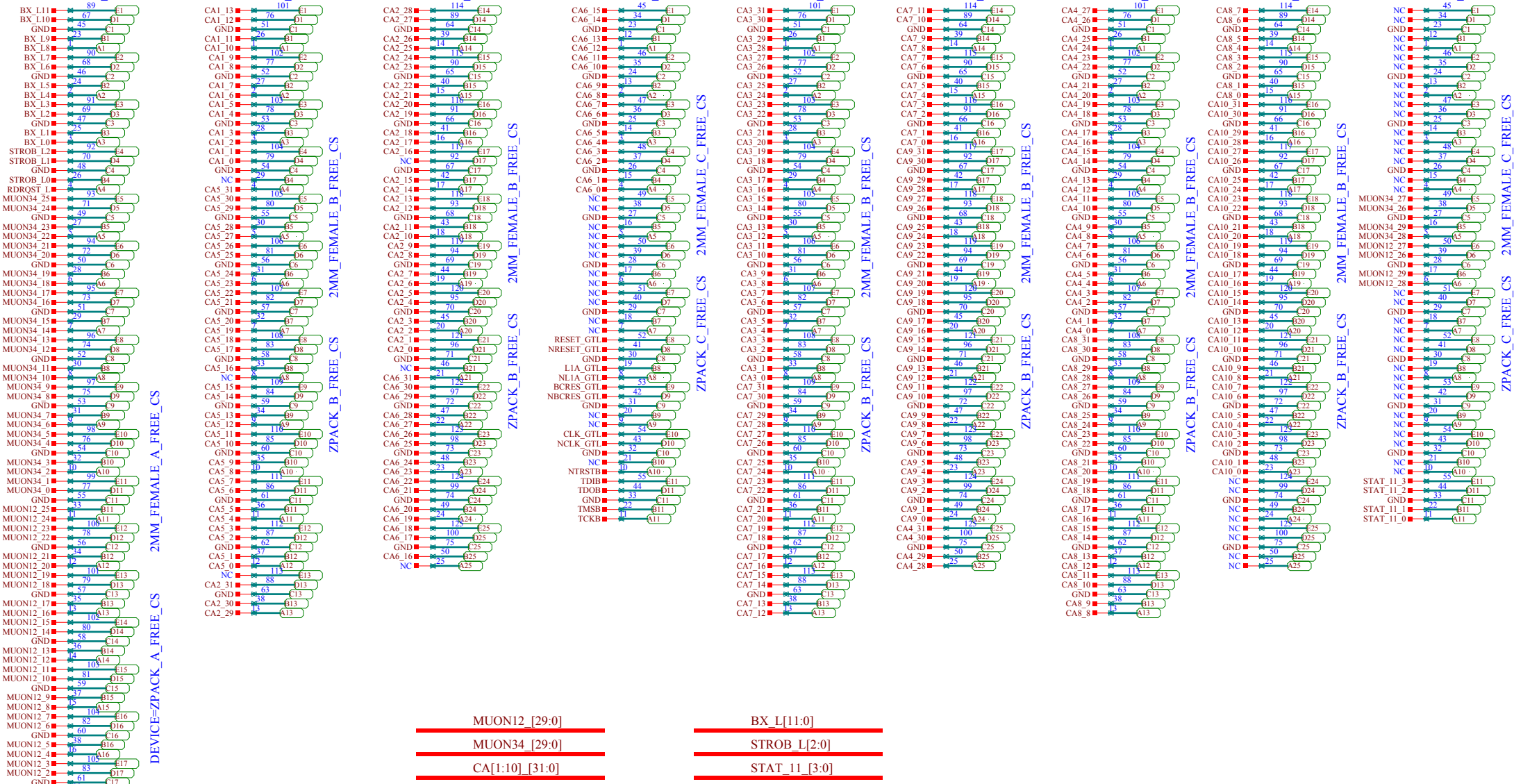
Front Panel buttons

Front Panel Drills

GTL-BOARD-9U

FRONT

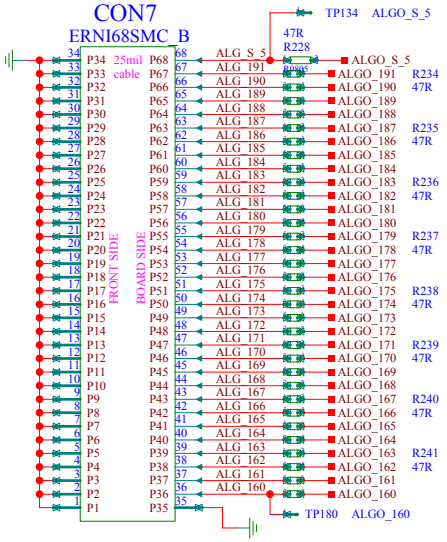
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: HB	8-9-2005_17:43
checked by: AT	7-4-2005_14:24

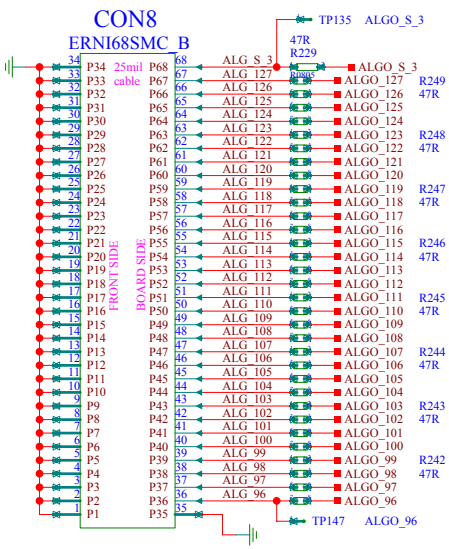


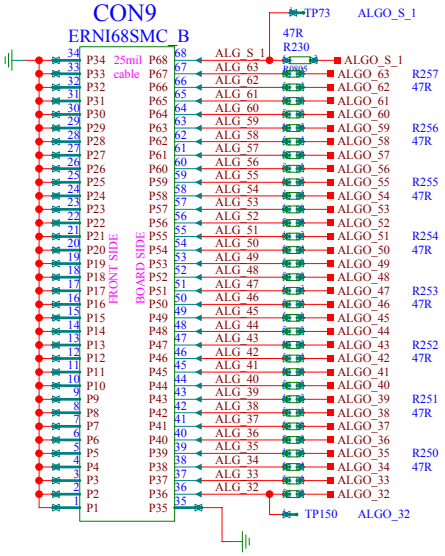
GTL-BOARD-9U

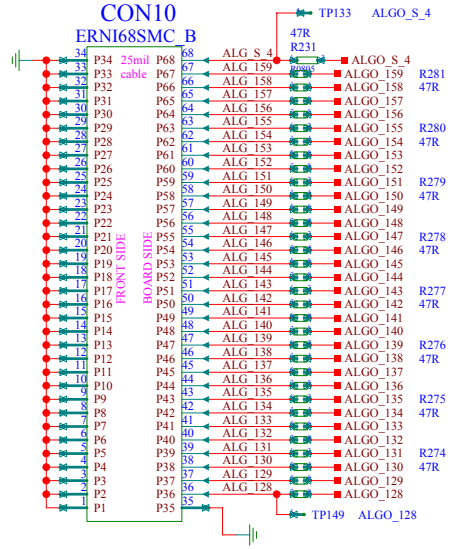
GTL_BACK_CONNECTION

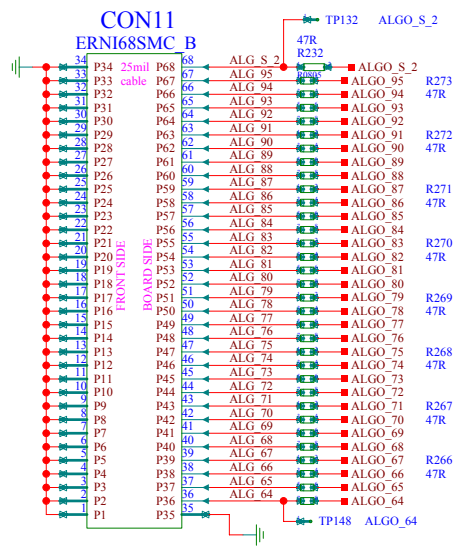
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: HB	8-9-2005_9:13
checked by: AT	2-28-2005_13:57

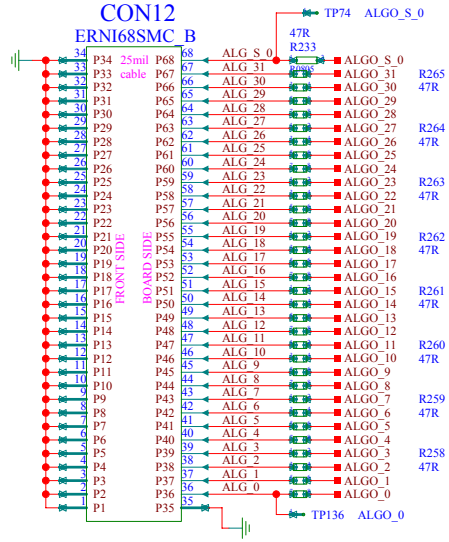












ALGO_S_[5:3]

ALGO_S_[2:0]

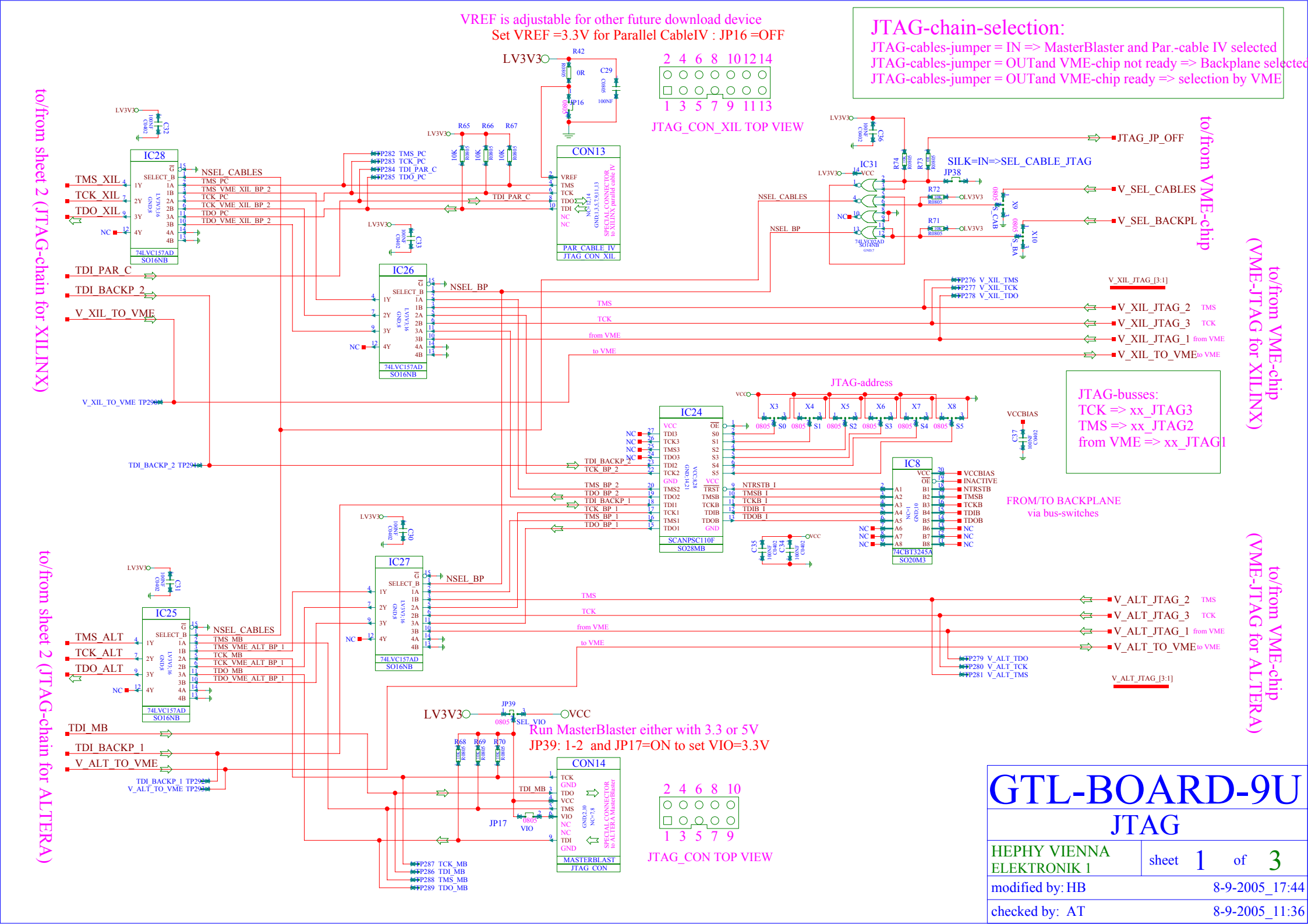
ALGO_[191:96]

ALGO_[95:0]

GTL-BOARD-9U

GTL_FDL_CONNECTION

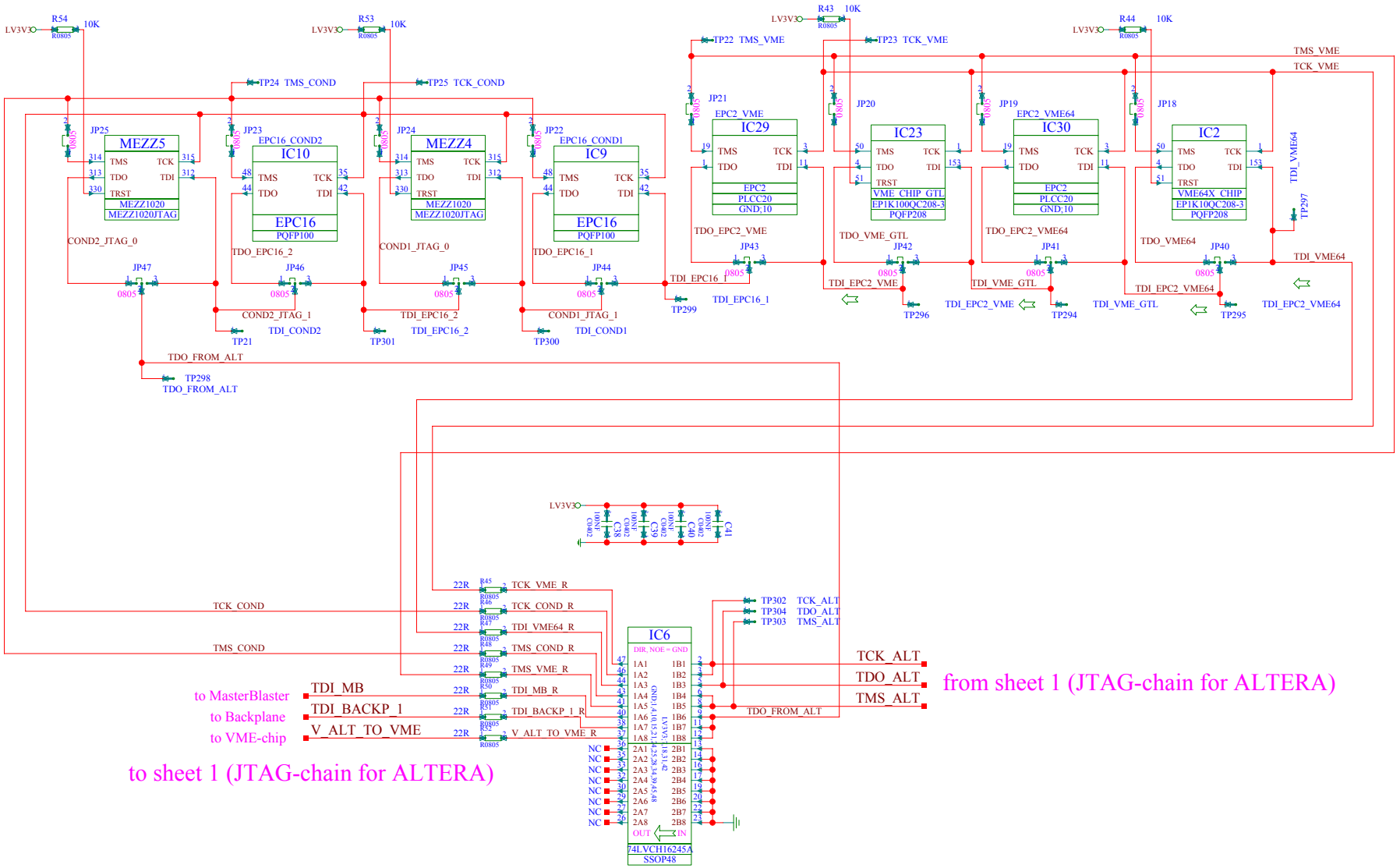
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1	
modified by: HB		7-4-2005_14:29
checked by: AT		6-1-2005_9:09



GTL-BOARD-9U

JTAG

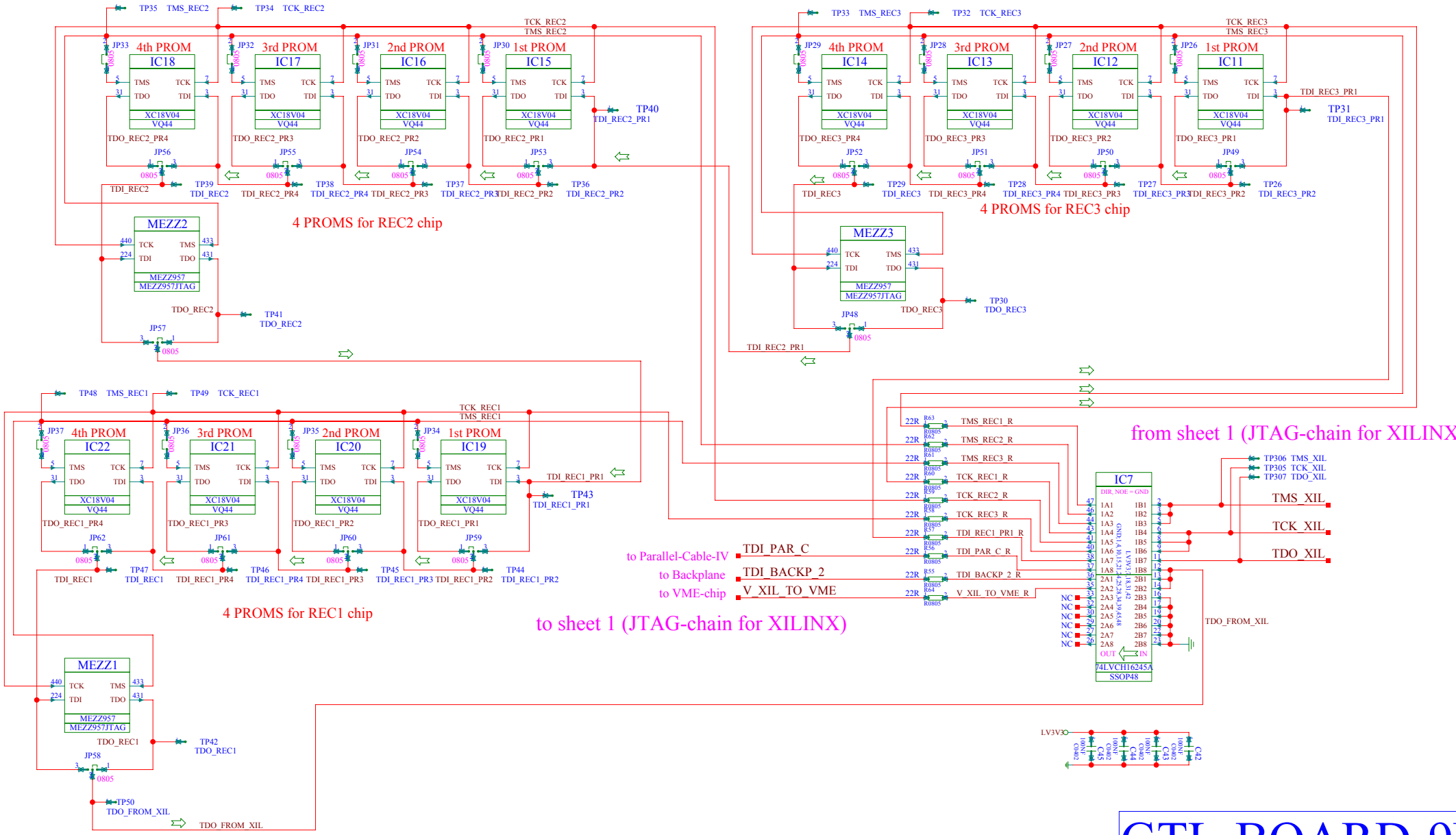
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3
modified by: HB	8-9-2005_17:44
checked by: AT	8-9-2005_11:36



GTL-BOARD-9U

JTAG

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB	8-9-2005_17:46
checked by: AT	8-9-2005_12:00

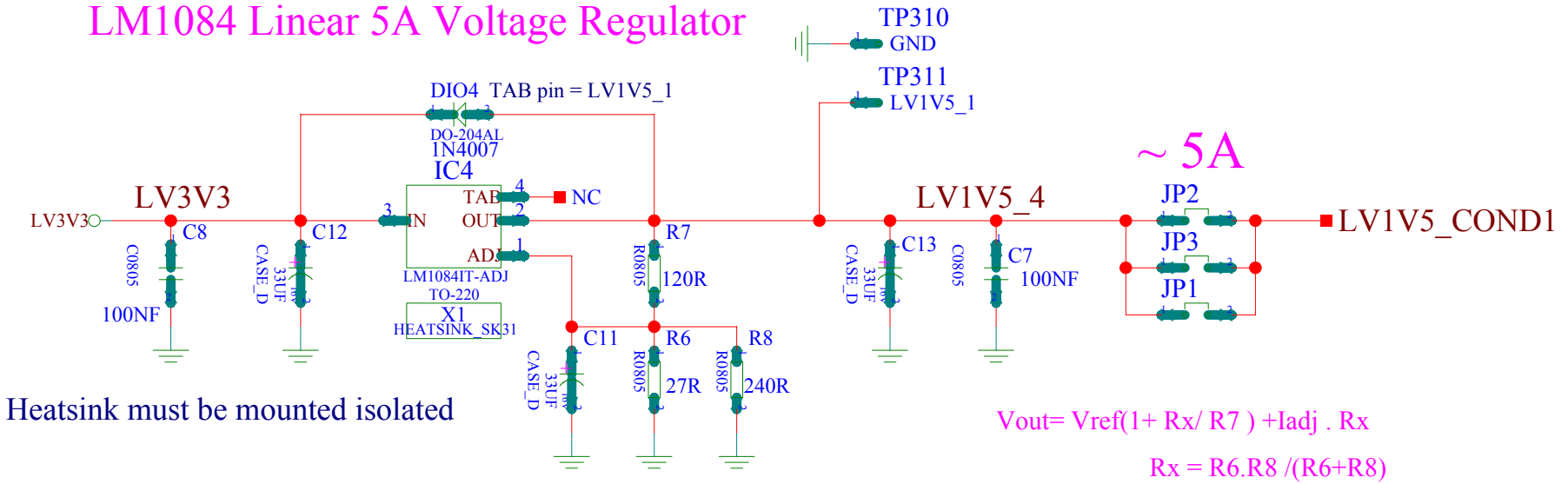


GTL-BOARD-9U

JTAG

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB	8-9-2005_17:50
checked by: AT	8-9-2005_12:10

LM1084 Linear 5A Voltage Regulator



Heatsink must be mounted isolated

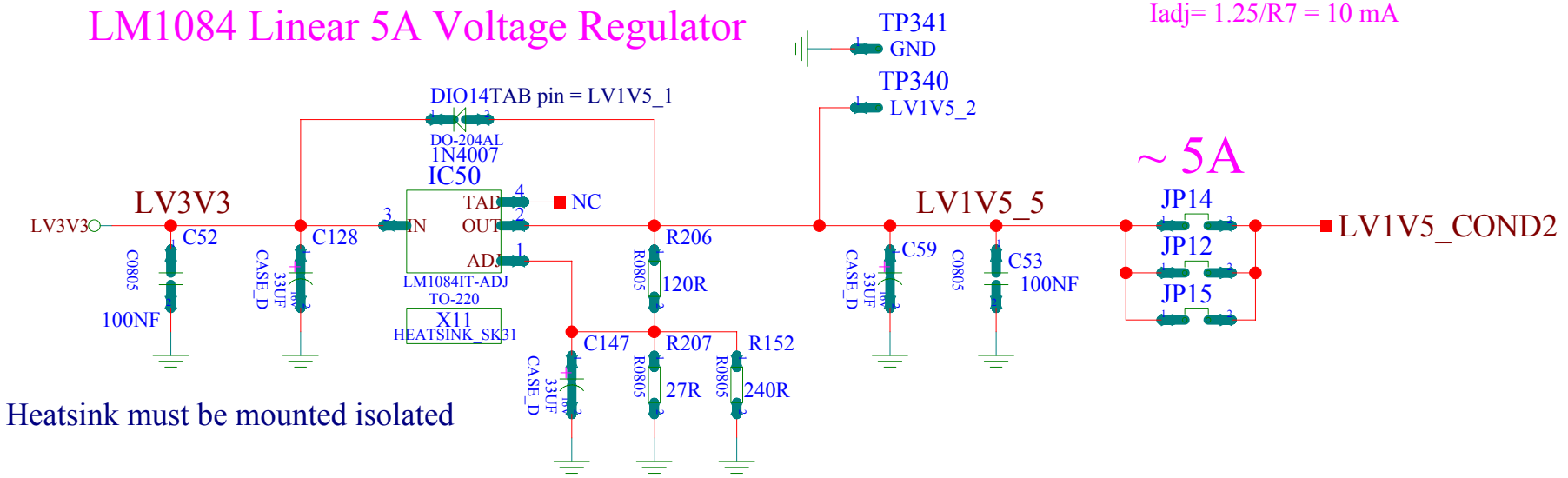
Vout= Vref(1+ Rx/ R7) +Iadj . Rx

Rx = R6.R8 /(R6+R8)

Vref=1.25V

Iadj= 1.25/R7 = 10 mA

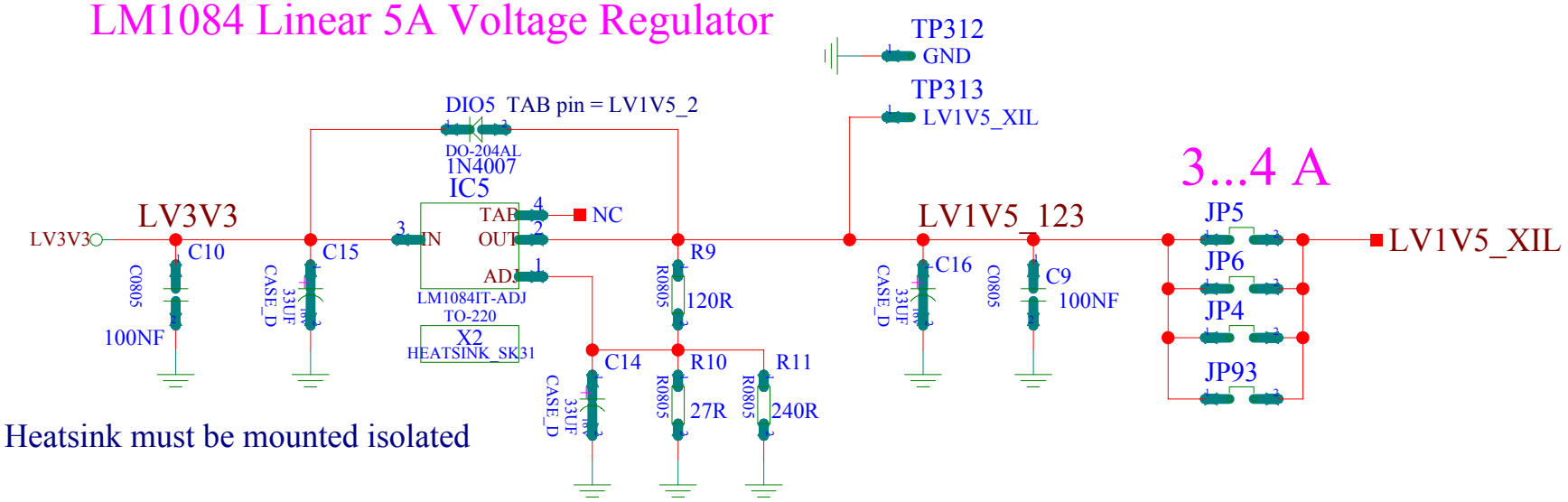
LM1084 Linear 5A Voltage Regulator



Heatsink must be mounted isolated

GTL-BOARD-9U	
POWER	
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 2
modified by: HB	8-9-2005_12:28
checked by: AT	8-9-2005_12:10

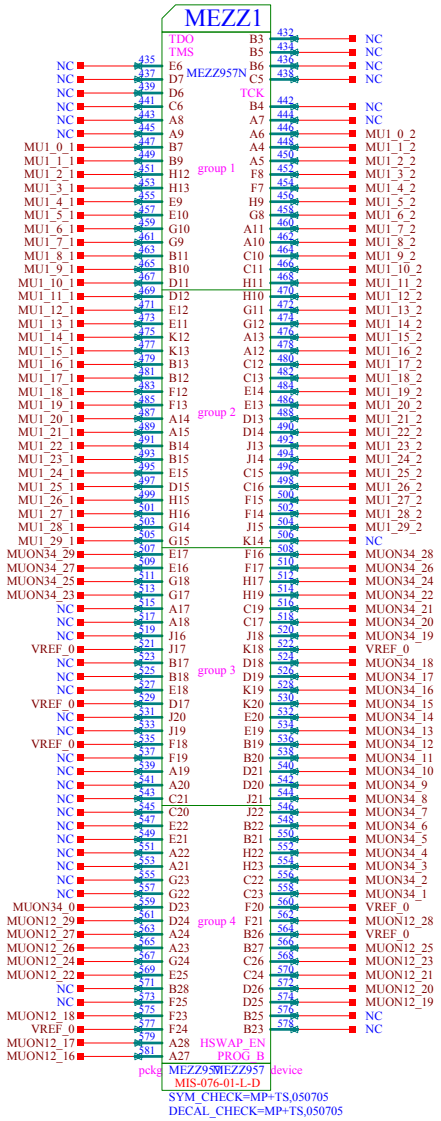
LM1084 Linear 5A Voltage Regulator



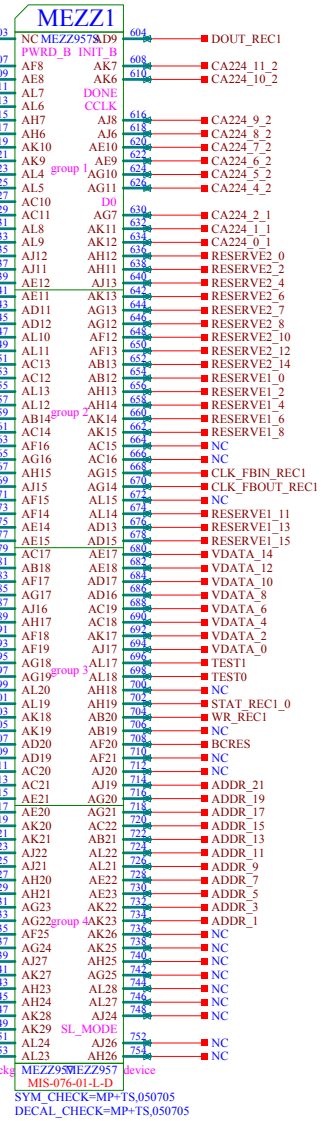
Heatsink must be mounted isolated

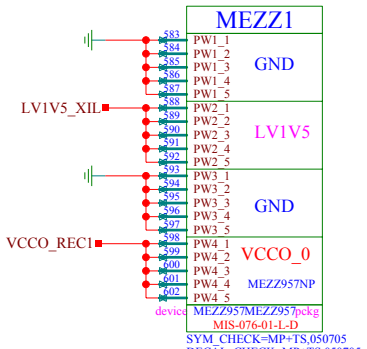
GTL-BOARD-9U	
POWER	
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 2
modified by: HB	8-9-2005_12:29
checked by: AT	8-8-2005_10:23

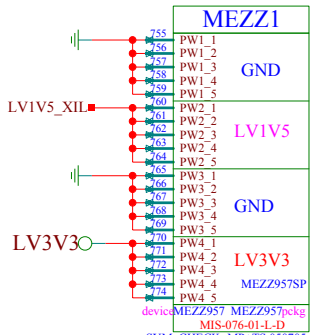
NORD MIS_076 connector



SOUTH MIS_076 connector







Receiver-chips

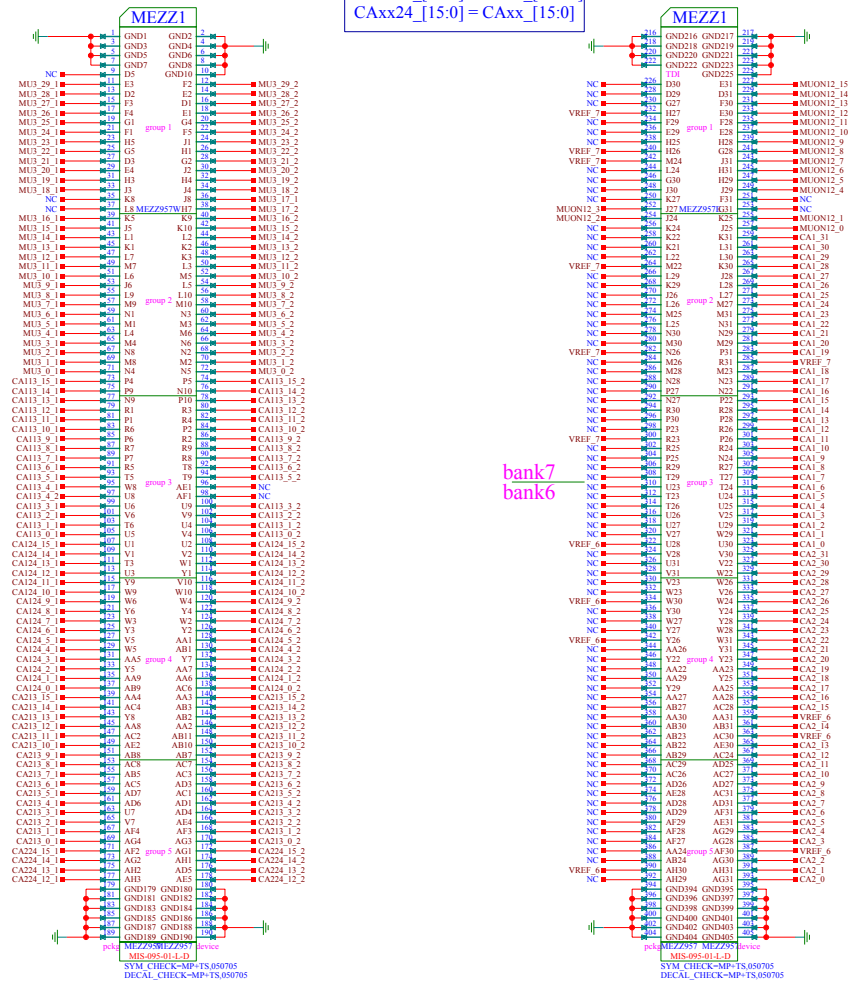
CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]

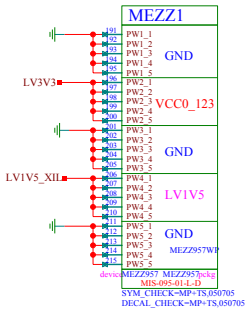
MEZZ957		
REC1		
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3	
modified by: HB	8-8-2005 11:06	
checked by: CHECKER	0-00-0000 00:00	

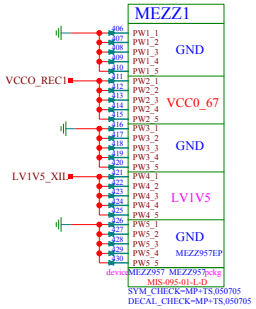
WEST MIS_095 connector

Receiver-chips
CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]

EAST MIS_095 connector



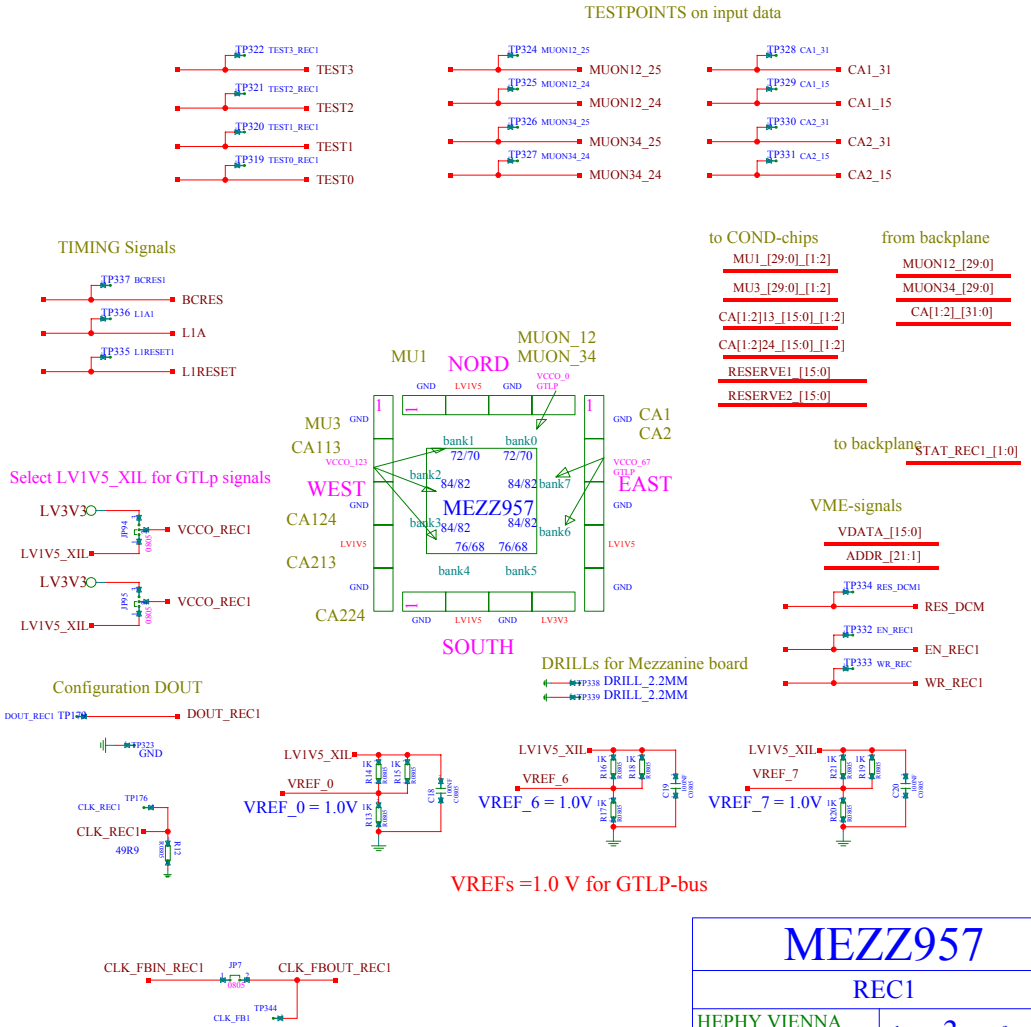




MEZZ957

REC1

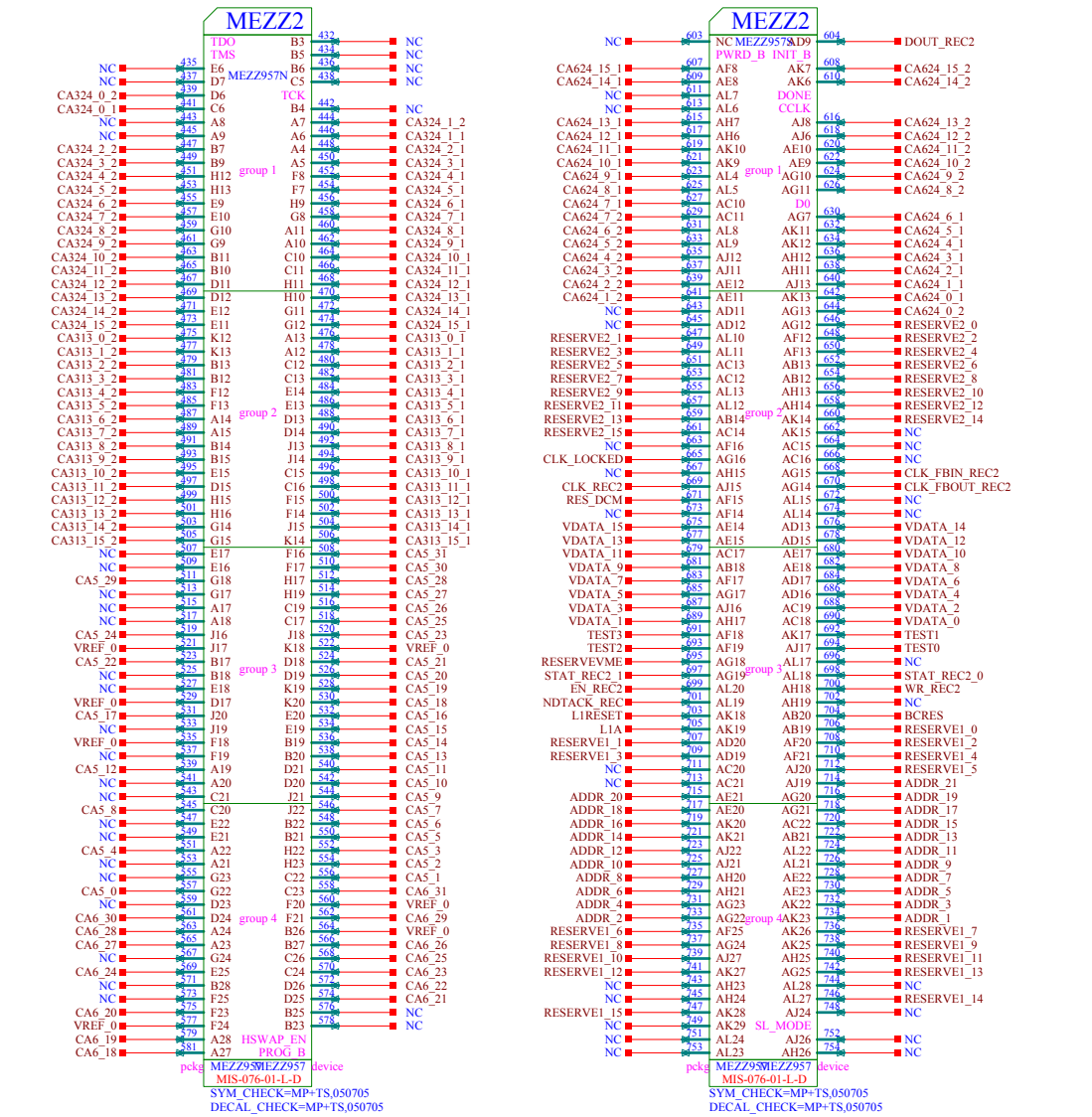
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB	8-8-2005_11:06
checked by: CHECKER	0-00-0000_00:00



MEZZ957

REC1

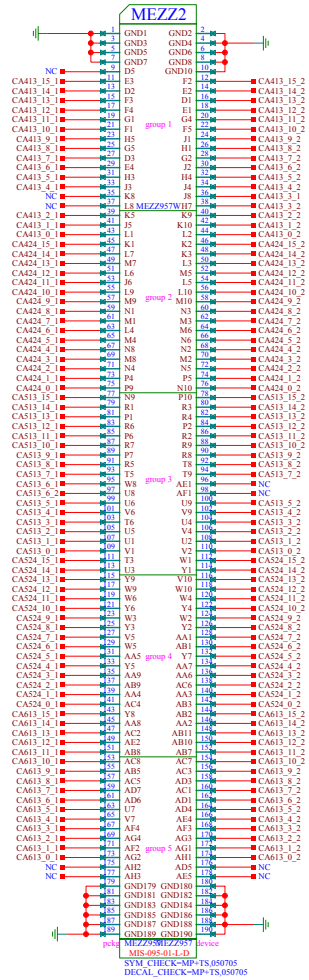
HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB	8-9-2005_17:24
checked by: AT	8-9-2005_17:01

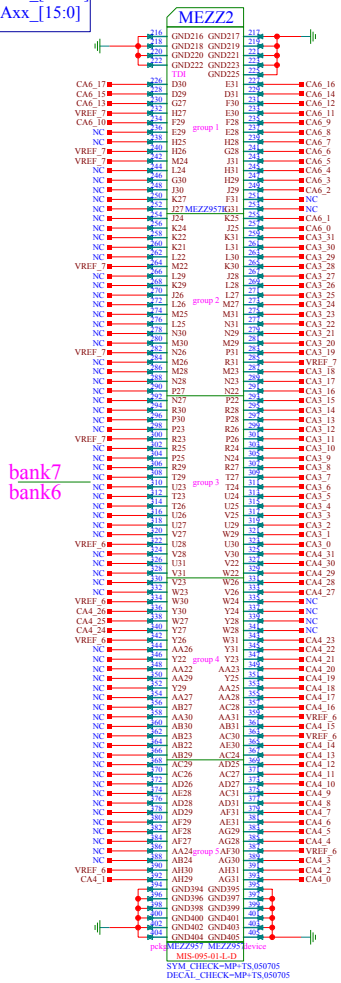

NORD MIS_076 connector
SOUTH MIS_076 connector
MEZZ2
MEZZ957N
MEZZ957S
MEZZ957NP
MEZZ957SP
MIS-076-01-L-D
SYM_CHECK=MP+TS,050705
DECAL_CHECK=MP+TS,050705
GND
LV1V5
LV3V3
VCCO_0
LV1V5_XIL
VCCO_REC2
Receiver-chips
CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]
MEZZ957
REC2
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 3
modified by: HB 8-8-2005 11:25
checked by: CHECKER 0-00-0000 00:00

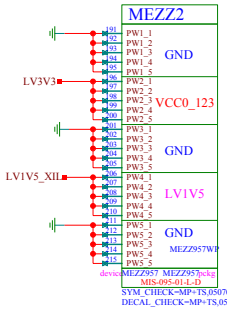
WEST MIS_095 connector

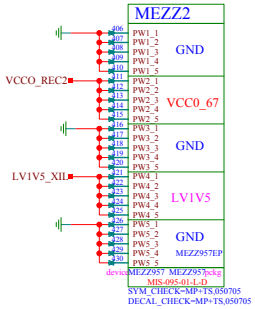
Receiver-chips
CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]

EAST MIS_095 connector





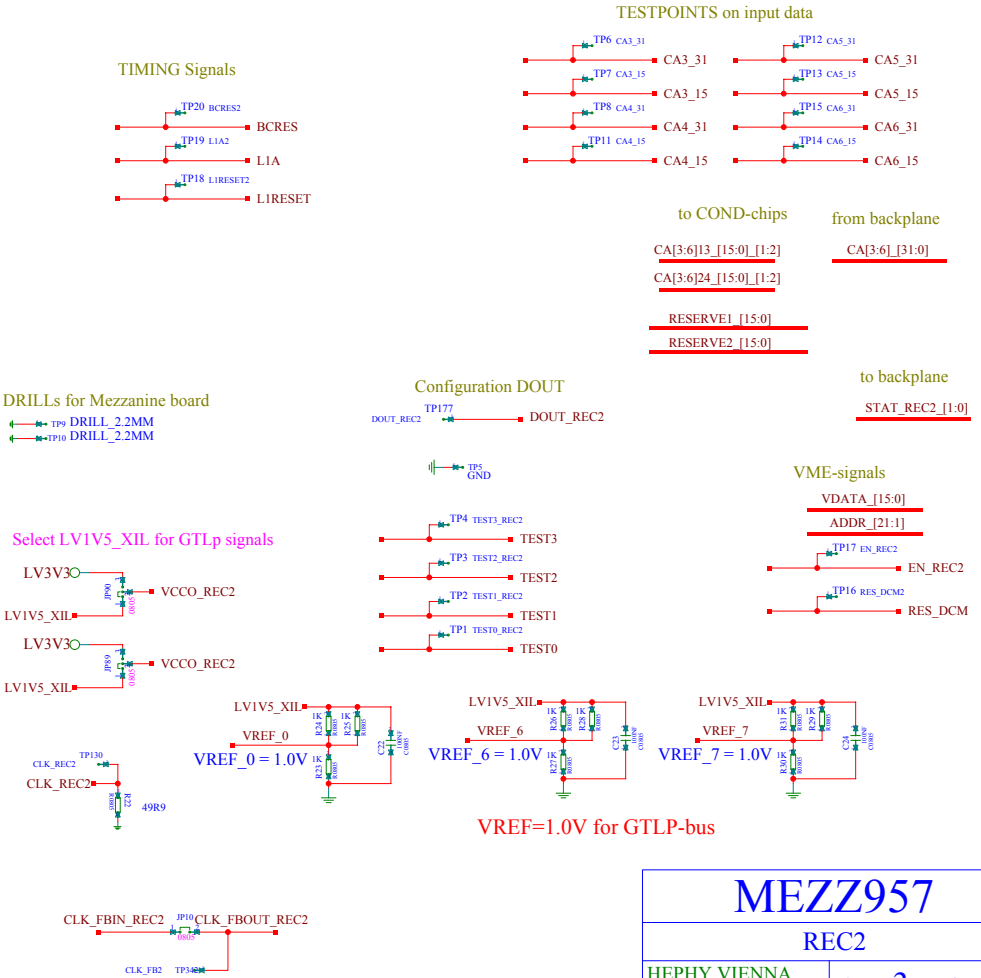




MEZZ957

REC2

HEPHY VIENNA ELEKTRONIK 1	sheet	2	of 3
modified by: HB		8-8-2005_11:08	
checked by: CHECKER		0-00-0000_00:00	

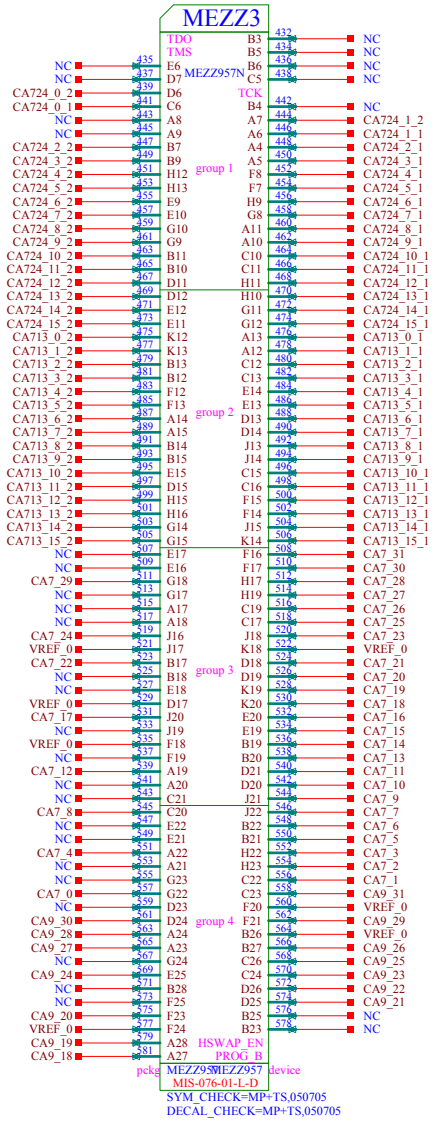


MEZZ957

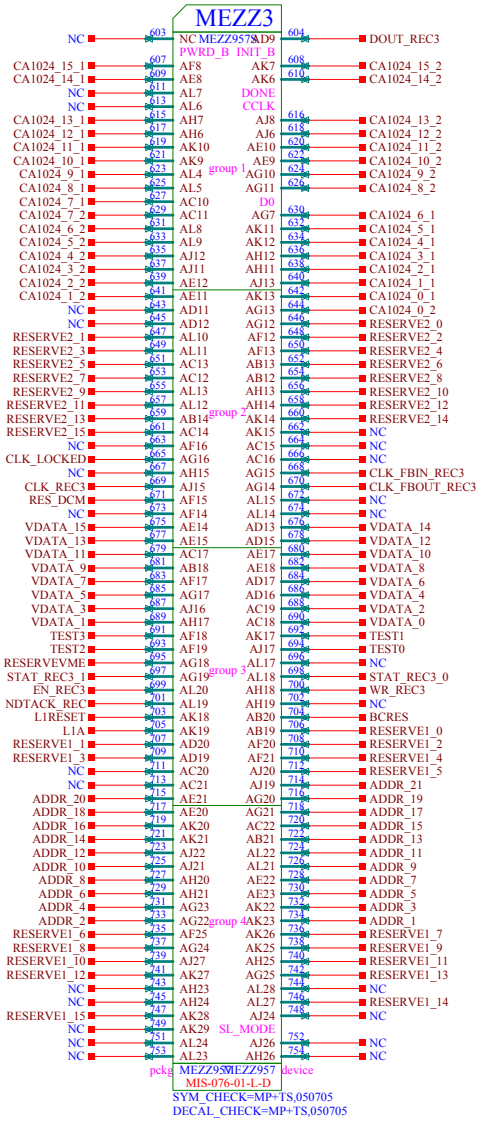
REC2

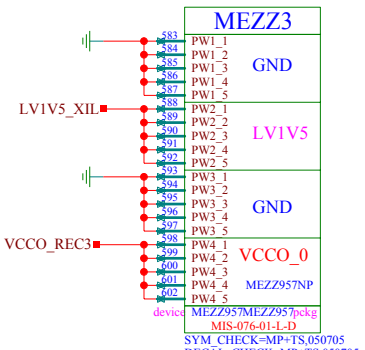
HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB	8-9-2005_17:22
checked by: CHECKER	0-00-0000_00:00

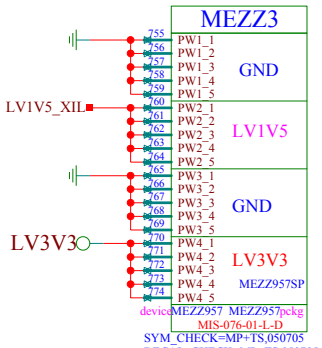
NORD MIS_076 connector



SOUTH MIS_076 connector







Receiver-chips

CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]

MEZZ957

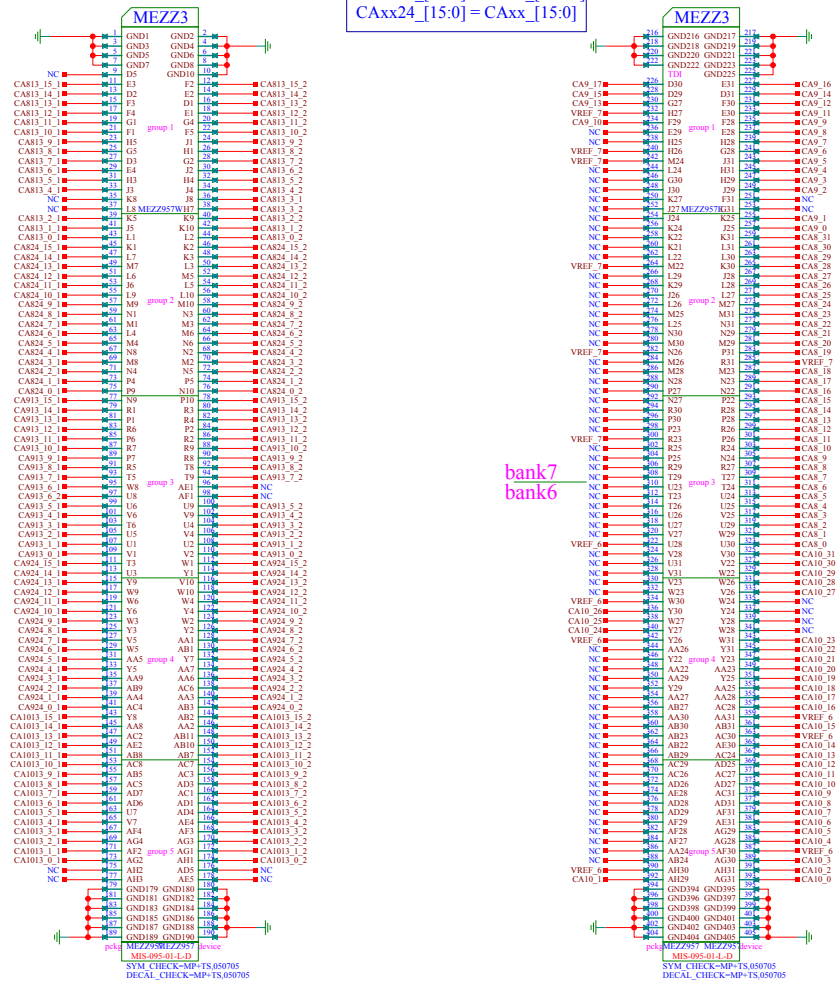
REC3

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3	
modified by: HB	8-8-2005 11:09	
checked by: CHECKER	0-00-0000 00:00	

WEST MIS_095 connector

Receiver-chips
CAxx13_[15:0] = CAxx_[31:16]
CAxx24_[15:0] = CAxx_[15:0]

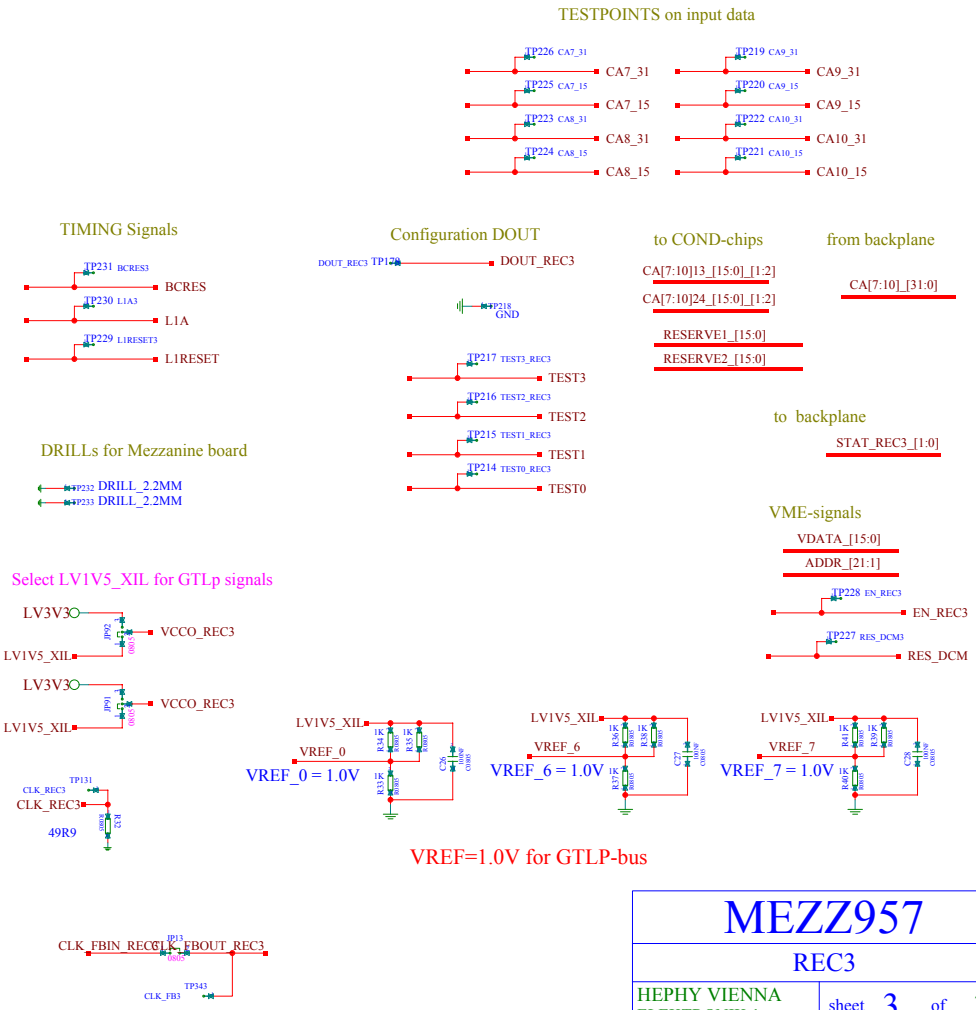
EAST MIS_095 connector



MEZZ957

REC3

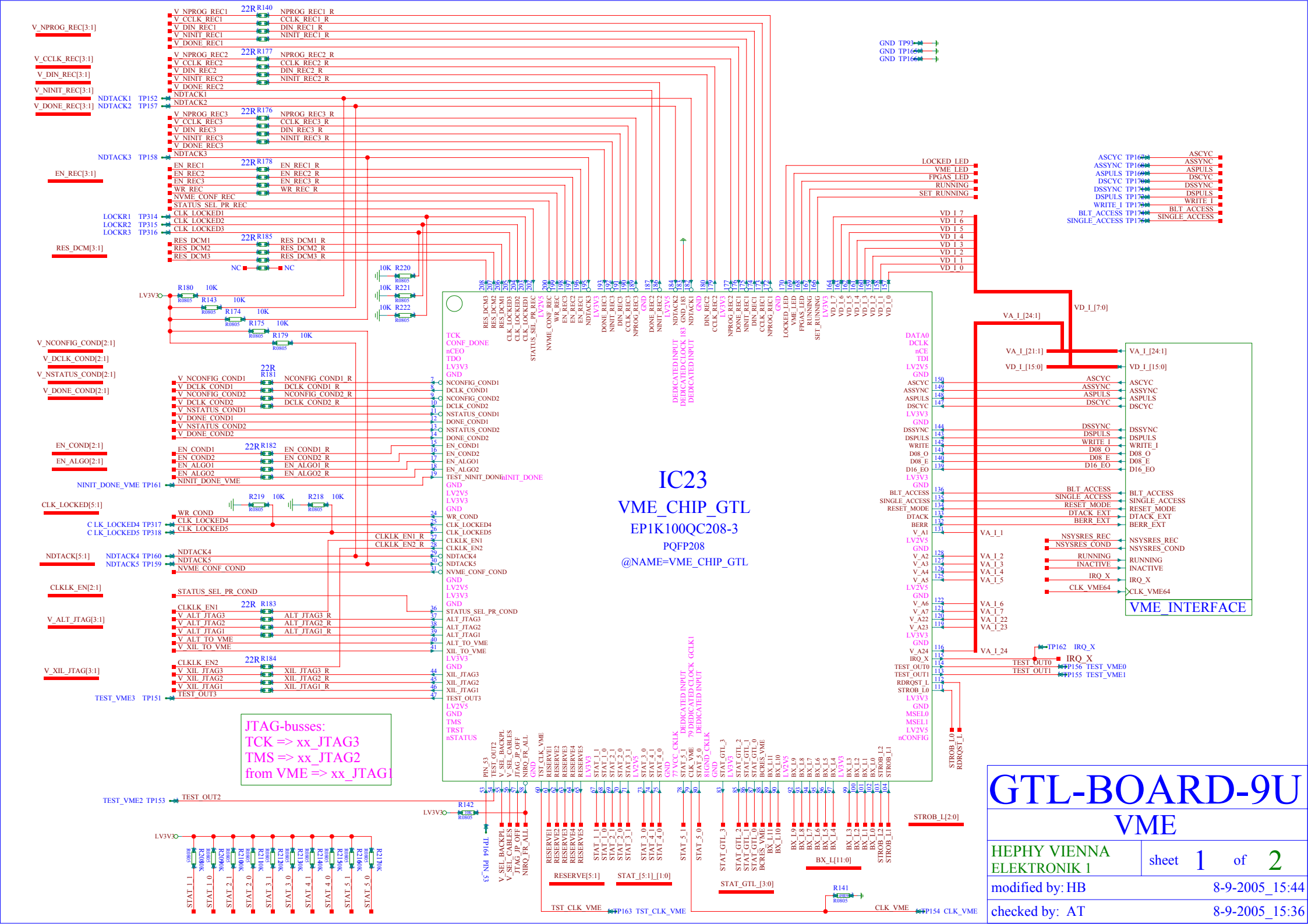
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB	8-8-2005_11:09
checked by: CHECKER	0-00-0000_00:00

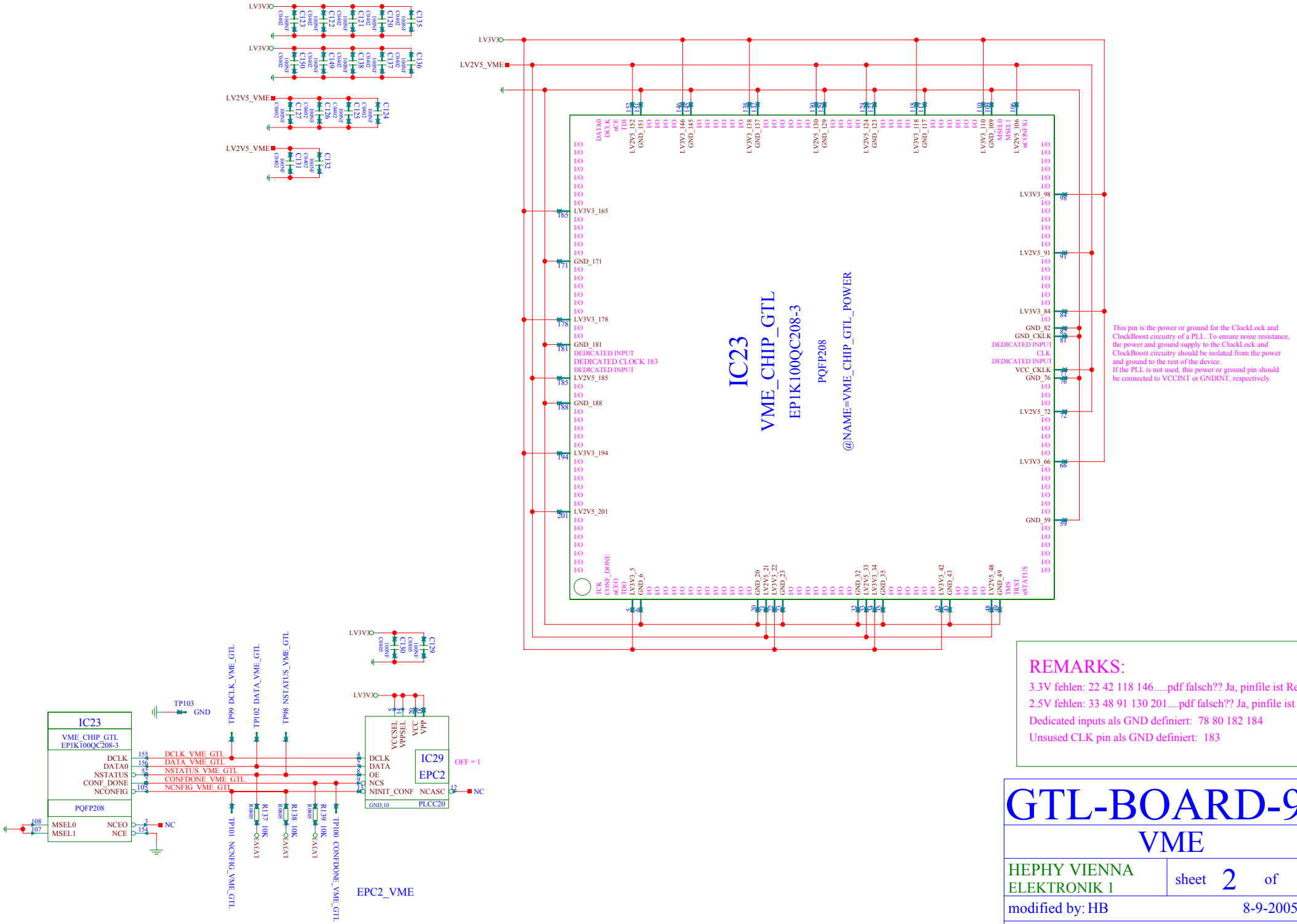


MEZZ957

REC3

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3	
modified by: HB		8-9-2005_17:25
checked by: AT		8-9-2005_17:22

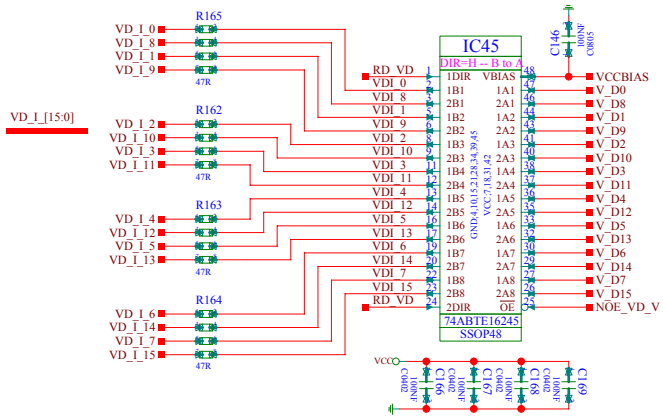

IC23
VME_CHIP_GTL
EP1K100QC208-3
PQFP208
@NAME=VME_CHIP_GTL
VME_INTERFACE
JTAG-busses:
TCK => xx_JTAG3
TMS => xx_JTAG2
from VME => xx_JTAG1
GTL-BOARD-9U
VME
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 2
modified by: HB 8-9-2005_15:44
checked by: AT 8-9-2005_15:36

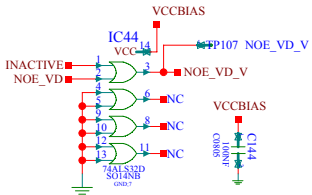

IC23
VME_CHIP_GTL
EP1K100QC208-3
PQFP208
@NAME=VME_CHIP_GTL_POWER
LV3V3
LV2V5_VME
This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
IC23
VME_CHIP_GTL
EP1K100QC208-3
PQFP208
DCLK_VME_GTL
DATA_VME_GTL
NSTATUS_VME_GTL
CONFDONE_VME_GTL
NCNFIG_VME_GTL
IC29
EPC2
PLCC20
OFF = 1
EPC2_VME
REMARKS:
3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Referenz, H
2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Referenz,
Dedicated inputs als GND definiert: 78 80 182 184
Unsused CLK pin als GND definiert: 183
GTL-BOARD-9U
VME
HEPHY VIENNA
ELEKTRONIK 1
sheet 2 of 2
modified by: HB 8-9-2005_15:49
checked by: AT 8-9-2005_15:36

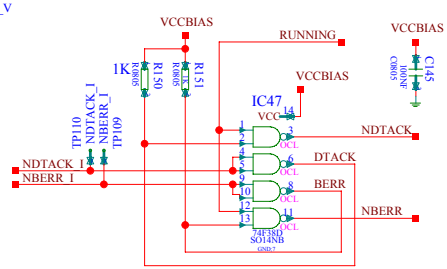
47 Ohm resistors protect the Virtex drivers against overvoltage spikes.

GTL9U must not be inserted into the 6U Backplane!!!

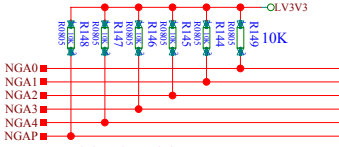
D1 = VCC on BACK6U
D1 = LV3V3bias on BACK9U







Keep NDTACK NBERR inactive while VME64X chip is unconfigured



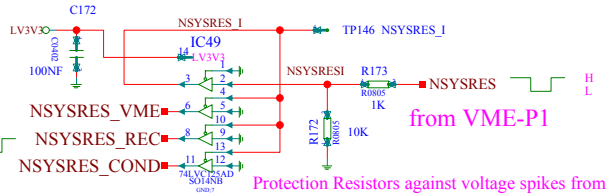
inverted values

Geographical Addresses

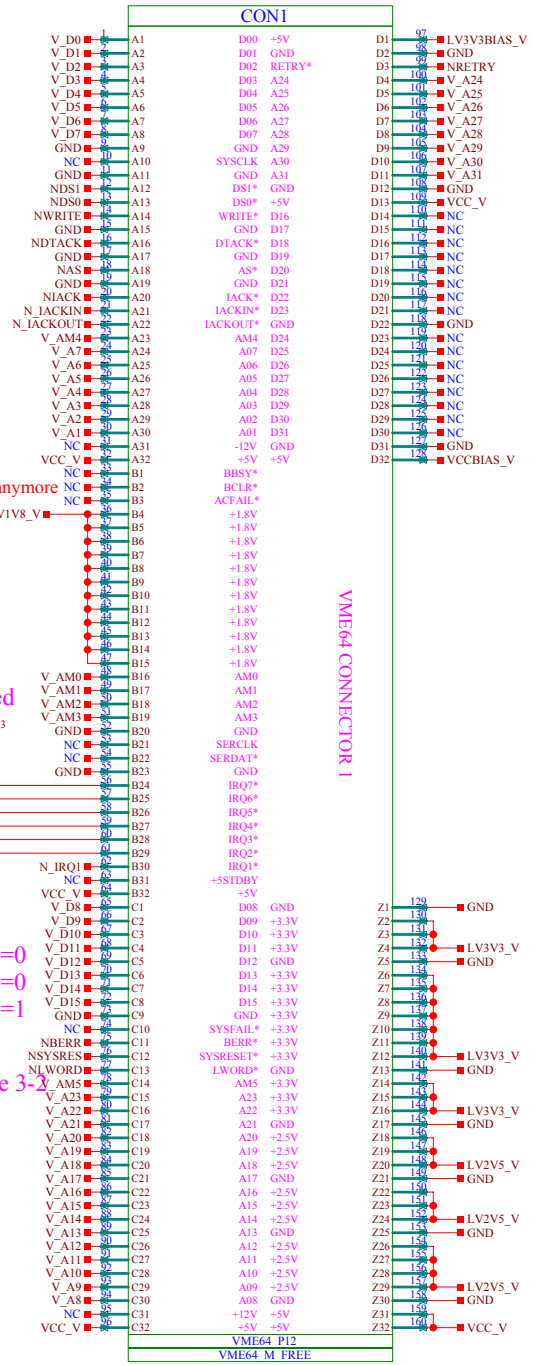
Parity bit: for odd parity

slot=1: GA=0 0001 => GAP=0
slot=2: GA=0 0010 => GAP=0
slot=3: GA=0 0011 => GAP=1
etc

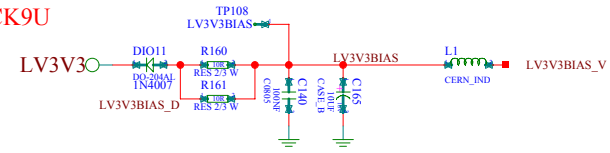
See VME64x.pdf page 10 Table 3-2

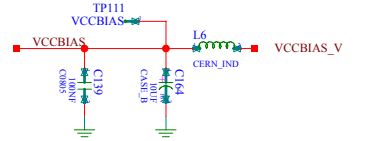


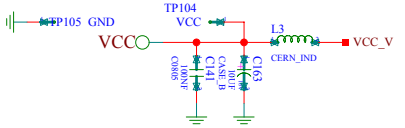
Protection Resistors against voltage spikes from backplane.

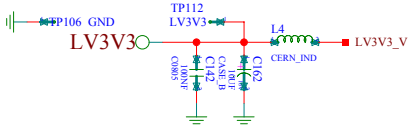


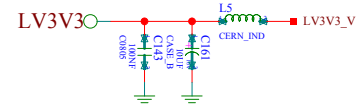
LV2V5_V not used anymore



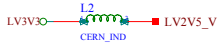


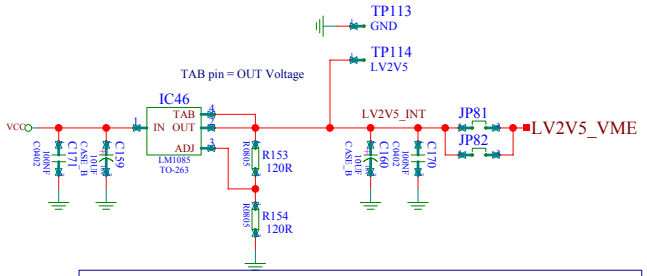






Unused 2.5V plane can be connected to 3.3V optionally on 9U backplane if GTL-6U is not used anymore in Crate
Do not solder this part.



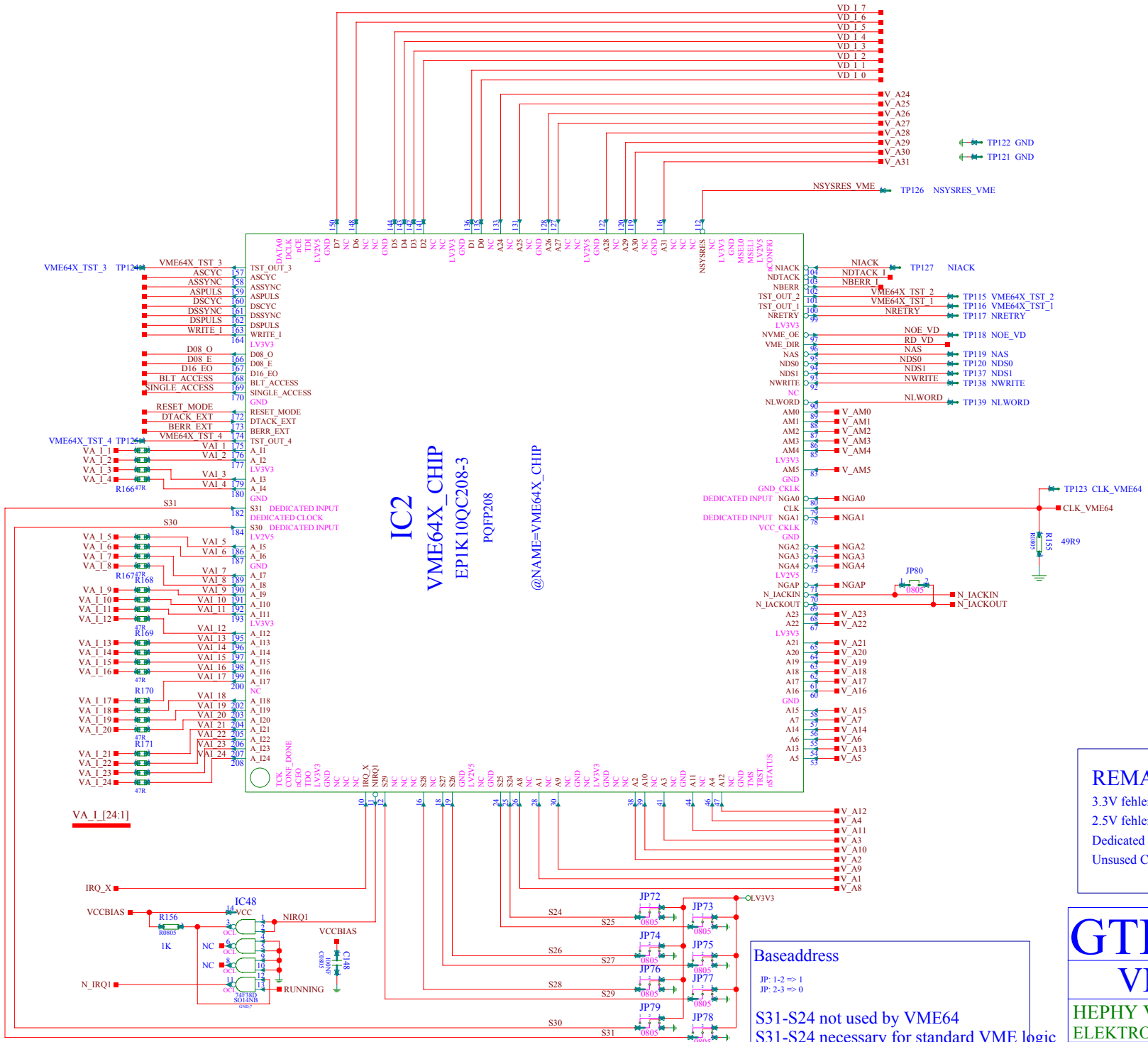


Do not use LV2V5 and LV1V8 from BACKPLANE-6U
LV2V5 and LV1V8 will not be connected on the Backplane-9U

GTL-BOARD-9U

VME_INTERFACE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3	
modified by: HB		8-9-2005_16:25
checked by: AT		8-9-2005_15:56



REMARKS:

3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Referenz, HB

2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Referenz, H

Dedicated inputs als GND definiert: 78 80 182 184

Unused CLK pin als GND definiert: 183

Baseaddress

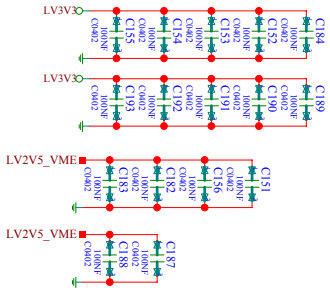
JP: 1-2 => 1
JP: 2-3 => 0

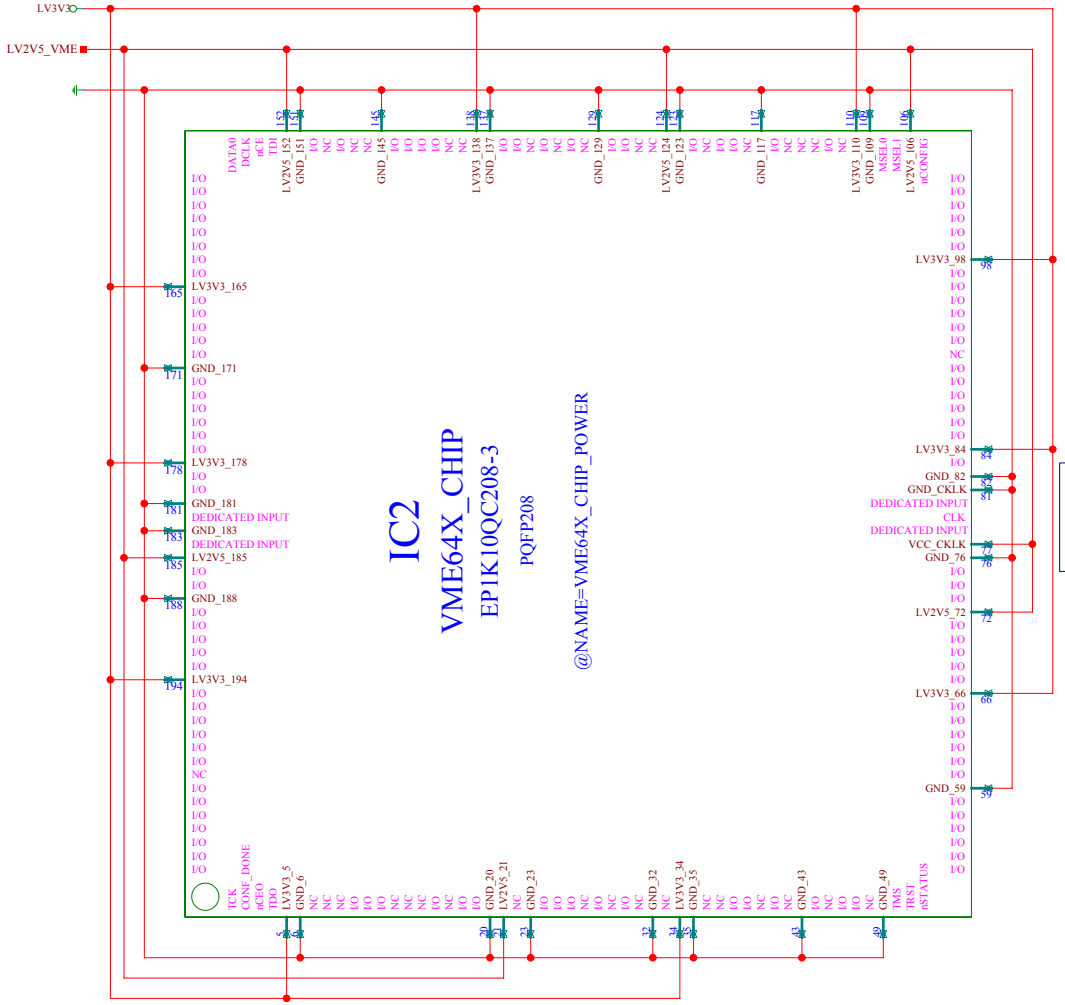
S31-S24 not used by VME64
S31-S24 necessary for standard VME logic

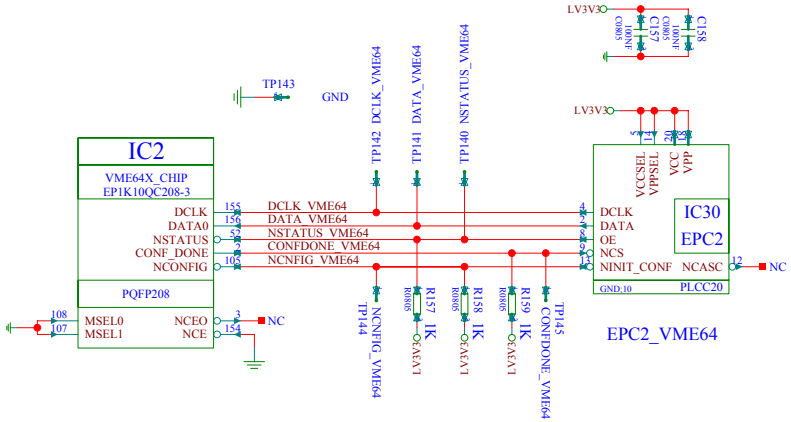
GTL-BOARD-9U

VME_INTERFACE

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: HB	8-9-2005_16:26
checked by: AT	8-9-2005_16:25







REMARKS:

3.3V pins 22 42 118 146 are missing on EP1K10. See pinfile as reference, HB 200803
2.5V pins 33 48 91 130 201 are missing on EP1K10. See pinfile as reference, HB 200803
Unsused CLK pin 183 is defined as GND.

GTL-BOARD-9U

VME_INTERFACE

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: HB	8-9-2005_16:36
checked by: AT	8-9-2005_16:35