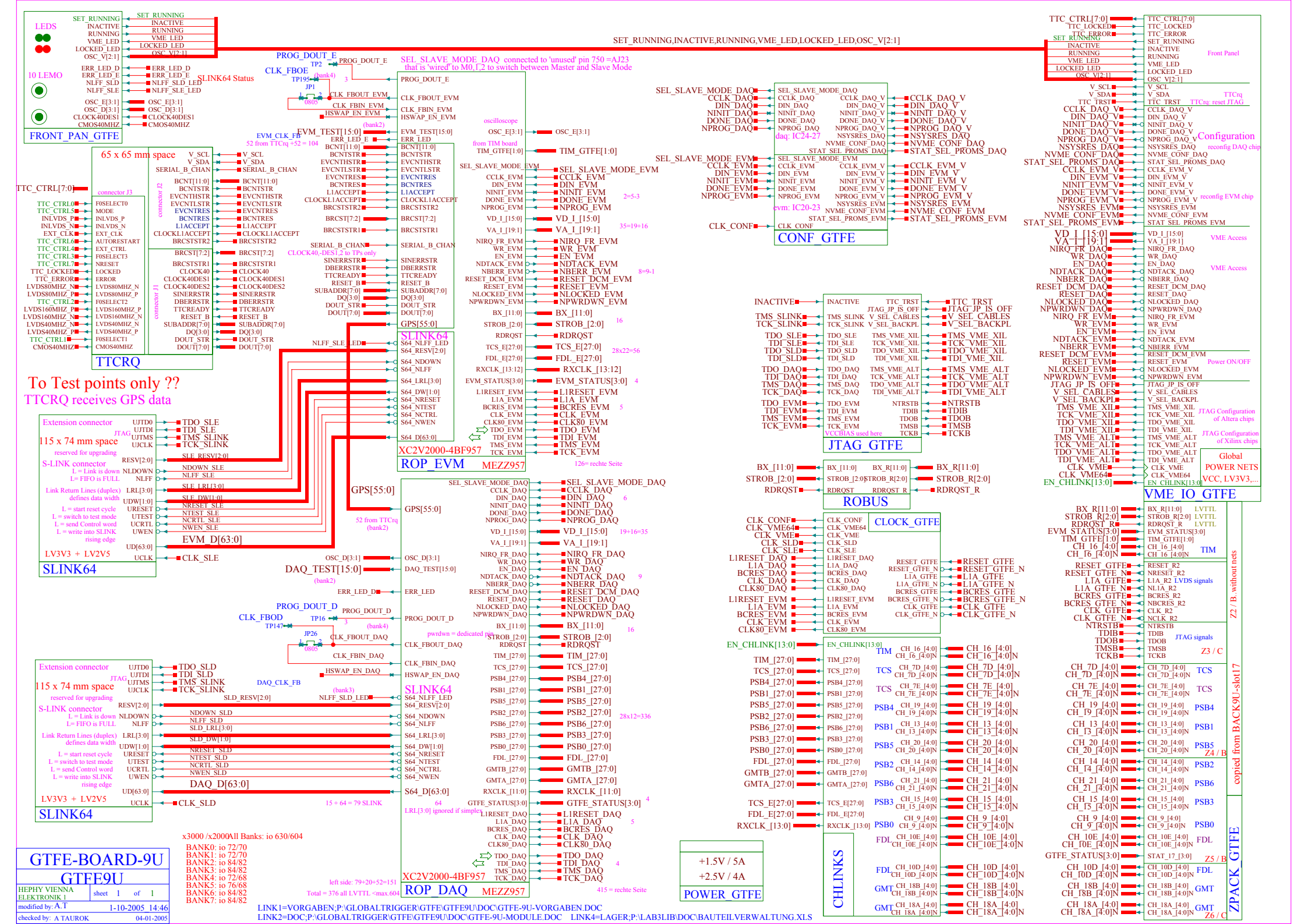
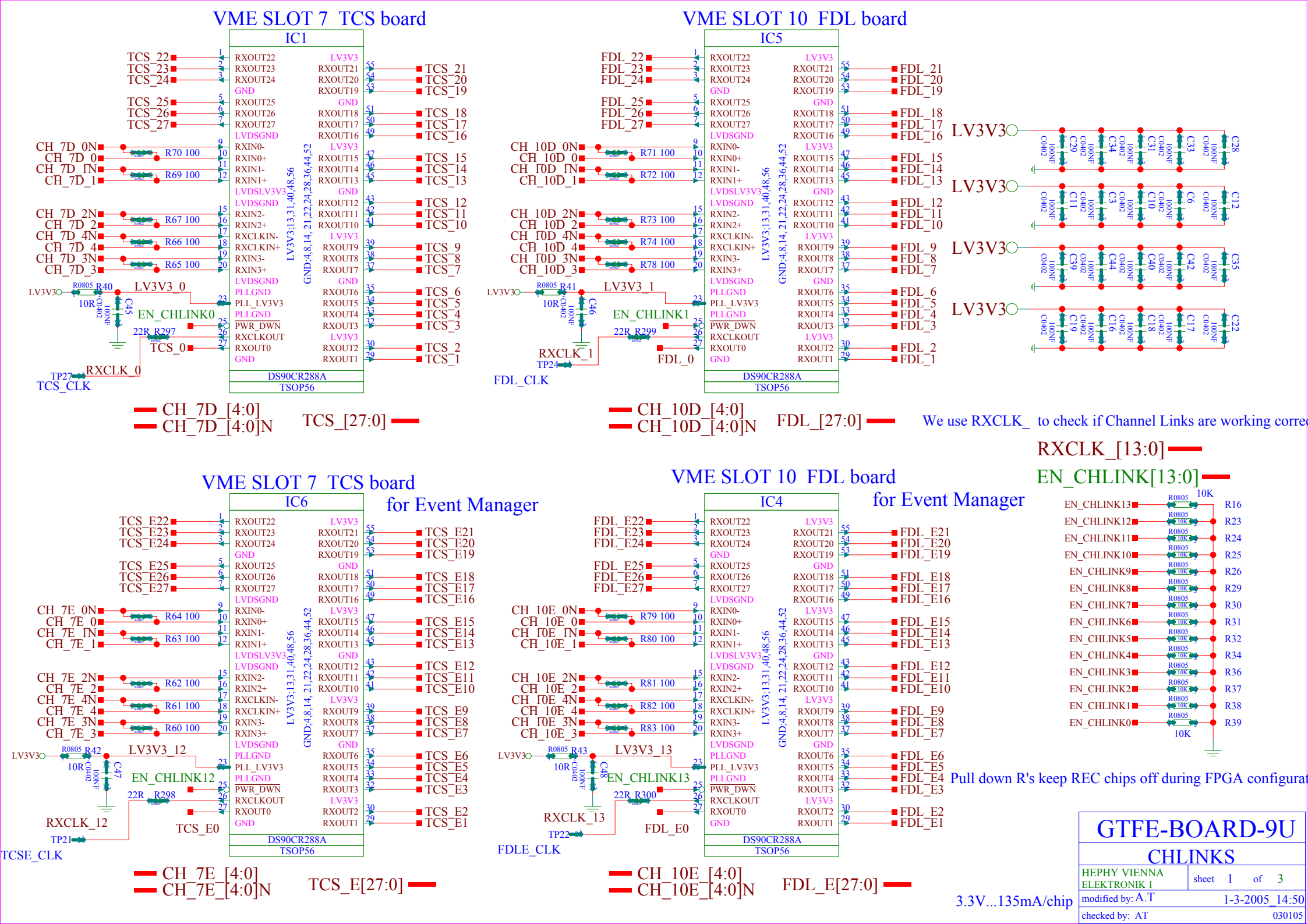
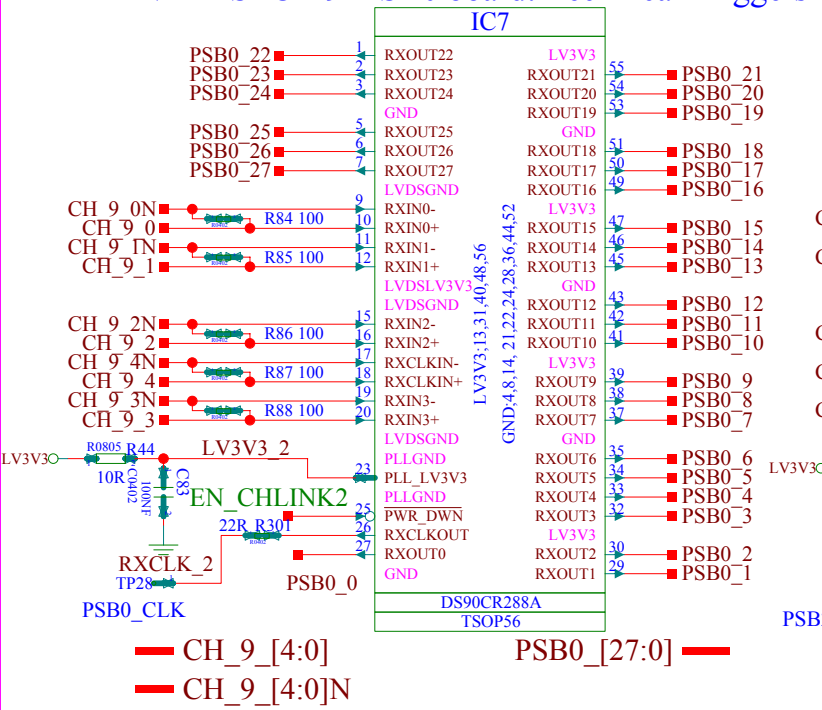
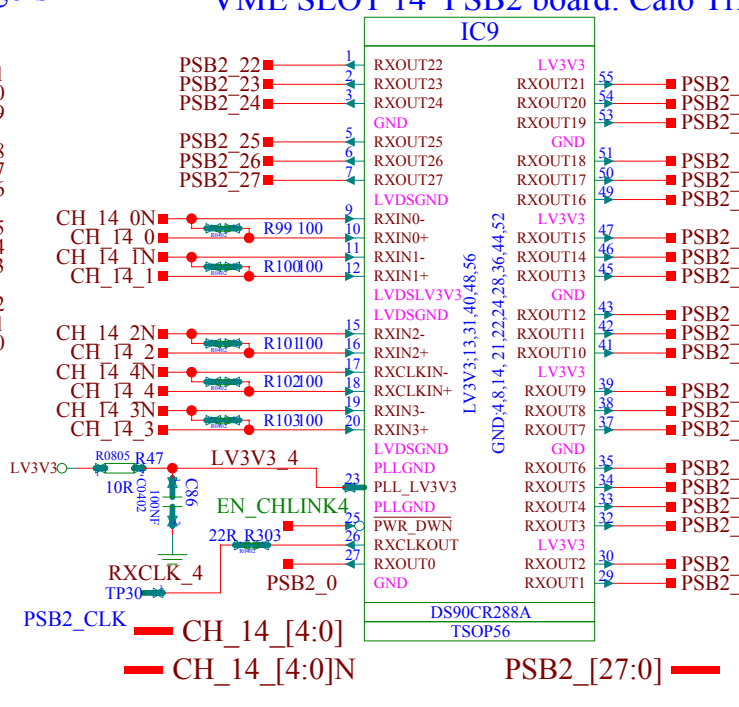

SET_RUNNING,INACTIVE,RUNNING,VME_LED,LOCKED_LED,OSC_V[2:1]
LEDS
10 LEMO
FRONT_PAN_GTFE
SLINK64 Status
PROG_DOUT_E
CLK_FBOE
EVM_CLK_FB
52 from TTCrq +52 = 104
EVM_TEST[15:0]
65 x 65 mm space
connector J3
connector J2
connector J1
TTCRQ
SEL_SLAVE_MODE_DAQ connected to 'unused' pin 750 =AJ23
that is 'wired' to M0,1,2 to switch between Master and Slave Mode
oscilloscope
from TIM board
SEL_SLAVE_MODE_EVM
2=5-3
35=19+16
8=9-1
CLOCK40,-DES1,2 to TPs only
SLINK64
XC2V2000-4BF957
ROP_EVM
MEZZ957
126= rechte Seite
28x22=56
16
4
5
CONF_GTFE
daq: IC24-27
evm: IC20-23
JTAG_GTFE
ROBUS
CLOCK_GTFE
VME_IO_GTFE
Front Panel
TTCrq
TTCrq: reset JTAG
Configuration
reconfig DAQ chip
reconfig EVM chip
VME Access
Power ON/OFF
JTAG Configuration of Altera chips
JTAG Configuration of Xilinx chips
Global POWER NETS
VCC, LV3V3,...
To Test points only ??
TTCRQ receives GPS data
Extension connector
115 x 74 mm space
reserved for upgrading
S-LINK connector
L = Link is down
L= FIFO is FULL
Link Return Lines (duplex) defines data width
L = start reset cycle
L = switch to test mode
L = send Control word
L = write into SLINK rising edge
LV3V3 + LV2V5
EVM_D[63:0]
GPS[55:0]
52 from TTCrq (bank2)
DAQ_TEST[15:0]
PROG_DOUT_D
CLK_FBOD
DAQ_CLK_FB
DAQ_D[63:0]
15 + 64 = 79 SLINK
64
LRL[3:0] ignored if simplex
left side: 79+20+52=151
Total = 376 all LVTTL <max.604
415 = rechte Seite
x3000 /x2000All Banks: io 630/604
BANK0: io 72/70
BANK1: io 72/70
BANK2: io 84/82
BANK3: io 84/82
BANK4: io 72/68
BANK5: to 76/68
BANK6: to 84/82
BANK7: to 84/82
+1.5V / 5A
+2.5V / 4A
POWER_GTFE
CHLINKS
ZPACK_GTFE
copied from BACK9U-slot17
Z2 / B. without nets
Z3 / C
Z4 / B
Z5 / B
Z6 / C
GTFE-BOARD-9U
GTFE9U
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by: A.T
1-10-2005 14:46
checked by: A TAUROK
04-01-2005
LINK1=VORGABEN;P:\GLOBALTRIGGER\GTFE\GTFE9U\DOC\GTFE-9U-VORGABEN.DOC
LINK2=DOC;P:\GLOBALTRIGGER\GTFE\GTFE9U\DOC\GTFE-9U-MODULE.DOC
LINK4=LAGER;P:\LAB3LIB\DOC\BAUTEILVERWALTUNG.XLS


VME SLOT 7 TCS board
IC1
DS90CR288A
TSOP56
CH_7D_[4:0]
CH_7D_[4:0]N
TCS_[27:0]
VME SLOT 10 FDL board
IC5
DS90CR288A
TSOP56
CH_10D_[4:0]
CH_10D_[4:0]N
FDL_[27:0]
We use RXCLK_ to check if Channel Links are working corre
RXCLK_[13:0]
EN_CHLINK[13:0]
VME SLOT 7 TCS board
for Event Manager
IC6
DS90CR288A
TSOP56
CH_7E_[4:0]
CH_7E_[4:0]N
TCS_E[27:0]
VME SLOT 10 FDL board
for Event Manager
IC4
DS90CR288A
TSOP56
CH_10E_[4:0]
CH_10E_[4:0]N
FDL_E[27:0]
Pull down R's keep REC chips off during FPGA configurat
3.3V...135mA/chip
GTFE-BOARD-9U
CHLINKS
HEPHY VIENNA ELEKTRONIK 1
sheet 1 of 3
modified by: A.T
1-3-2005_14:50
checked by: AT
030105

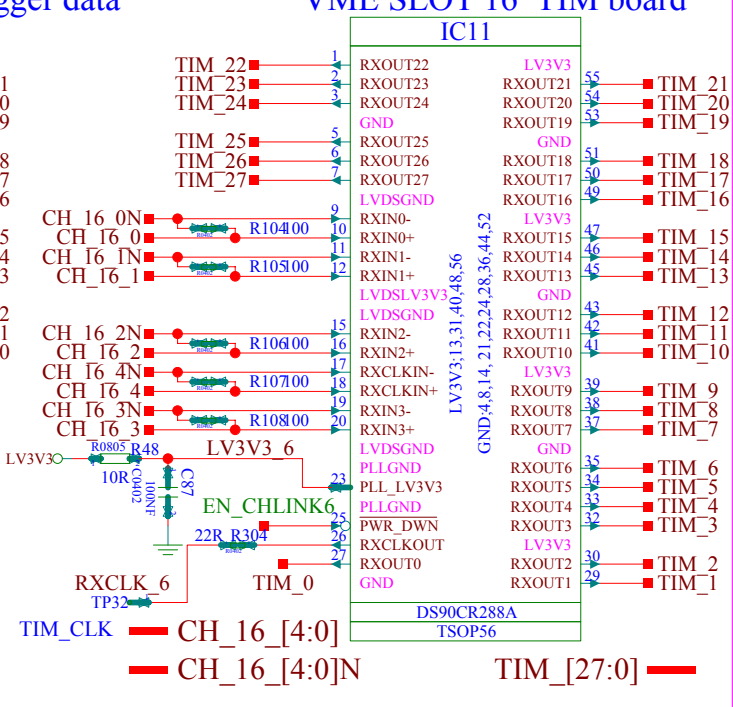
VME SLOT 9 PSB0 board: Technical Triggers



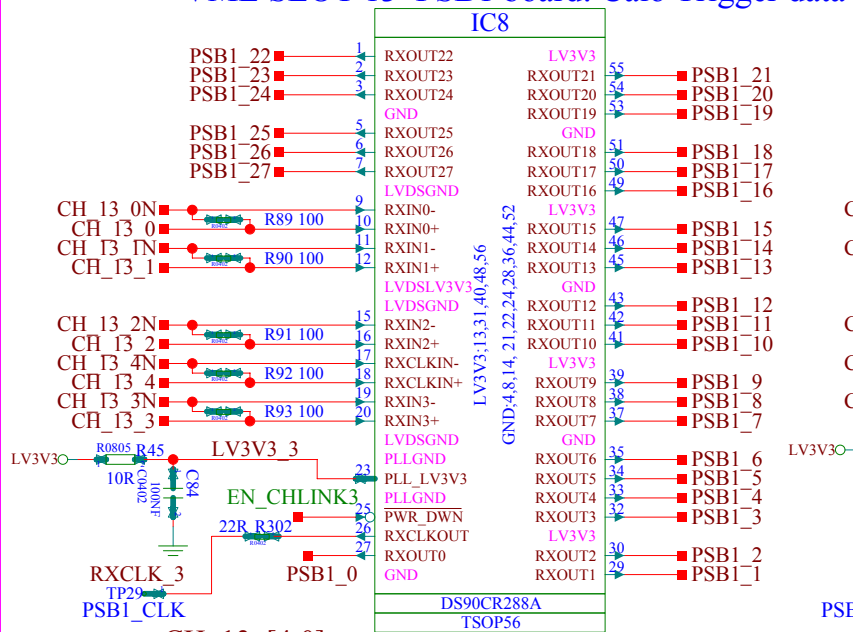
VME SLOT 14 PSB2 board: Calo Trigger data



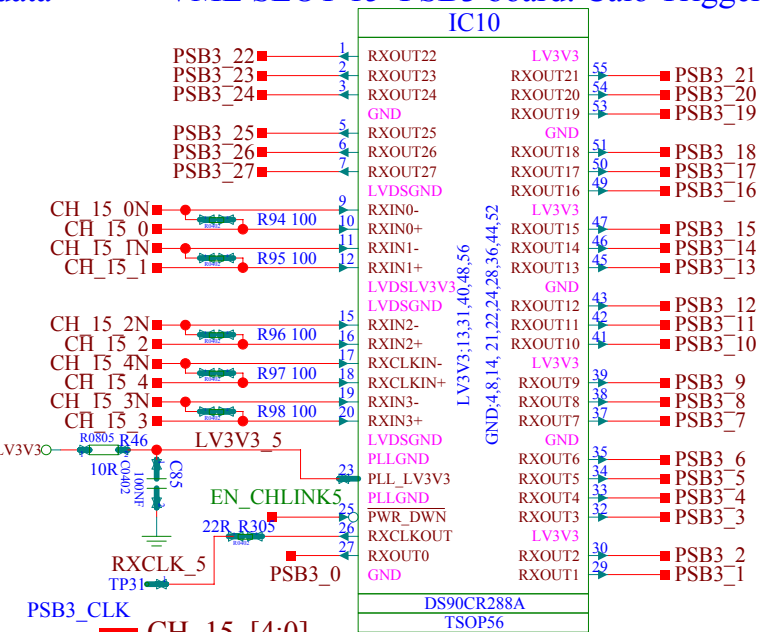
VME SLOT 16 TIM board

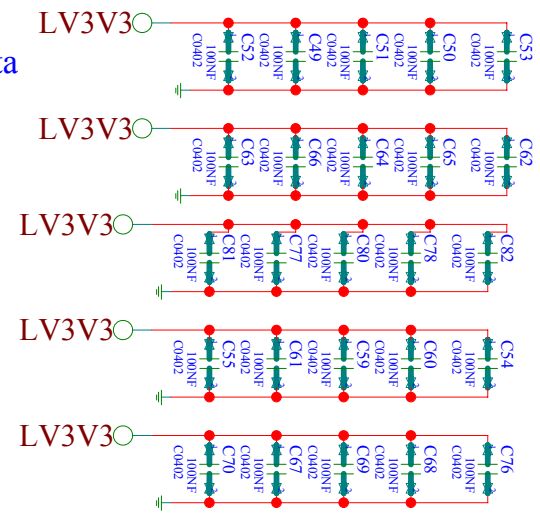


VME SLOT 13 PSB1 board: Calo Trigger data



VME SLOT 15 PSB3 board: Calo Trigger data



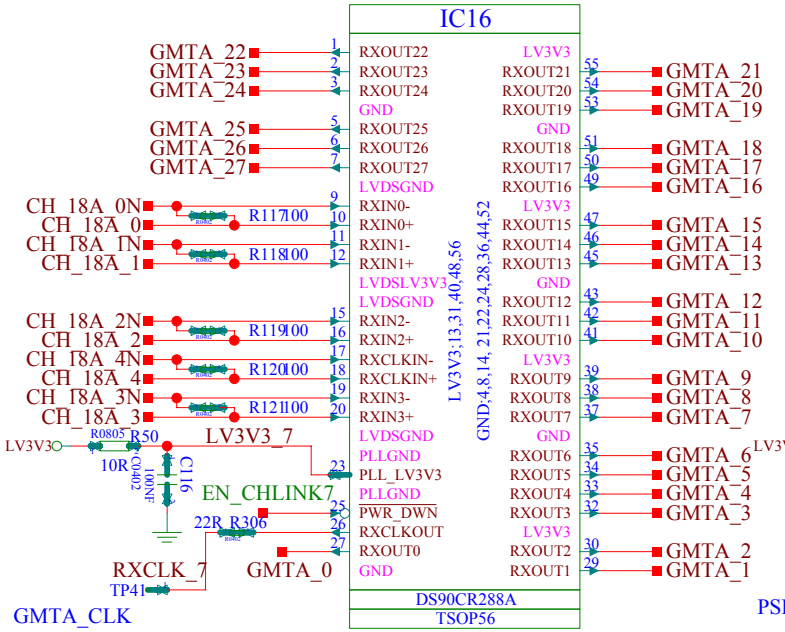


GTFE-BOARD-9U

CHLINKS

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: A.T	1-3-2005_14:54
checked by: AT	030105

VME SLOT 18 GMTA board: Global Muon Trigger

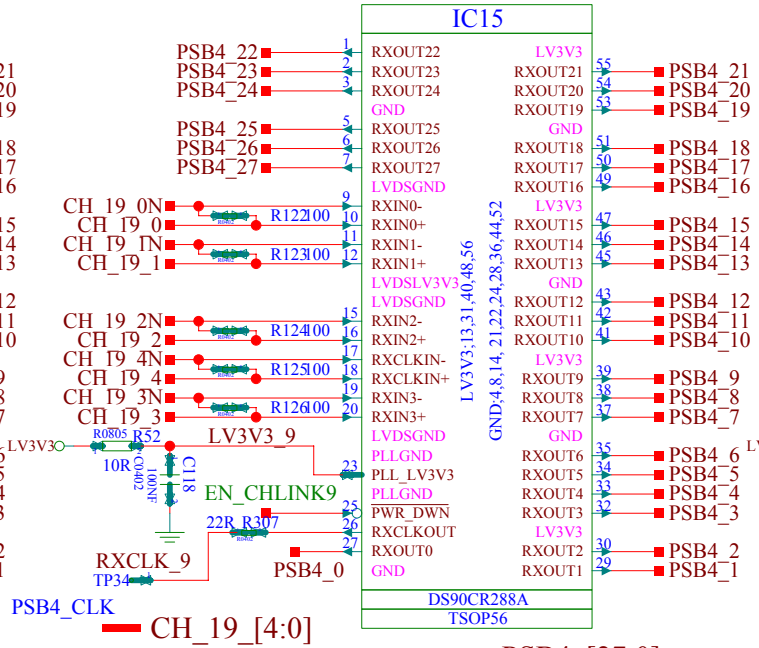


CH_18A_[4:0]

CH_18A_[4:0]N

GMTA_[27:0]

VME SLOT 19 PSB4 board: mip/quiet bits

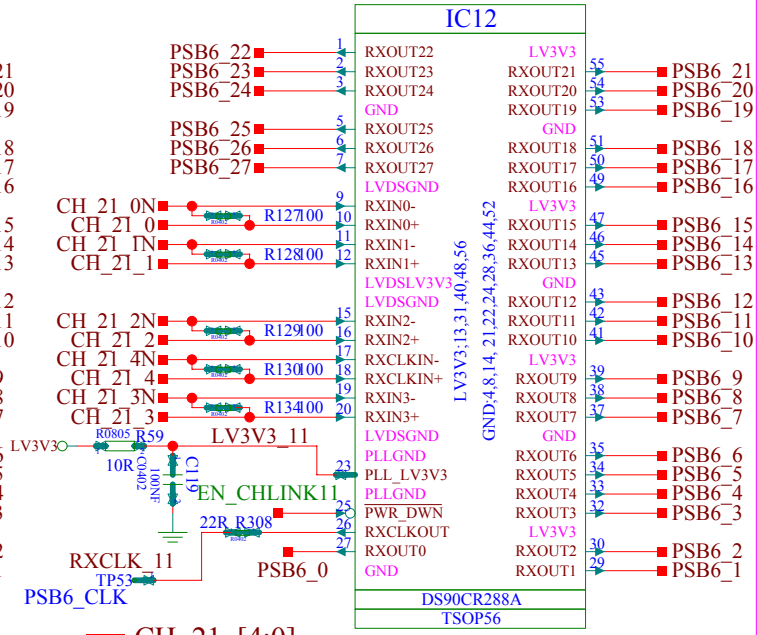


CH_19_[4:0]

CH_19_[4:0]N

PSB4_[27:0]

VME SLOT 21 PSB6 board: mip/quiet bits

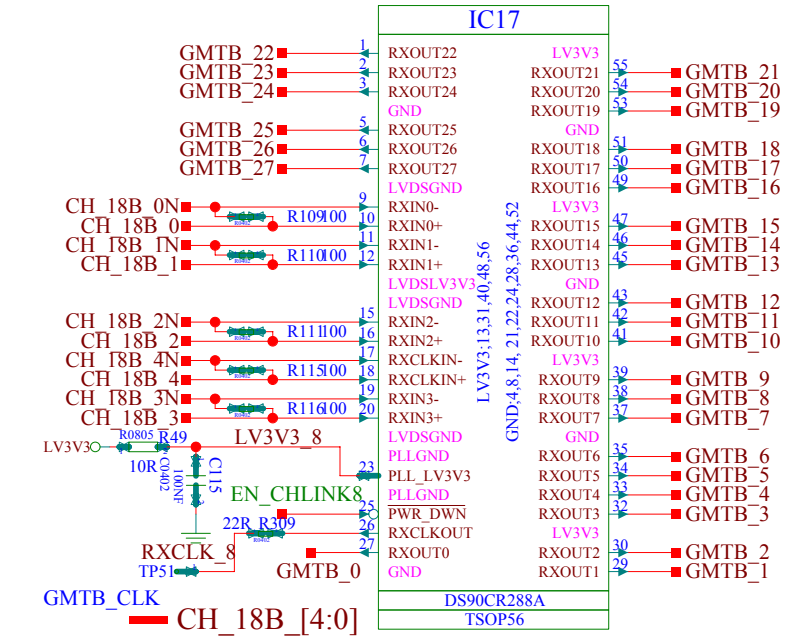


CH_21_[4:0]

CH_21_[4:0]N

PSB6_[27:0]

VME SLOT 18 GMTB board: Global Muon Trigger

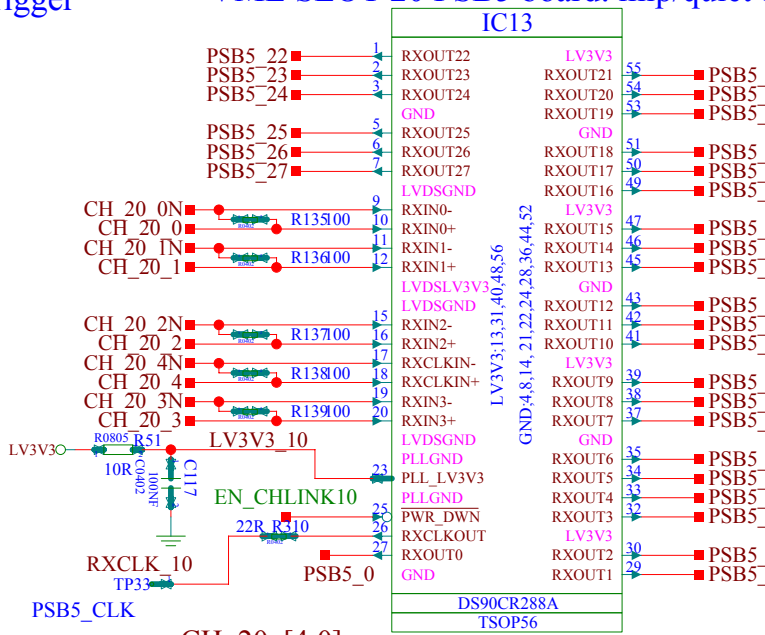


CH_18B_[4:0]

CH_18B_[4:0]N

GMTB_[27:0]

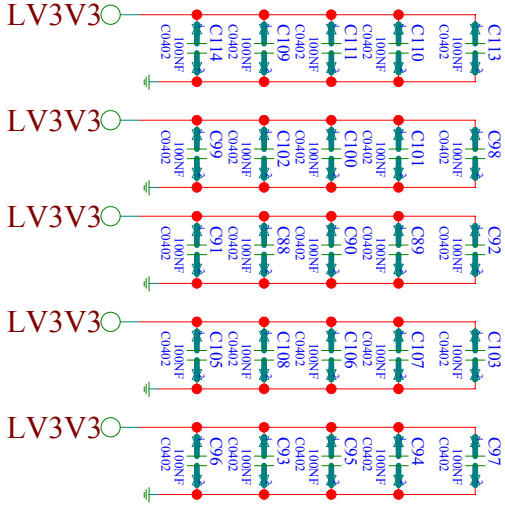
VME SLOT 20 PSB5 board: mip/quiet bits



CH_20_[4:0]

CH_20_[4:0]N

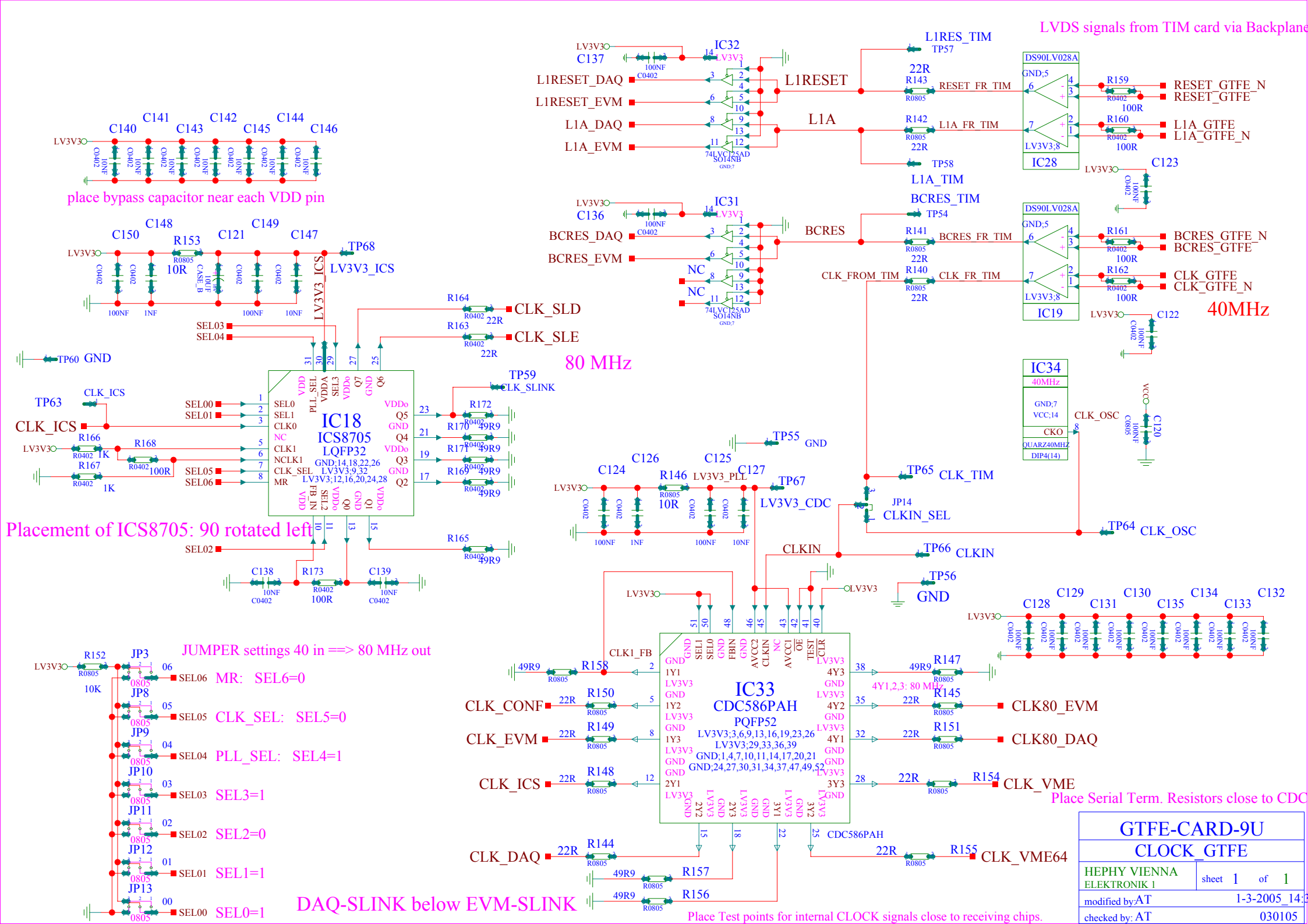
PSB5_[27:0]

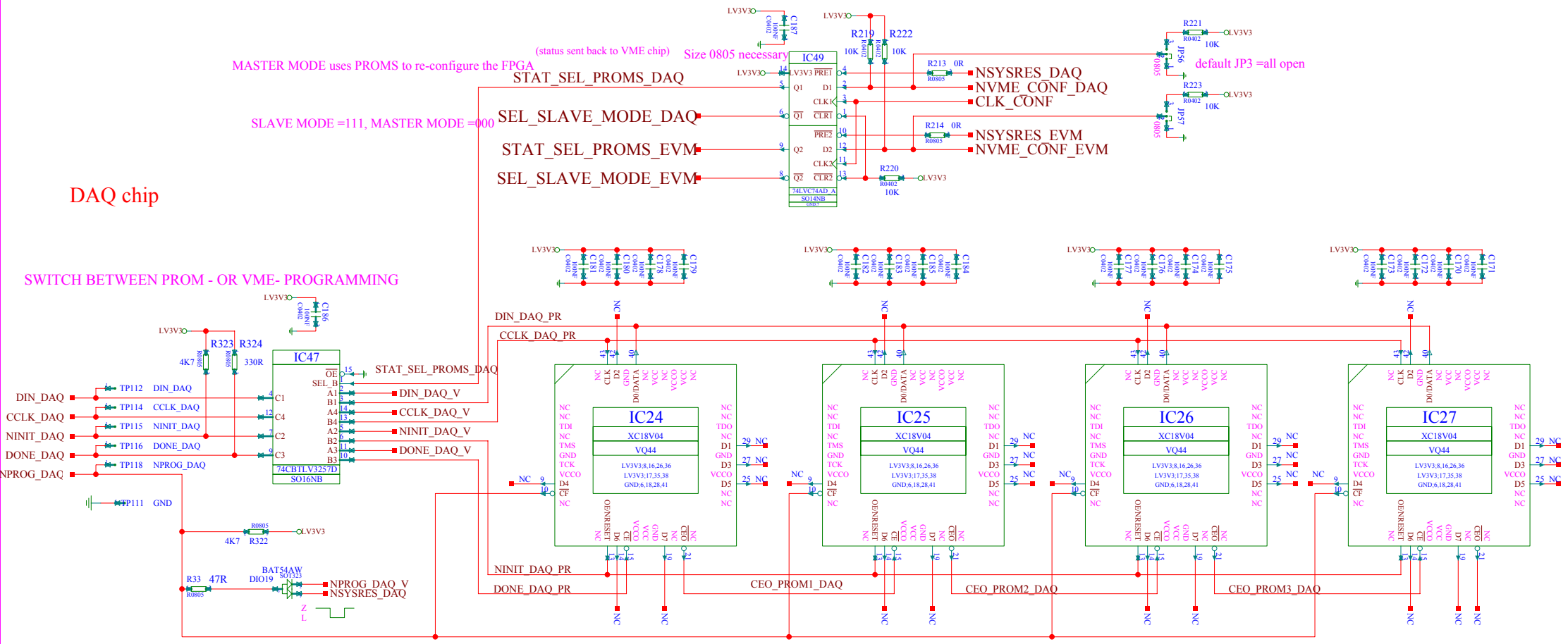


GTFE-BOARD-9U

CHLINKS

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: A.T	1-3-2005_14:56
checked by: AT	03-01-05


LVDS signals from TIM card via Backplane
place bypass capacitor near each VDD pin
80 MHz
40MHz
Placement of ICS8705: 90 rotated left
JUMPER settings 40 in ==> 80 MHz out
MR: SEL6=0
CLK_SEL: SEL5=0
PLL_SEL: SEL4=1
SEL3=1
SEL2=0
SEL1=1
SEL0=1
DAQ-SLINK below EVM-SLINK
4Y1,2,3: 80 MHz
Place Serial Term. Resistors close to CDC
Place Test points for internal CLOCK signals close to receiving chips.
IC18
ICS8705
LQFP32
IC33
CDC586PAH
PQFP52
IC32
IC31
IC28
IC19
IC34
40MHz
DS90LV028A
74LVC125AD
SO14NB
QUARZ40MHZ
DIP4(14)
GTFE-CARD-9U
CLOCK_GTFE
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by:AT
1-3-2005_14:3
checked by: AT
030105



CLK: IN

/CF: OUT: OPEN DRAIN
/CF: Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.

OE/RESET: BIDIR and OPEN DRAIN
OE/RESET: When Low, this input holds the address counter reset and the DATA output is in a Low while the PROM is reset. Polarity is NOT programmable. high-impedance state. This is a bidirectional open-drain pin that is held

/CE: IN
/CE: When CE is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.

/CEO: OUT
/CEO Chip Enable Output (CEO) is connected to the CE input of the next PROM in the chain. This output is Low when CE is Low and OE/RESET input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. CEO returns to High when OE/RESET goes Low or CE goes High.

Important: REFDES in CONF_GTFE und JTAG schematics shall agree!!

While running NPROG_DAQ_V reconfigures FPGA from Proms. (FPGA=master mode)
While running JTAG can reconfigure FPGA with new Prom content (FPGA=master mode)

See DAQ_CHIP schematic to find:
HSWAP_EN_DAQ
NPWRDWN_B
DOUT_DAQ
On Mezzanine board for DAQ you find: M0,M1,M2

Selecting Configuration Modes
We use serial mode only.

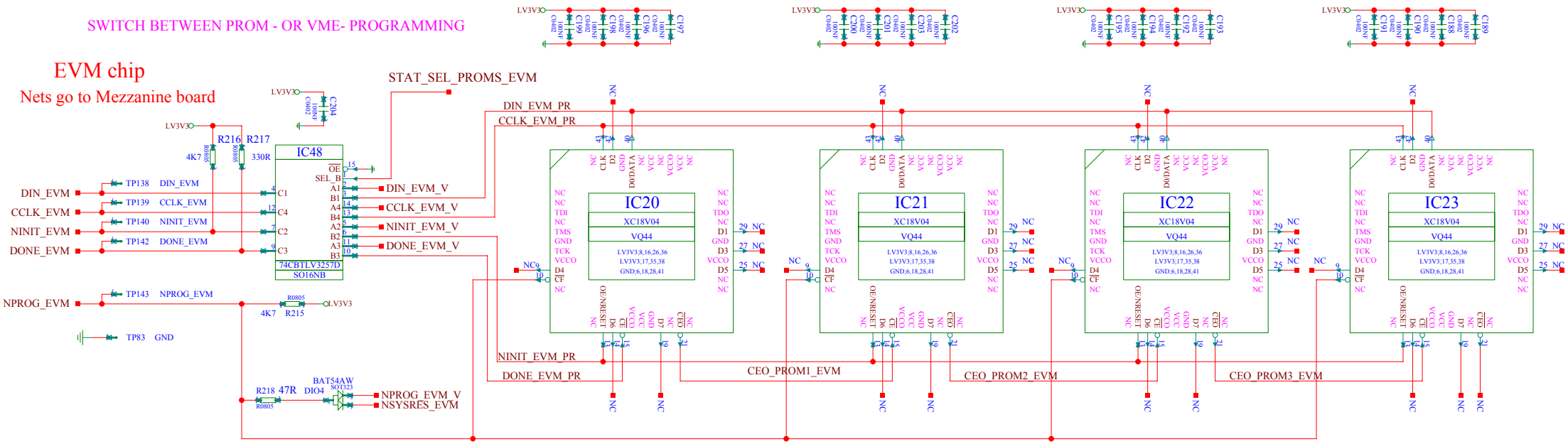
The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

JTAG pins of PROMs : See JTAG circuits

GTFE-CARD-9U

CONF_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 2
modified by: A.TAUROK	12-22-2004_15:13
checked by: HB	221204



CLK: IN

/CF: OUT: OPEN DRAIN
/CF: Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.

OE/RESET: BIDIR and OPEN DRAIN
OE/RESET: When Low, this input holds the address counter reset and the DATA output is in a Low while the PROM is reset. Polarity is NOT programmable.
high-impedance state. This is a bidirectional open-drain pin that is held

/CE: IN
/CE: When CE is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.

/CEO: OUT
/CEO Chip Enable Output (CEO) is connected to the CE input of the next PROM in the chain. This output is Low when CE is Low and OE/RESET input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. CEO returns to High when OE/RESET goes Low or CE goes High.

Important: REFDES in CONF_GTFE und JTAG schematics shall agree!!

While running NPROG_DAQ_V reconfigures FPGA from Proms. (FPGA=master mode)
While running JTAG can reconfigure FPGA with new Prom content (FPGA=master mode)

JTAG pins of PROMs : See JTAG circuits

See EVM_CHIP schematic to find:
HSWAP_EN_EVM
NPWRDWN_B
DOUT_EVM
On Mezzanine board for EVM you find: M0,M1,M2

Selecting Configuration Modes
We use serial mode only.

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

GTFE-CARD-9U

CONF_GTFE

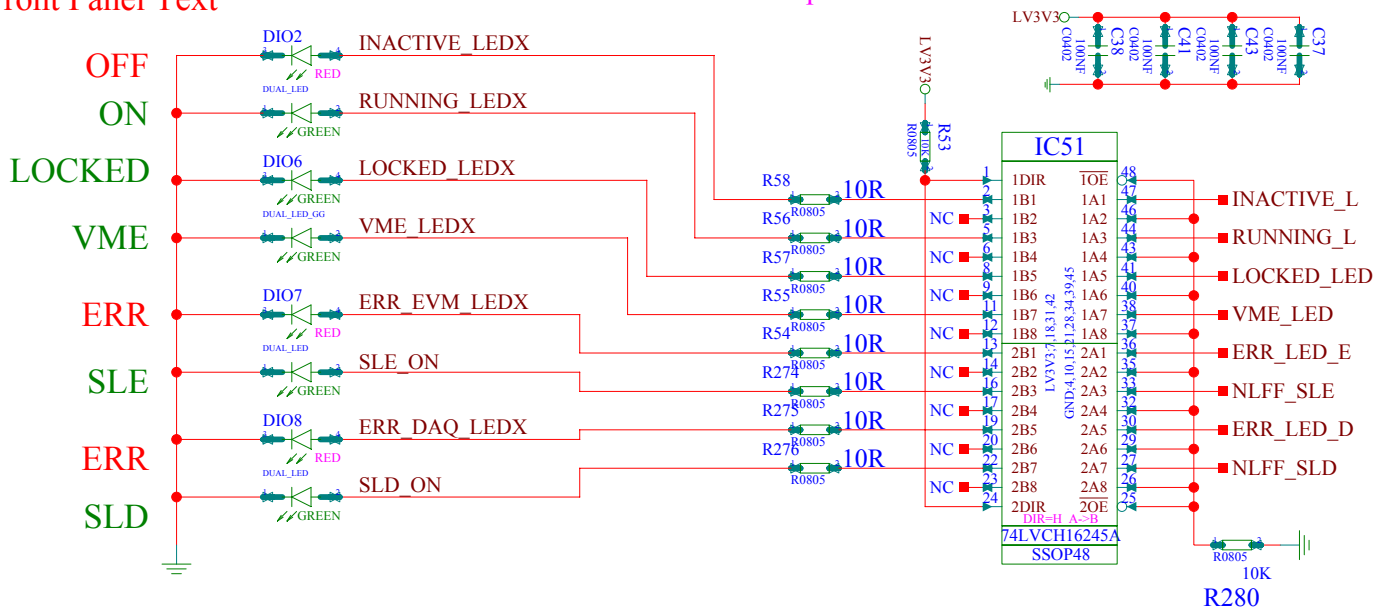
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 2
modified by: A.TAUROK	12-22-2004_15:13
checked by: HB	221204

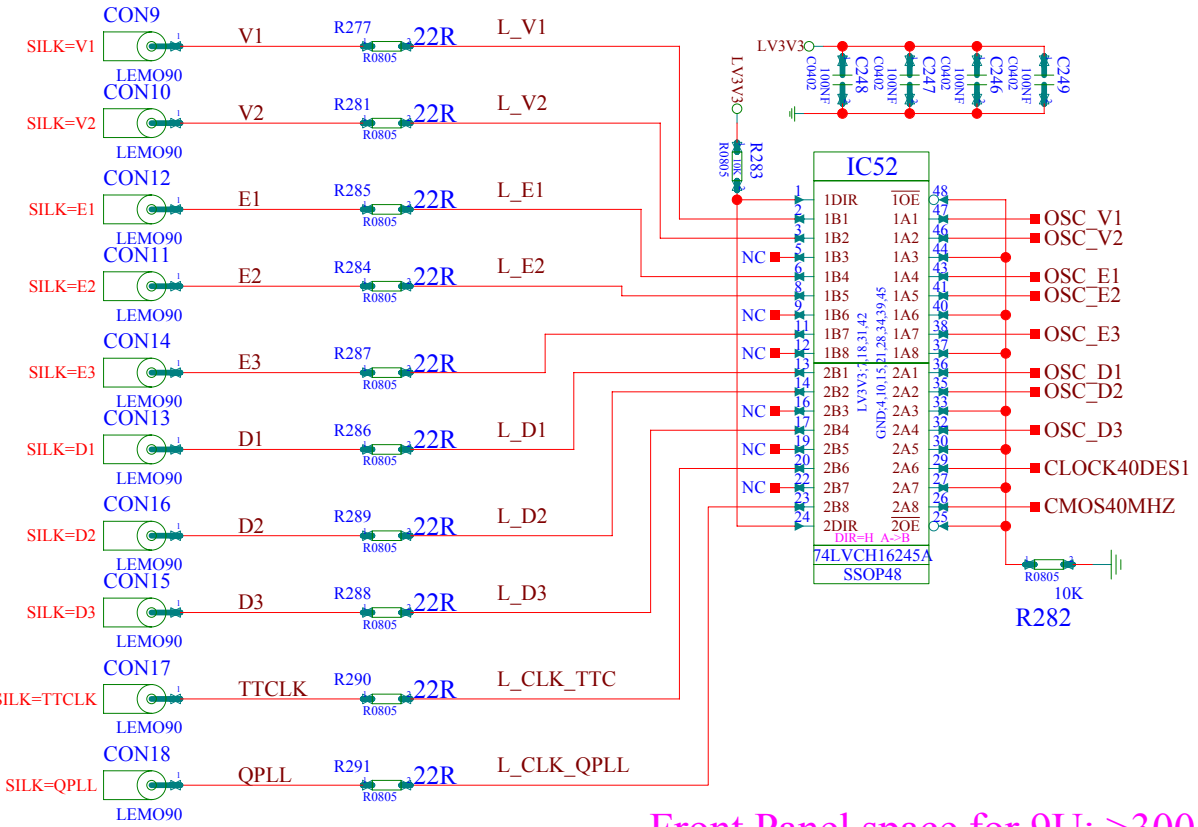
DISPLAY

leds mounted above all connectors on frontpanel

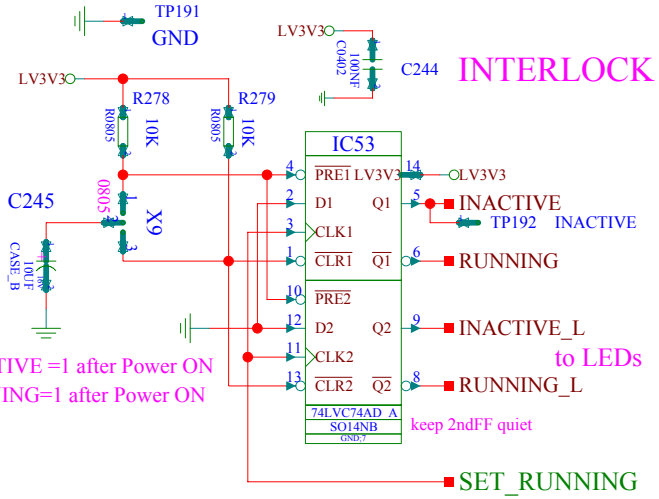
Front Panel Text

OFF
ON
LOCKED
VME
ERR
SLE
ERR
SLD





OSC_V[2:1]
OSC_E[3:1]
OSC_D[3:1]



1-2 ==> INACTIVE =1 after Power ON
3-2 ==> RUNNING=1 after Power ON

Frontpanel

DR1 DRILL 2P8 | DR2 DRILL 2P8 | DR3 DRILL 2P8 | DR4 DRILL 2P8 | DR5 DRILL 2P8

Rail

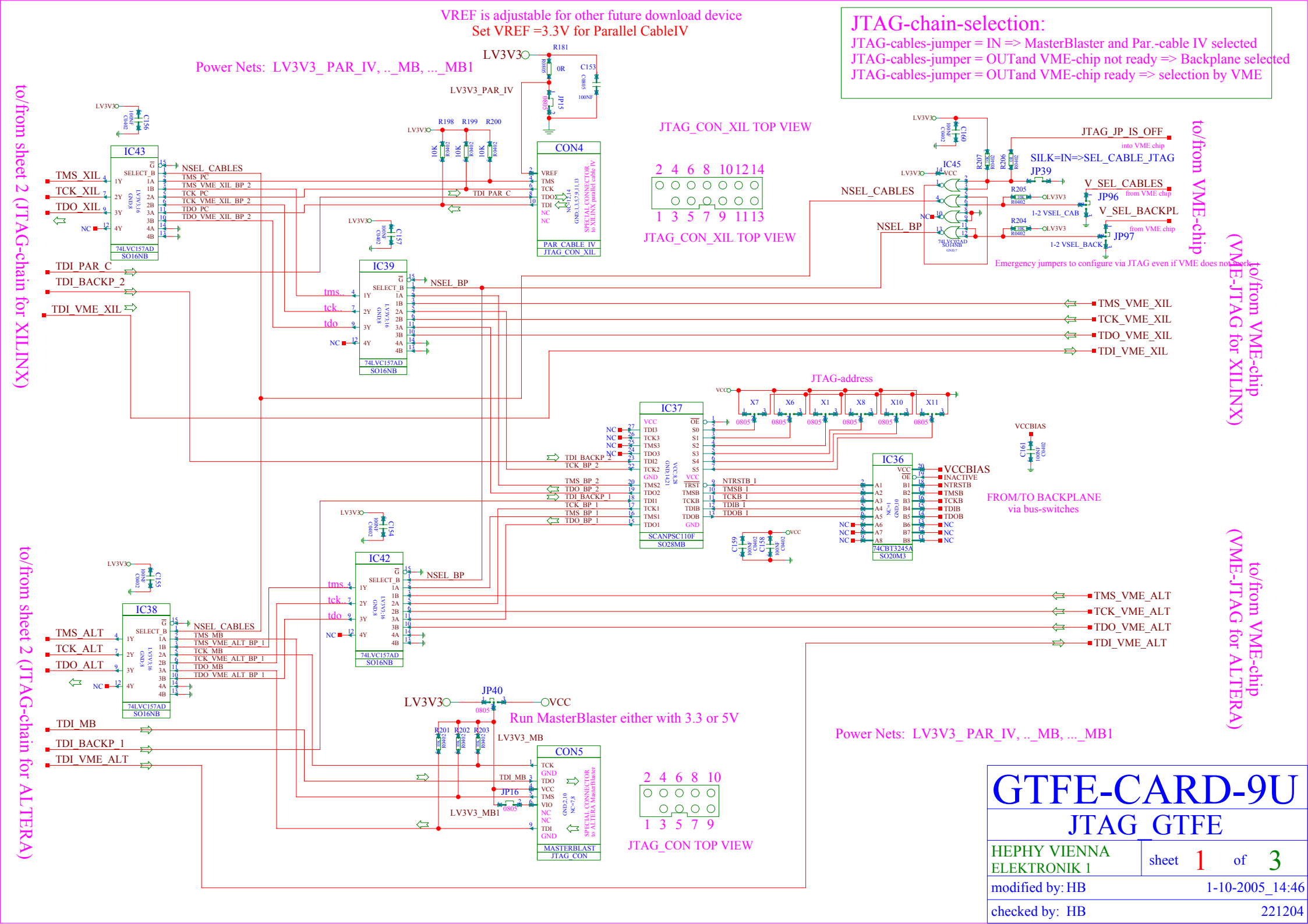
X5 DRILL 2P8 | X4 DRILL 2P8 | X3 DRILL 2P8 | X2 DRILL 2P8

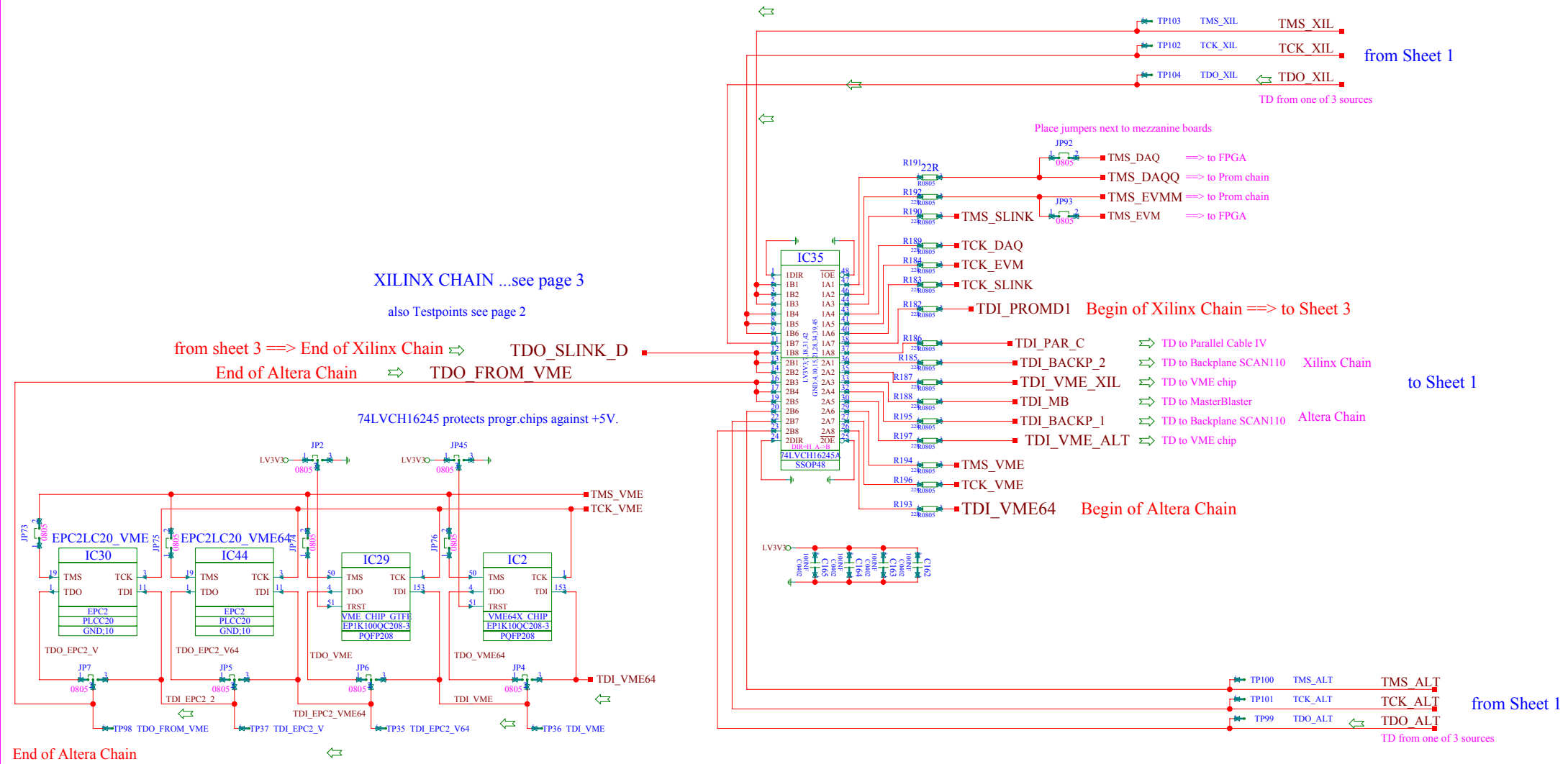
Front Panel space for 9U: >300 mm

GTFE-9U-CARD

FRONT_PAN_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.TAUROK	1-4-2005_9:18
checked by: AT	03-01-2005

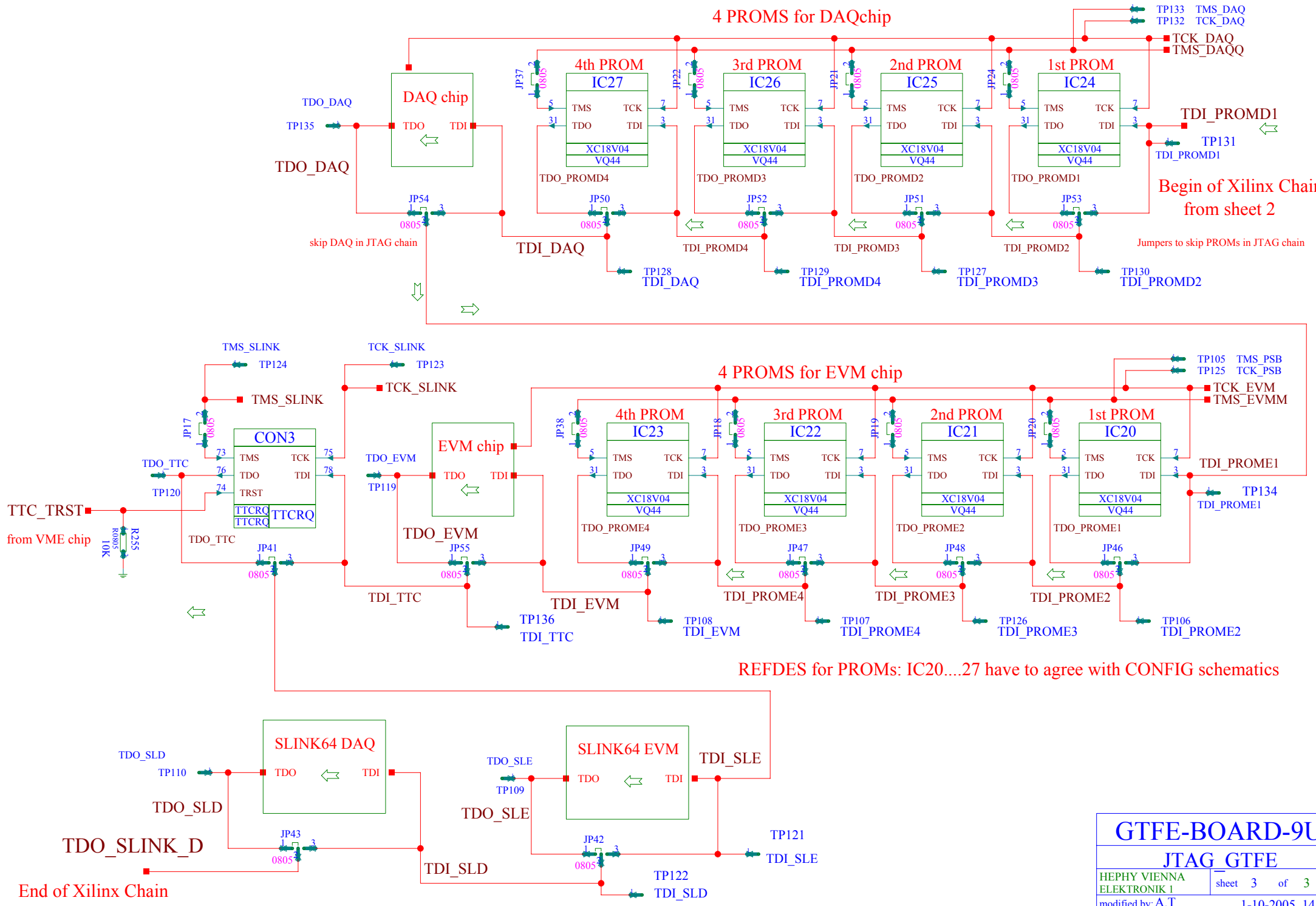

VREF is adjustable for other future download device
Set VREF =3.3V for Parallel CableIV
Power Nets: LV3V3_ PAR_IV, .._MB, ..._MB1
JTAG-chain-selection:
JTAG-cables-jumper = IN => MasterBlaster and Par.-cable IV selected
JTAG-cables-jumper = OUTand VME-chip not ready => Backplane selected
JTAG-cables-jumper = OUTand VME-chip ready => selection by VME
to/from sheet 2 (JTAG-chain for XILINX)
to/from sheet 2 (JTAG-chain for ALTERA)
to/from VME-chip (VME-JTAG for XILINX)
to/from VME-chip (VME-JTAG for ALTERA)
JTAG_CON_XIL TOP VIEW
JTAG_CON_XIL TOP VIEW
JTAG_CON TOP VIEW
JTAG-address
Run MasterBlaster either with 3.3 or 5V
Emergency jumpers to configure via JTAG even if VME does not work
FROM/TO BACKPLANE
via bus-switches
GTFE-CARD-9U
JTAG_GTFE
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 3
modified by: HB 1-10-2005_14:46
checked by: HB 221204



GTFE-CARD-9U

JTAG_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: AT	1-10-2005_14:46
checked by: HB	221204



GTFE-BOARD-9U	
JTAG_GTFE	
HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: A.T	1-10-2005_14:46
checked by: HB	221204

Compatible Types:

Adjustable Voltage Regulators replacing CS5206

LMS1585ACT-ADJ Linear 5A Adjustable Voltage Regulator, National Semiconductor

FAN1585AT Linear 5A Adjustable Voltage Regulator, Fairchild

LMS1084ACT-ADJ Linear 5A Adjustable Voltage Regulator, National Semiconductor

LMS1084IT-ADJ Linear 5A Adjustable Voltage Regulator, National Semiconductor / RS

Fixed 1.5 V Voltage Regulator:

LMS1585ACT-1.5 Linear 5A Fixed Voltage Regulator, National Semiconductor> For LMS1585ACT-1.5 remove 68R and 510R and replace C23 (33uF) and 12R by Solder_Bridge

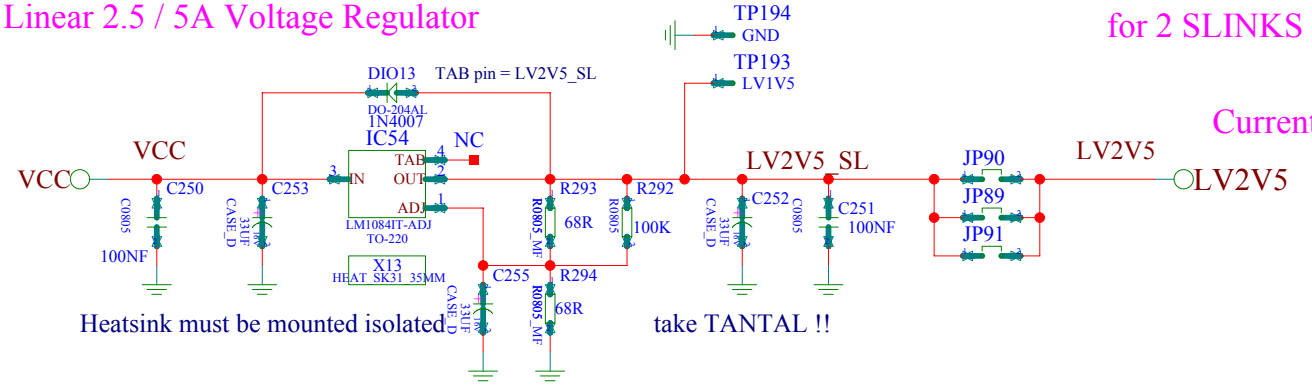
FAN1585AT-1.5 Linear 5A Fixed Voltage Regulator, Fairchild

LT1585AT-1.5 Linear 5A Fixed Voltage Regulator, Linear Technology

Linear 2.5 / 5A Voltage Regulator

for 2 SLINKS

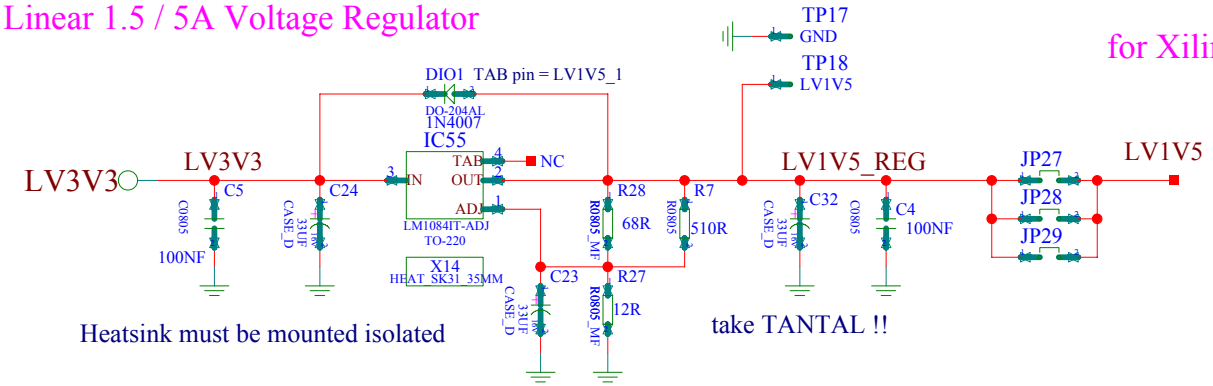
Current Limit <3A because of 35mm Heatsink



Linear 1.5 / 5A Voltage Regulator

for Xilinx Virtex2 FPGAs

Current Limit <5A because of 35mm Heatsink

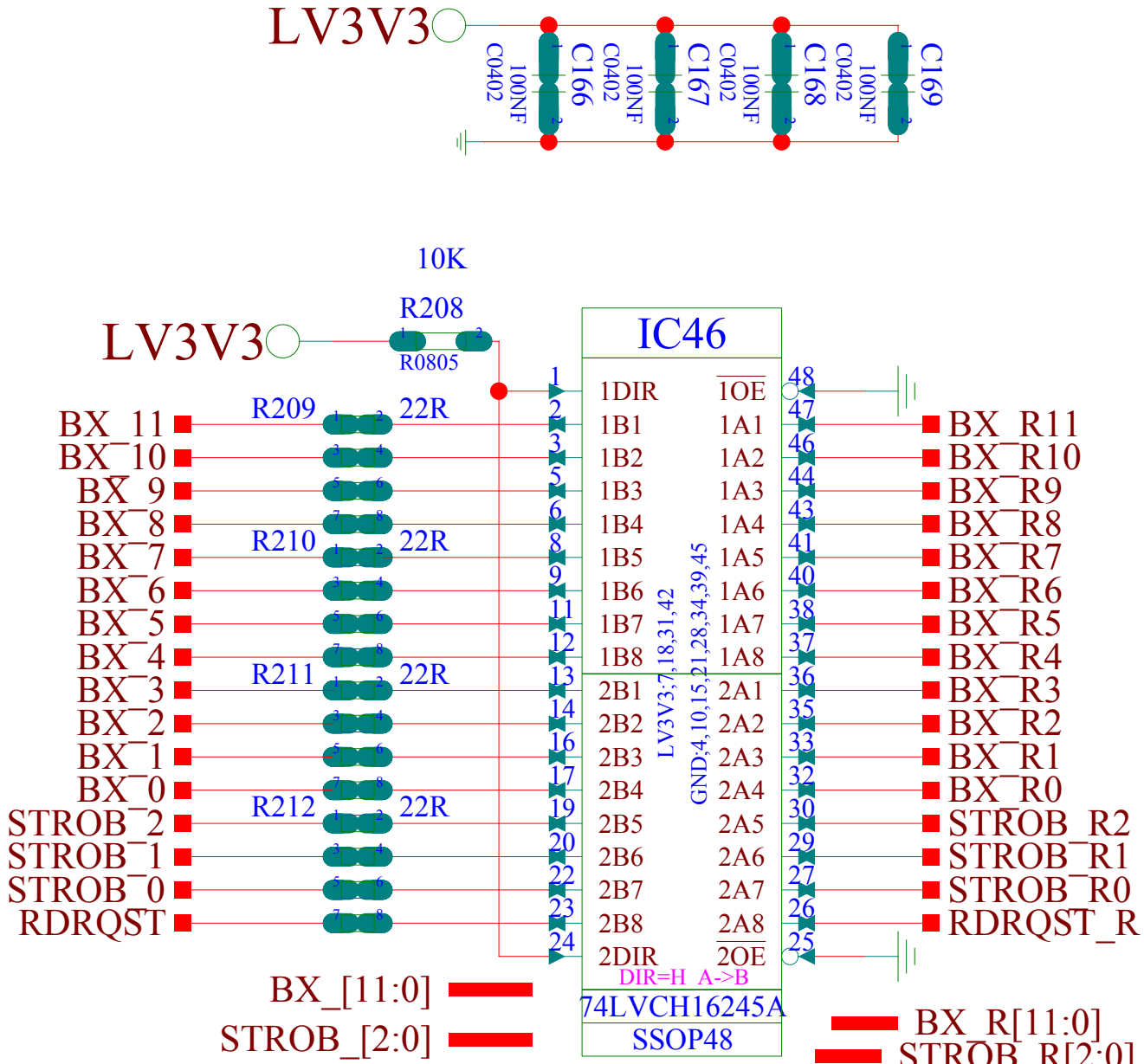


V_ref
(1.240...1.254..1.266)V/68.1 = 18.2...18.4...18.6 mA >10mA
250 mV /(18.2...18.6 mA) = 13.73...13.44 Ohm
Adjust voltage with R131 = 475....562 Ohm
I_adj=54 uA...can be neglected
all resistors for CS5206 in metalfilm

GTFE-CARD-9U

POWER_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.T.	1-3-2005_18:29
checked by: HB	221204



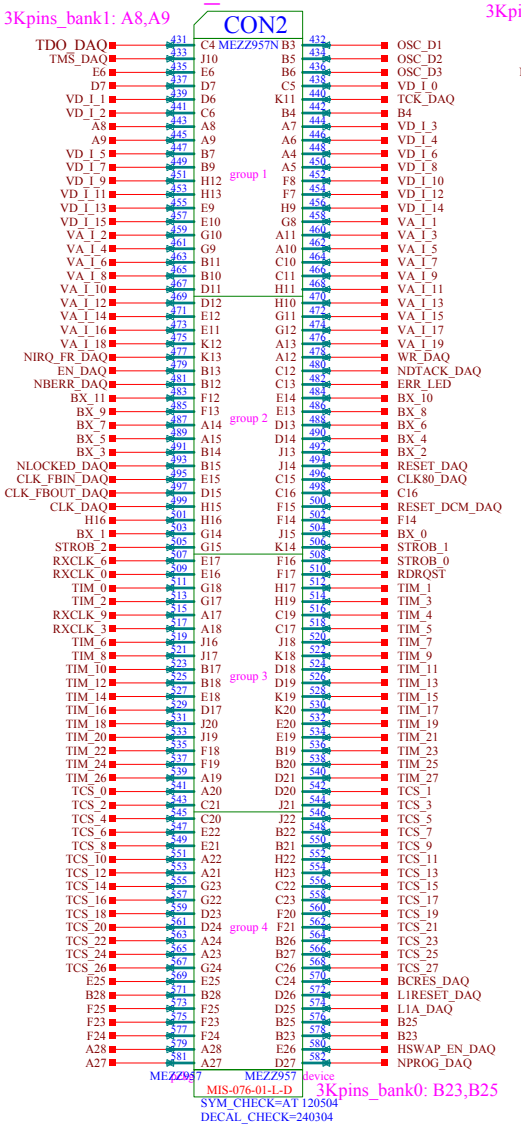
GTFE-BOARD-9U

ROBUS

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.T	1-3-2005_13:44
checked by: AT	030104

NORD MIS_076 connector

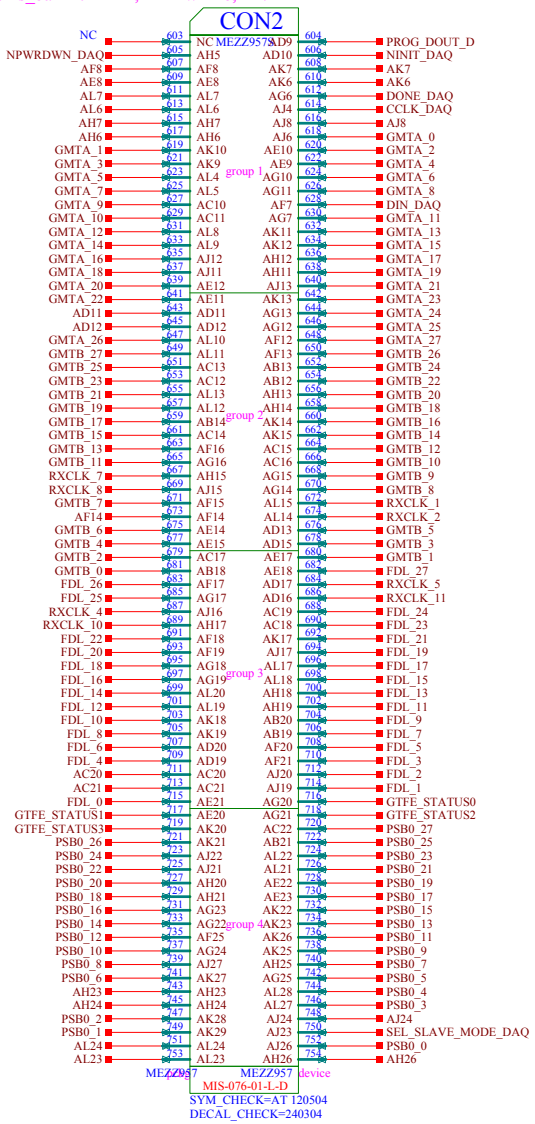
3Kpins_bank1: A8,A9



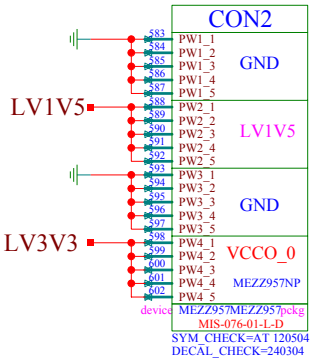
3Kpins_bank0: B23,B25

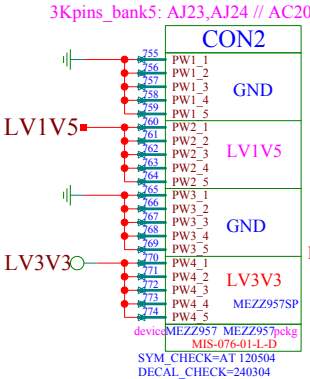
SOUTH MIS_076 connector

3Kpins_bank4: AD11,AD12 //AL6,AL7



3Kpins_bank5: AJ23,AJ24 // AC20,AC21 // AL23,AL24 // AH23,AH24





Default: Apply 3.3V to VCCO_0 (=Banks 0)

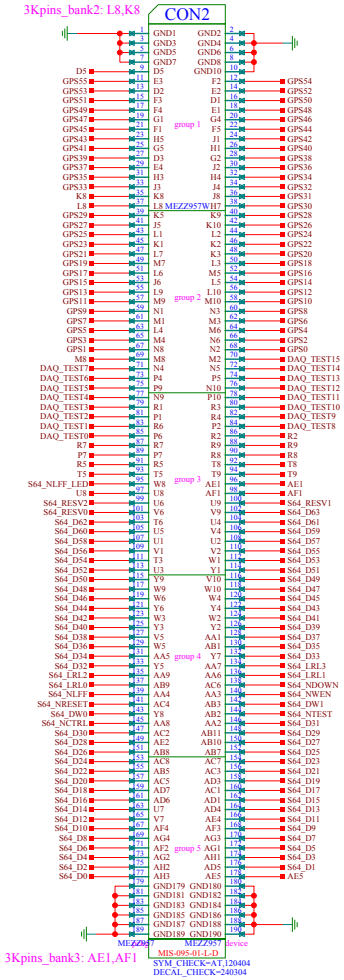
FDL,AUB,AUF: Apply 1.5V to VCCO_0 (=Banks 0) for GTL+ signals

APPLY always 3.3V to Banks 4,5

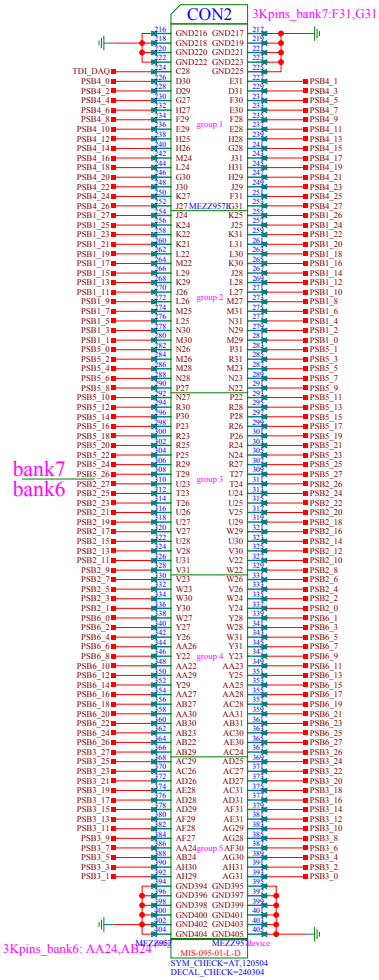
MEZZ957 TEMPLATE for 9U BOARDS

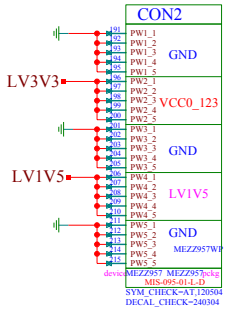
MEZZ957 TEMPLATE		
ROP_DAQ		
HEPHY VIENNA ELEKTRONIK 1	sheet 1	of 3
modified by: A.T 13.2.04	12-2-2004 14:59	
checked by: CHECKER	0-00-0000 00:00	

WEST MIS_095 connector

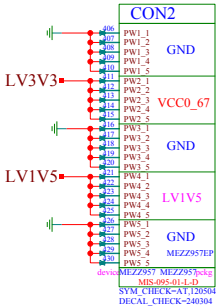


EAST MIS_095 connector





Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)



Default: Apply 3.3V to VCCO_67 (=Banks 6,7)
AUB,AUF,SRT: Apply 1.5V to VCCO_67 (=Banks 6&7) for GTL+ signals

MEZZ957 TEMPLATE for 9U BOARDS

MEZZ957 TEMPLATE

ROP_DAQ

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3	
modified by: AT 13.2.04		12-2-2004_14:59
checked by: CHECKER		0-00-0000_00:00

1CLB = 4 slices (as 2x2) 1slice= F+G LUT, 2 FF, hor.cascade OR,

Device	Row x Col.	/Slices/	RAM kbits/	Multiplier/	RAMBlocks (Kbits)/	DCMs/	maxIO pads
XC2V1000	40x32	5120	160	40	40	8	432
XC2V1500	48x40	7680	240	48	48	8	528

XC2V1500: =15360 DFF XC2V2000-4BF957 xxx io
XC2V1500-5FF896 413 $ XC2V3000-4BF957 xxx io

Monitor RAMs: (192+16+68)/16 = 18RAMblocks RingBuf (DPM)
18RAMblocks RO-Buf (Fifo)
1RAMblocks RX-Buf
1RAMblocks L1Aqueue 1 RAMblock =18 kbit DPRAM

XC2V3000 benötigt 3 Proms XC18V04VQ44C
XC2V4000 benötigt 4 Proms XC18V04VQ44C
XC2V6000 benötigt 6 Proms XC18V04VQ44C

VREF, CLK, Special PINS have to be on same pins on both MEZZ boards.

RESET Signale to DAQ chip
RESET_DCM_DAQ...resynchronizes CHIP to CLK
RESET_DAQ...==> GSR to STARTUP...resets all registers
INACTIVE ==> GTS to STARTUP...releases IO pins
NSYSRES ==> reconfigures DAQ chip from PROM

Testpoints for Oscilloscope on Front Panel
OSC_D[3:1]
ERR_LED
To Front side
PROG_DOUT_D

15 ctrl to SLINK
S64_NDOWN
S64_NWEN
S64_NTEST
S64_NLFF
S64_NRESET
S64_NCTRL
S64_RESV[2:0]
S64_LRL[3:0]
S64_DW[1:0]
S64_D[63:0]
64 data to SLINK

GPS[55:0]
52 GPS (TTCrq)

NORD
WEST
EAST
SOUTH
MEZZ957
bank0 bank1 bank2 bank3 bank4 bank5 bank6 bank7
72/70 84/82 76/68

RXCLK_[11:0]

Nets copied from GTFE9U schematic:
SEL_SLAVE_MODE_DAQ
CCLK_DAQ
DIN_DAQ
NINIT_DAQ
DONE_DAQ
NPROG_DAQ
6 CONFIG

VD_I_[15:0]
VA_I_[19:1]
NIRQ_FR_DAQ
WR_DAQ
EN_DAQ
NDTACK_DAQ
NBERR_DAQ
40 VME
Bank 1

RESET_DCM_DAQ
RESET_DAQ
NLOCKED_DAQ
NPWRDWN_DAQ
Bank 4
Bank 4

BX_[11:0]
STROB_[2:0]
RDRQST
16 RO-bus

TIM_[27:0]
TCS_[27:0]
PSB4_[27:0]
PSB1_[27:0]
PSB5_[27:0]
PSB2_[27:0]
PSB6_[27:0]
PSB3_[27:0]
PSB0_[27:0]
FDL_[27:0]
GMTB_[27:0]
GMTA_[27:0]
GTFE_STATUS[3:0]
336 INPUT data

5 CLOCK
4 DAQ STATUS

L1RESET_DAQ
L1A_DAQ
BCRES_DAQ
CLK_DAQ
CLK80_DAQ
Bank 4 CLOCK and TIMING

TDO_DAQ
TDI_DAQ
TMS_DAQ
TCK_DAQ
JTAG SIGNALS 4

Bank 4
CLK_TO_DAQ
TP168
CLK_DAQ
Bank 4: GCLK0P

CLK80_TO_DAQ
Bank 4
TP167
CLK80_DAQ
Bank 4: GCLK2P

TP94 DRILL_2.2MM
TP95 DRILL_2.2MM

TESTPOINTS for internal Signals
TP20
DAQ_TEST15
DAQ_TEST14
DAQ_TEST13
DAQ_TEST12
DAQ_TEST11
DAQ_TEST10
DAQ_TEST9
DAQ_TEST8
TEST_PIN7
TEST_PIN6
TEST_PIN5
TEST_PIN4
TEST_PIN3
TEST_PIN2
TEST_PIN1
TEST_PIN0
TEST_8PIN
DAQ_TEST15-8

TP19
DAQ_TEST7
DAQ_TEST6
DAQ_TEST5
DAQ_TEST4
DAQ_TEST3
DAQ_TEST2
DAQ_TEST1
DAQ_TEST0
DAQ_TEST7-0

DAQ_TEST[15:0]

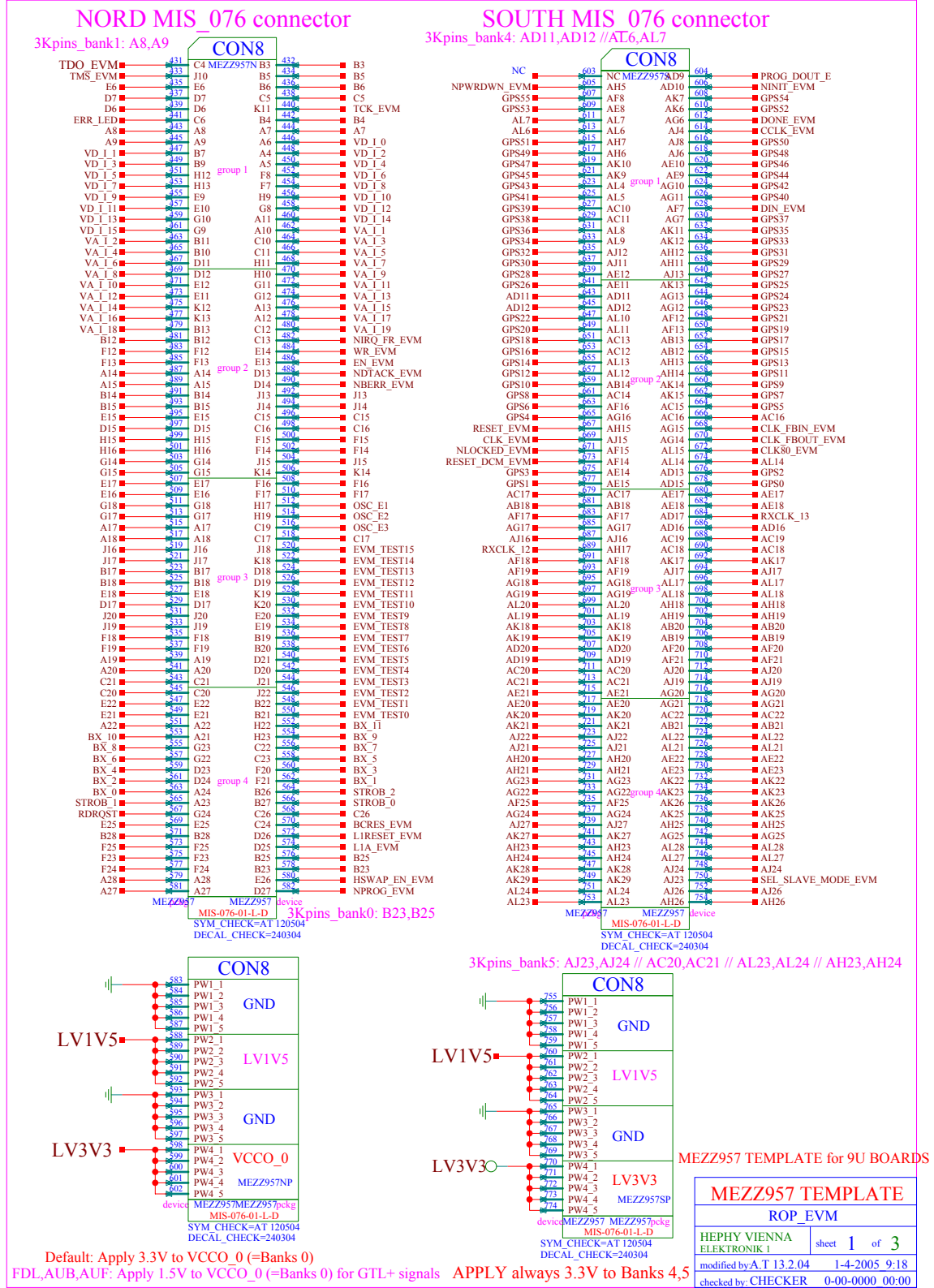
LV3V3
10K
IP2SHSWAP_EN
HSWAP_EN_DAQ
bank0
HSWAP_EN auch auf Symbol gezeichnet.

XC2V3000

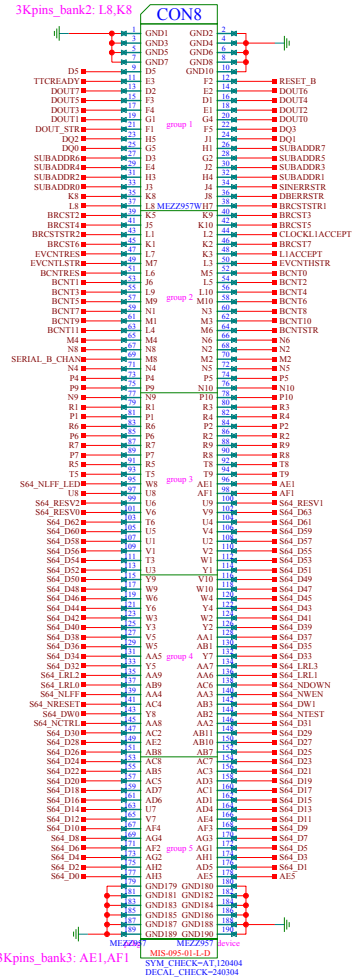
NPWRDWN_B is bidirectional pin!!
NPWRDWN_for each Virtex chip necessary!

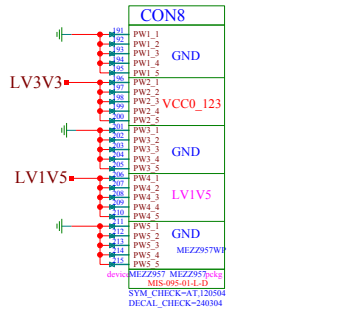
GTFE-BOARD-9U
ROP_DAQ

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: AT	12-2-2004_9:49
checked by: CHECKER	0-00-0000_00:00


NORD MIS_076 connector
3Kpins_bank1: A8,A9
CON8
TDO_EVM
TMS_EVM
ERR_LED
VD_I_1
VD_I_3
VD_I_5
VD_I_7
VD_I_9
VD_I_11
VD_I_13
VD_I_15
VA_I_2
VA_I_4
VA_I_6
VA_I_8
VA_I_10
VA_I_12
VA_I_14
VA_I_16
VA_I_18
group 1
group 2
group 3
group 4
VD_I_0
VD_I_2
VD_I_4
VD_I_6
VD_I_8
VD_I_10
VD_I_12
VD_I_14
VA_I_1
VA_I_3
VA_I_5
VA_I_7
VA_I_9
VA_I_11
VA_I_13
VA_I_15
VA_I_17
VA_I_19
NIRQ_FR_EVM
WR_EVM
EN_EVM
NDTACK_EVM
NBERR_EVM
J13
J14
C15
C16
F15
F14
J15
K14
F16
F17
OSC_E1
OSC_E2
OSC_E3
C17
EVM_TEST15
EVM_TEST14
EVM_TEST13
EVM_TEST12
EVM_TEST11
EVM_TEST10
EVM_TEST9
EVM_TEST8
EVM_TEST7
EVM_TEST6
EVM_TEST5
EVM_TEST4
EVM_TEST3
EVM_TEST2
EVM_TEST1
EVM_TEST0
BX_11
BX_9
BX_7
BX_5
BX_3
BX_1
STROB_2
STROB_0
C26
BCRES_EVM
L1RESET_EVM
L1A_EVM
B25
B23
HSWAP_EN_EVM
NPROG_EVM
MEZZ957
MEZZ957 device
MIS-076-01-L-D
SYM_CHECK=AT 120504
DECAL_CHECK=240304
3Kpins_bank0: B23,B25
SOUTH MIS_076 connector
3Kpins_bank4: AD11,AD12 //AL6,AL7
CON8
NC
NPWRDWN_EVM
RESET_EVM
CLK_EVM
NLOCKED_EVM
RESET_DCM_EVM
RXCLK_12
RXCLK_13
group 1
group 2
group 3
group 4
PROG_DOUT_E
NINIT_EVM
DONE_EVM
CCLK_EVM
DIN_EVM
SEL_SLAVE_MODE_EVM
CLK_FBIN_EVM
CLK_FBOUT_EVM
CLK80_EVM
MEZZ957
MEZZ957 device
MIS-076-01-L-D
SYM_CHECK=AT 120504
DECAL_CHECK=240304
3Kpins_bank5: AJ23,AJ24 // AC20,AC21 // AL23,AL24 // AH23,AH24
CON8
PW1_1
PW1_2
PW1_3
PW1_4
PW1_5
GND
LV1V5
PW2_1
PW2_2
PW2_3
PW2_4
PW2_5
PW3_1
PW3_2
PW3_3
PW3_4
PW3_5
LV3V3
PW4_1
PW4_2
PW4_3
PW4_4
PW4_5
VCCO_0
MEZZ957NP
MEZZ957SP
device
MEZZ957 MEZZ957pckg
MIS-076-01-L-D
SYM_CHECK=AT 120504
DECAL_CHECK=240304
MEZZ957 TEMPLATE for 9U BOARDS
MEZZ957 TEMPLATE
ROP_EVM
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 3
modified by: A.T 13.2.04 1-4-2005 9:18
checked by: CHECKER 0-00-0000 00:00
Default: Apply 3.3V to VCCO_0 (=Banks 0)
FDL,AUB,AUF: Apply 1.5V to VCCO_0 (=Banks 0) for GTL+ signals
APPLY always 3.3V to Banks 4,5

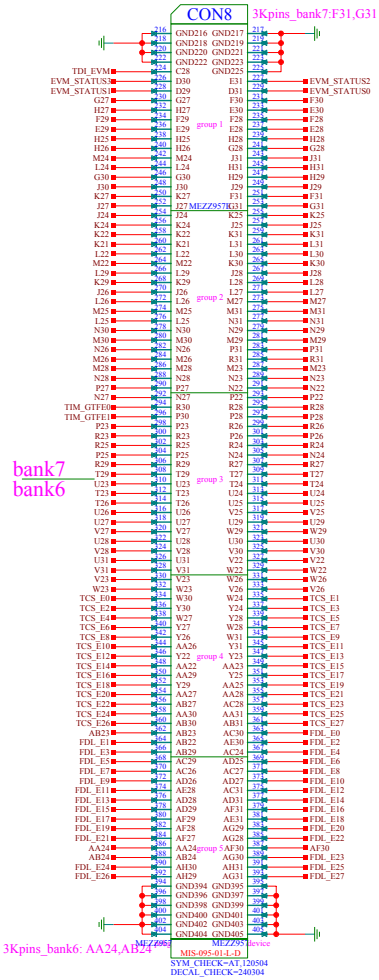
WEST MIS_095 connector

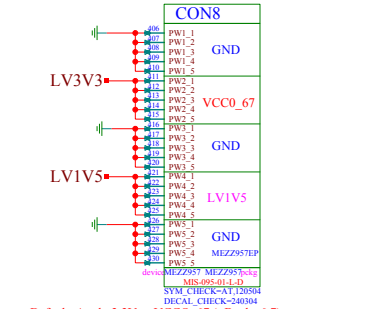




Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)

EAST MIS_095 connector





Default: Apply 3.3V to VCCO_67 (=Banks 6,7)
AUB,AUF,SRT: Apply 1.5V to VCCO_67 (=Banks 6&7) for GTL+ signals

MEZZ957 TEMPLATE for 9U BOARDS

MEZZ957 TEMPLATE

ROP_EVM

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: AT 13.2.04	1-4-2005_9:18
checked by: CHECKER	0-00-0000_00:00

1CLB = 4 slices (as 2x2) 1slice= F+G LUT, 2 FF, hor.cascade OR,

Device	Row x Col.	/Slices/	RAM kbits/	Multiplier/	RAMBlocks (Kbits)/	DCMs/	maxIO pads
XC2V1000	40x32	5120	160	40	40	8	432
XC2V1500	48x40	7680	240	48	48	8	528

XC2V1500: =15360 DFF XC2V2000-4BF957 xxx io
XC2V1500-5FF896 413 $ XC2V3000-4BF957 xxx io

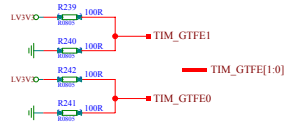
Monitor RAMs: (192+16+68)/16 = 18RAMblocks RingBuf (DPM)
18RAMblocks RO-Buf (Fifo)
1RAMblocks RX-Buf
1RAMblocks L1Aqueue 1 RAMblock =18 kbit DPRAM

XC2V3000 benötigt 3 Proms XC18V04VQ44C
XC2V4000 benötigt 4 Proms XC18V04VQ44C
XC2V6000 benötigt 6 Proms XC18V04VQ44C

VREF, CLK, Special PINS have to be on same pins on both MEZZ boards.

RESET Signale to DAQ chip
RESET_DCM_DAQ...resynchronizes CHIP to CLK
RESET_DAQ...==> GSR to STARTUP...resets all registers
~~INACTIVE ==> GTS to STARTUP...releases IO pins~~
NSYSRES ==> reconfigures DAQ chip from PROM

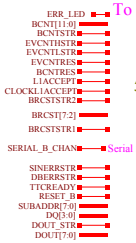
1.) TIM6U sends LVDS: TIM chip: GTFE1 from K17 (N), GTFE0 from K18 (P) pins
2.) TIM6U sends LVTTL signals
2a) LVTTL: TIM_GTFE1: GTFE ==> TIM and
2b) LVTTL: TIM_GTFE0: GTFE <== TIM



15 ctrl to SLINK

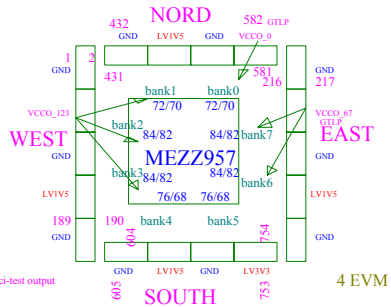
S64_RESV[2:0]
S64_LRL[3:0]
S64_DWL[1:0]
S64_D[63:0] 64 data to SLINK

GPS[55:0] 52 GPS (TTCrq)
To Front side



52 GPS (TTCrq)
Serial Signal of TTCrx can be sent to Osci-test output

OSC_E[3:1] Testpoints for Oscilloscope



Nets copied from GTFE9U schematic:

SEL_SLAVE_MODE_EVM ==>AJ23 ==> wired to MODE2,1,0 on modified MEZZ957

PROG_DOUT_E
SEL_SLAVE_MODE_EVM
CCLK_EVM
DIN_EVM
NINIT_EVM
DONE_EVM
NPROG_EVM
6 CONFIG

VD_I_[15:0]
VA_I_[19:1]
40 VME
NIRQ_FR_EVM
WR_EVM
EN_EVM
NDTACK_EVM
NBERR_EVM
Bank 1

RESET_DCM_EVM
RESET_EVM
NLOCKED_EVM
NPWRDWN_EVM
Bank 4
Bank 4

BX_[11:0]
STROB_[2:0]
RDROST
16 RO-bus

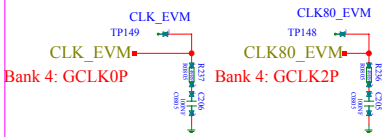
TCS_E[27:0]
FDL_E[27:0]
RXCLK_[13:12]
56+2 INPUT data

4 EVM STATUS EVM_STATUS[3:0]

5 CLOCK

L1RESET_EVM
L1A_EVM
BCRES_EVM
CLK_EVM
CLK80_EVM
Bank 4 CLOCK and TIMING

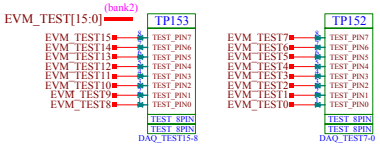
TDO_EVM
TDI_EVM
TMS_EVM
TCK_EVM
JTAG SIGNALS 4



TP150 DRILL_2.2MM
TP151 DRILL_2.2MM

CLK_FBOUT_EVM
CLK_FBIN_EVM

TESTPOINTS for internal Signals



HSWAP_EN auch auf Symbol gezeichnet.

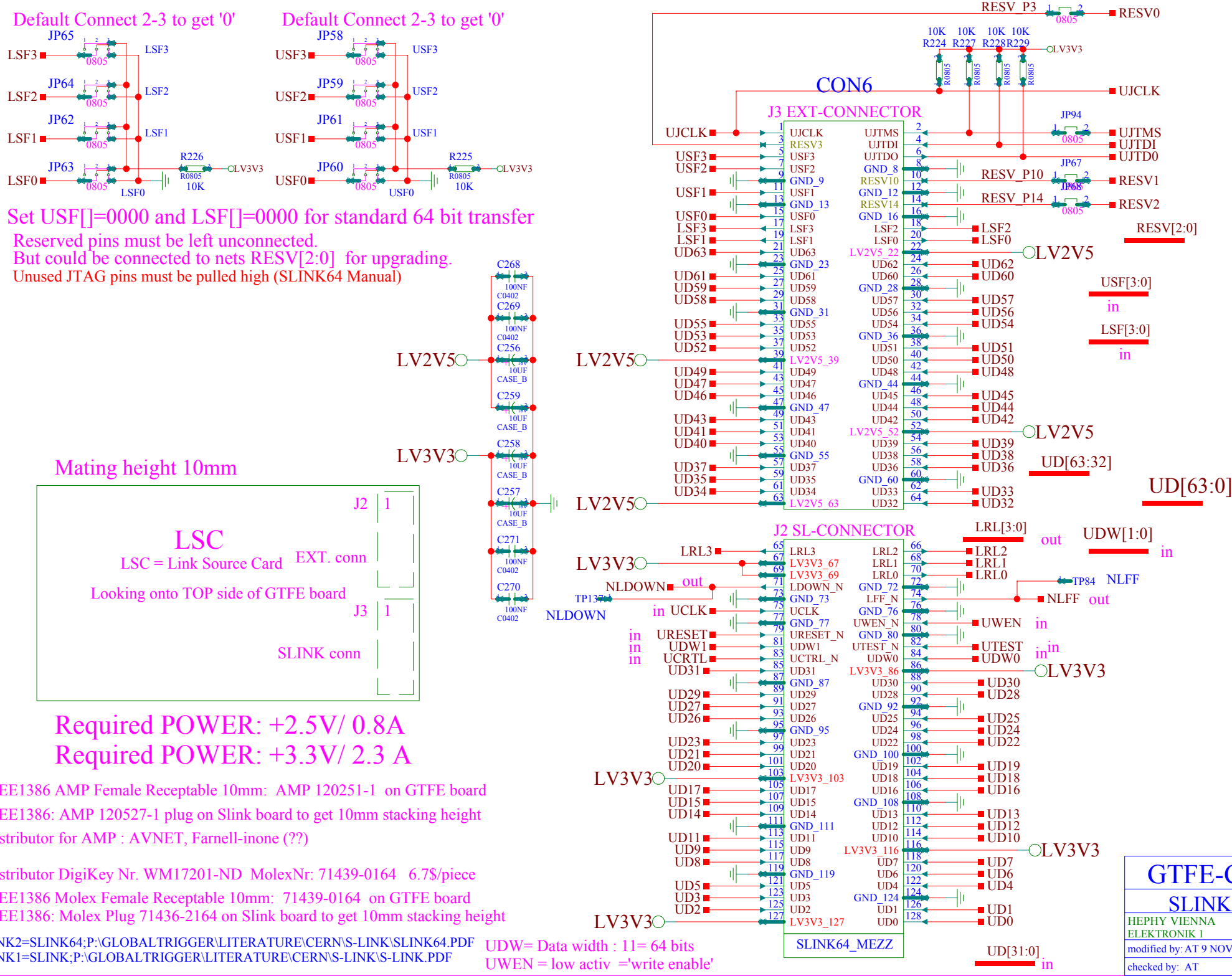
XC2V2000

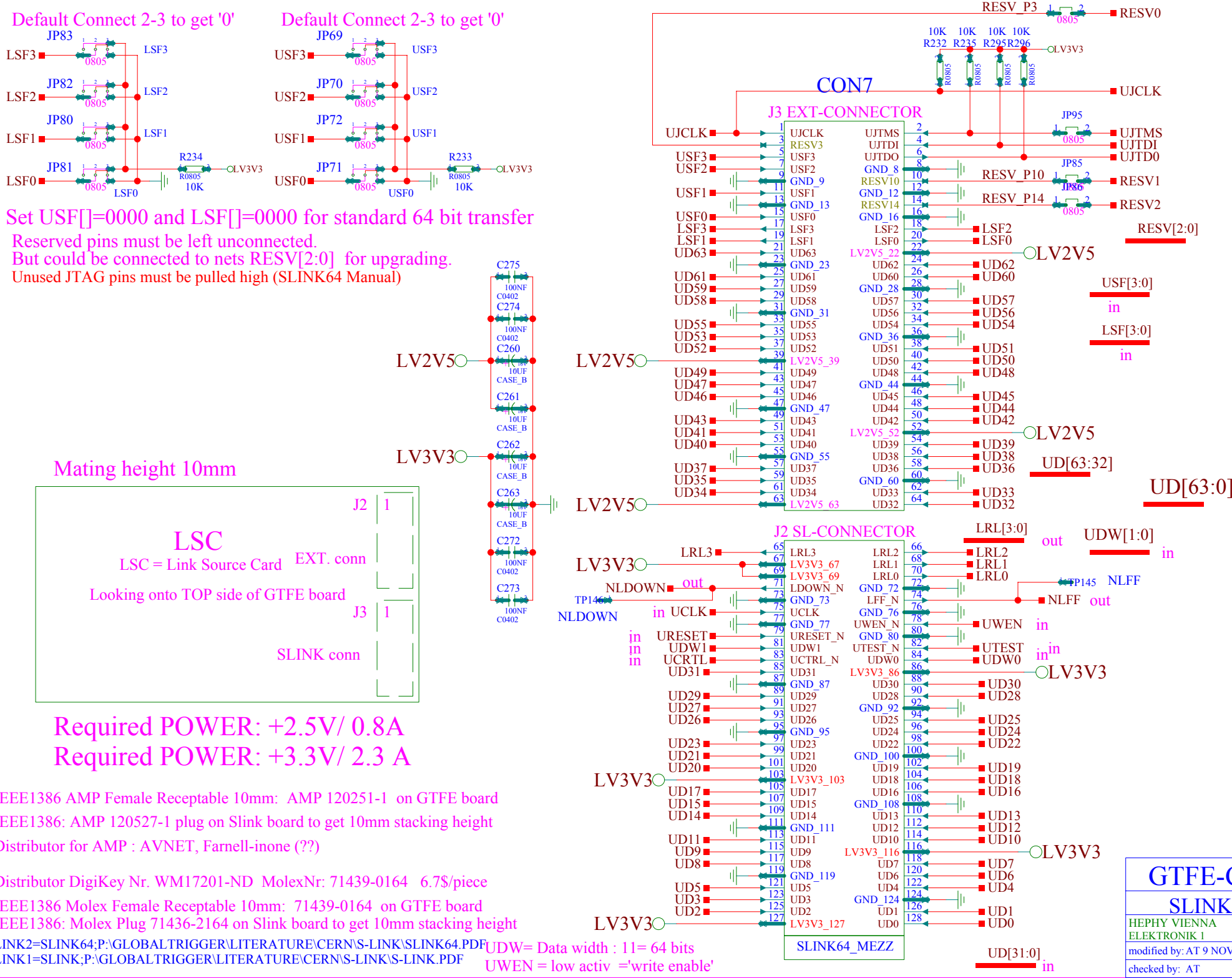
NPWRDWN_B is bidirectional pin!!
NPWRDWN_for each Virtex chip necessary!

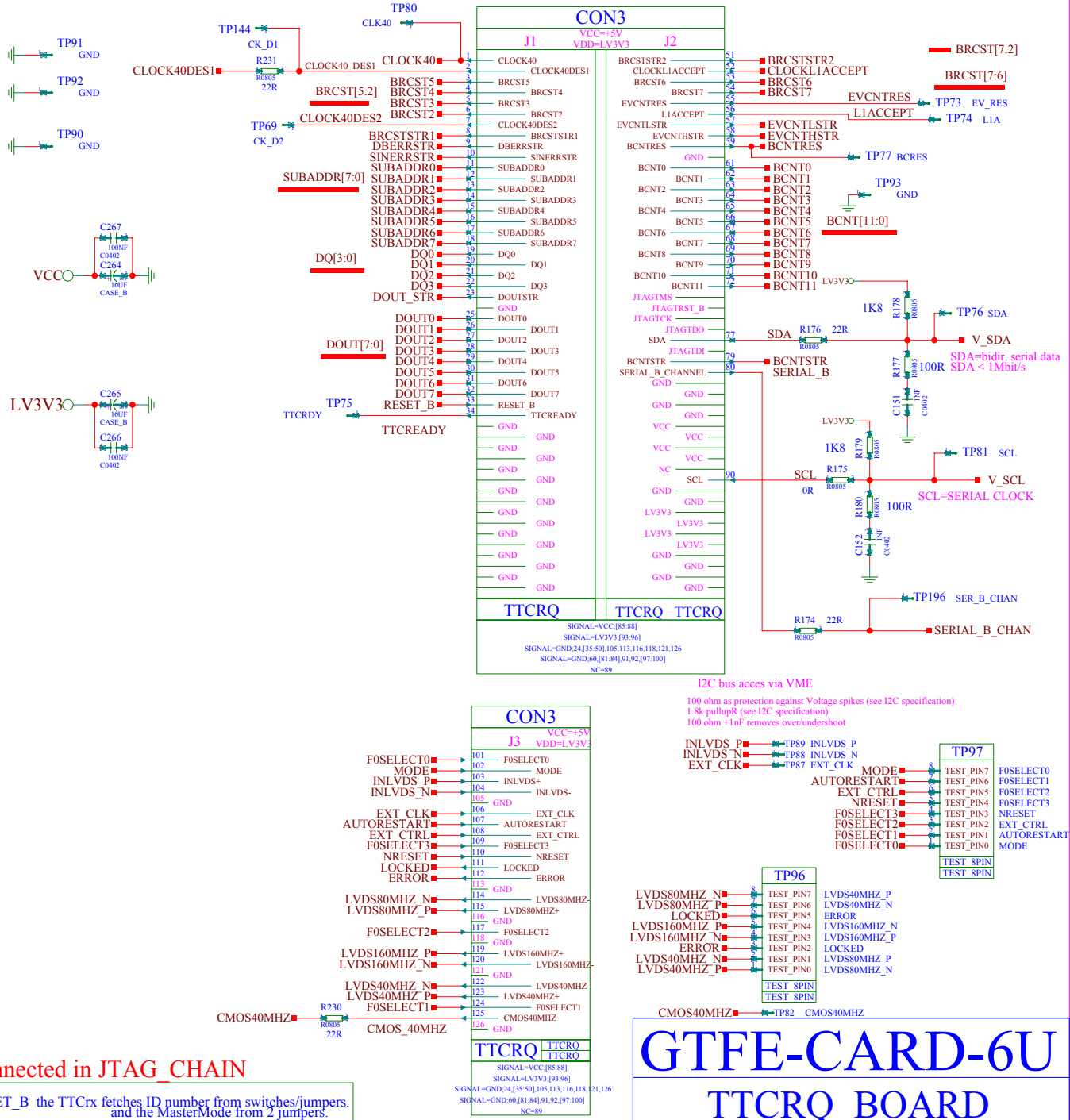
GTFE-BOARD-9U

ROP_EVM

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: AT	1-4-2005_13:58
checked by: CHECKER	0-00-0000_00:00


Default Connect 2-3 to get '0'
Default Connect 2-3 to get '0'
Set USF[]=0000 and LSF[]=0000 for standard 64 bit transfer
Reserved pins must be left unconnected.
But could be connected to nets RESV[2:0] for upgrading.
Unused JTAG pins must be pulled high (SLINK64 Manual)
Mating height 10mm
LSC
LSC = Link Source Card
EXT. conn
Looking onto TOP side of GTFE board
SLINK conn
Required POWER: +2.5V/ 0.8A
Required POWER: +3.3V/ 2.3 A
IEEE1386 AMP Female Receptable 10mm: AMP 120251-1 on GTFE board
IEEE1386: AMP 120527-1 plug on Slink board to get 10mm stacking height
Distributor for AMP : AVNET, Farnell-inone (??)
Distributor DigiKey Nr. WM17201-ND MolexNr: 71439-0164 6.7$/piece
IEEE1386 Molex Female Receptable 10mm: 71439-0164 on GTFE board
IEEE1386: Molex Plug 71436-2164 on Slink board to get 10mm stacking height
LINK2=SLINK64;P:\GLOBALTRIGGER\LITERATURE\CERN\S-LINK\SLINK64.PDF
LINK1=SLINK;P:\GLOBALTRIGGER\LITERATURE\CERN\S-LINK\S-LINK.PDF
UDW= Data width : 11= 64 bits
UWEN = low activ ='write enable'
CON6
J3 EXT-CONNECTOR
J2 SL-CONNECTOR
SLINK64_MEZZ
LV2V5
LV3V3
LV3V3
RESV[2:0]
USF[3:0]
LSF[3:0]
UD[63:32]
UD[63:0]
UD[31:0]
LRL[3:0]
UDW[1:0]
GTFE-CARD-9U
SLINK64_DAQ
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by: AT 9 NOV 2004
1-10-2005 14:46
checked by: AT
03-01-2005


Default Connect 2-3 to get '0'
Default Connect 2-3 to get '0'
Set USF[]=0000 and LSF[]=0000 for standard 64 bit transfer
Reserved pins must be left unconnected.
But could be connected to nets RESV[2:0] for upgrading.
Unused JTAG pins must be pulled high (SLINK64 Manual)
Mating height 10mm
LSC
LSC = Link Source Card
EXT. conn
Looking onto TOP side of GTFE board
SLINK conn
Required POWER: +2.5V/ 0.8A
Required POWER: +3.3V/ 2.3 A
IEEE1386 AMP Female Receptable 10mm: AMP 120251-1 on GTFE board
IEEE1386: AMP 120527-1 plug on Slink board to get 10mm stacking height
Distributor for AMP : AVNET, Farnell-inone (??)
Distributor DigiKey Nr. WM17201-ND MolexNr: 71439-0164 6.7$/piece
IEEE1386 Molex Female Receptable 10mm: 71439-0164 on GTFE board
IEEE1386: Molex Plug 71436-2164 on Slink board to get 10mm stacking height
LINK2=SLINK64;P:\GLOBALTRIGGER\LITERATURE\CERN\S-LINK\SLINK64.PDF
LINK1=SLINK;P:\GLOBALTRIGGER\LITERATURE\CERN\S-LINK\S-LINK.PDF
UDW= Data width : 11= 64 bits
UWEN = low activ ='write enable'
CON7
J3 EXT-CONNECTOR
J2 SL-CONNECTOR
SLINK64_MEZZ
RESV_P3
RESV0
RESV_P10
RESV1
RESV_P14
RESV2
RESV[2:0]
UJCLK
UJTMS
UJTDI
UJTDO
LV2V5
LV3V3
USF[3:0]
LSF[3:0]
UD[63:32]
UD[63:0]
UD[31:0]
LRL[3:0]
UDW[1:0]
NLDOWN
NLFF
UCLK
URESET
UDW1
UCTRL
UWEN
UTEST
UDW0
GTFE-CARD-9U
SLINK64_EVM
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by: AT 9 NOV 2004
1-10-2005 14:46
checked by: AT
03-01-2005



Copied from TTCrq Manual

JTAG pins are connected in JTAG_CHAIN

During RESET_B the TTCrx fetches ID number from switches/jumpers.
and the MasterMode from 2 jumpers.

RESET_B >50 musec for 100k pullup

enPROM to VDD to enable PROM

PROM contains fine-tune parameters and ID-number (overwriting jumper-ID)

Find I2C bus definition!!!!Check 3V3 Anschlussmoeglichkeit

GTFE-CARD-6U

TTCRQ_BOARD

HEPHY VIENNA
ELEKTRONIK 1

sheet 1 of 1

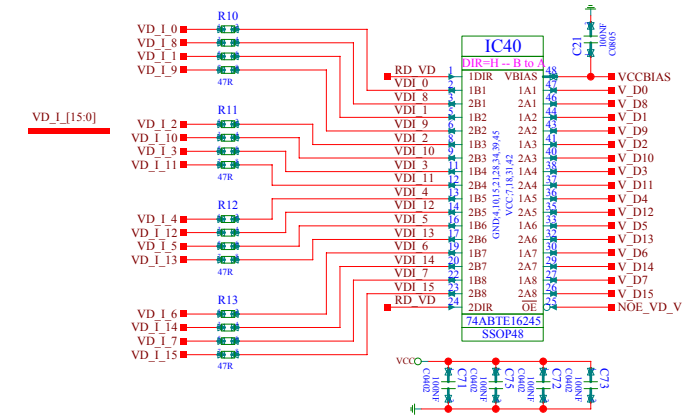
modified by: H. BERGAUER 1-4-2005_9:18

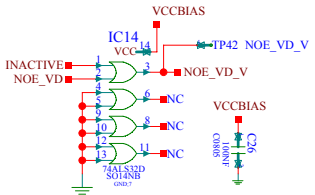
checked by: AT 03-01-2005

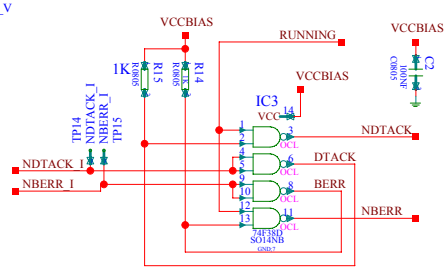
47 Ohm resistors protect the Virtex drivers against overvoltage spikes.

PSB9U must not be inserted into the 6U Backplane!!!

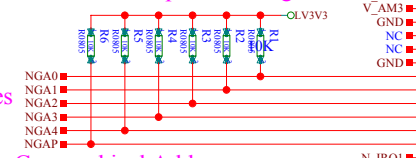
D1 = VCC on BACK6U
D1 = LV3V3bias on BACK9U







Keep NDTACK NBERR inactive while VME64X chip is unconfigured



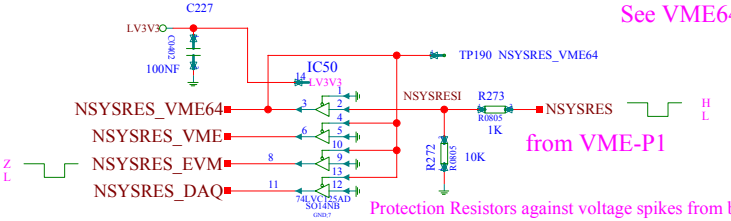
inverted values

Geographical Addresses

Parity bit: for odd parity

slot=1: GA=0 0001 => GAP=0
slot=2: GA=0 0010 => GAP=0
slot=3: GA=0 0011 => GAP=1
etc

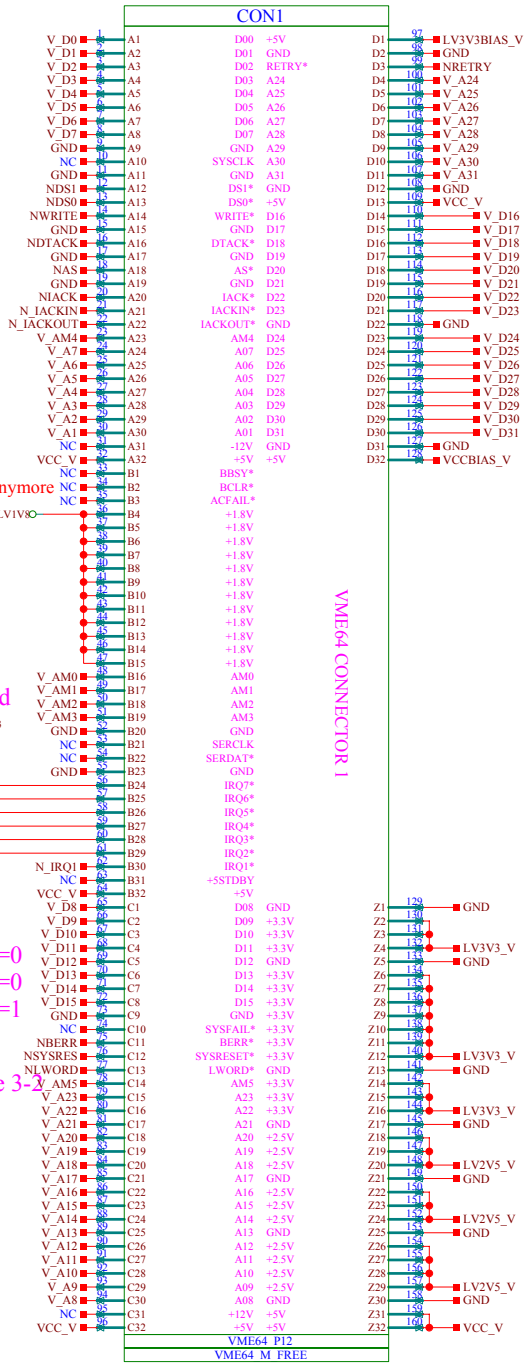
See VME64x.pdf page 10 Table 3-2



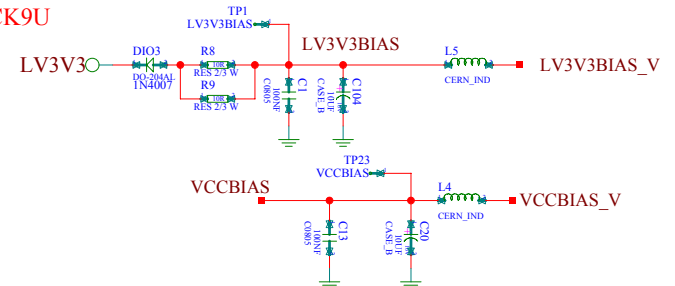
Protection Resistors against voltage spikes from backplane.

NSYSRES reconfigures all Altera and Xilinx programmable chips.

LV1V8_V not used anymore

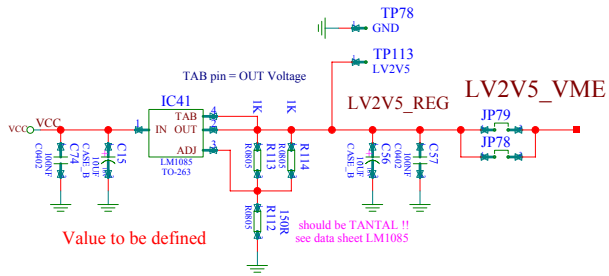


LV2V5_V not used anymore



Do not solder this part.

Unused 2.5V plane can be connected to 3.3V optionally on 9U backplane if GTL-6U is not used anymore in Crate



Value to be defined

should be TANTAL !!
see data sheet LM1085

Do not use LV2V5 and LV1V8 from BACKPLANE-6U

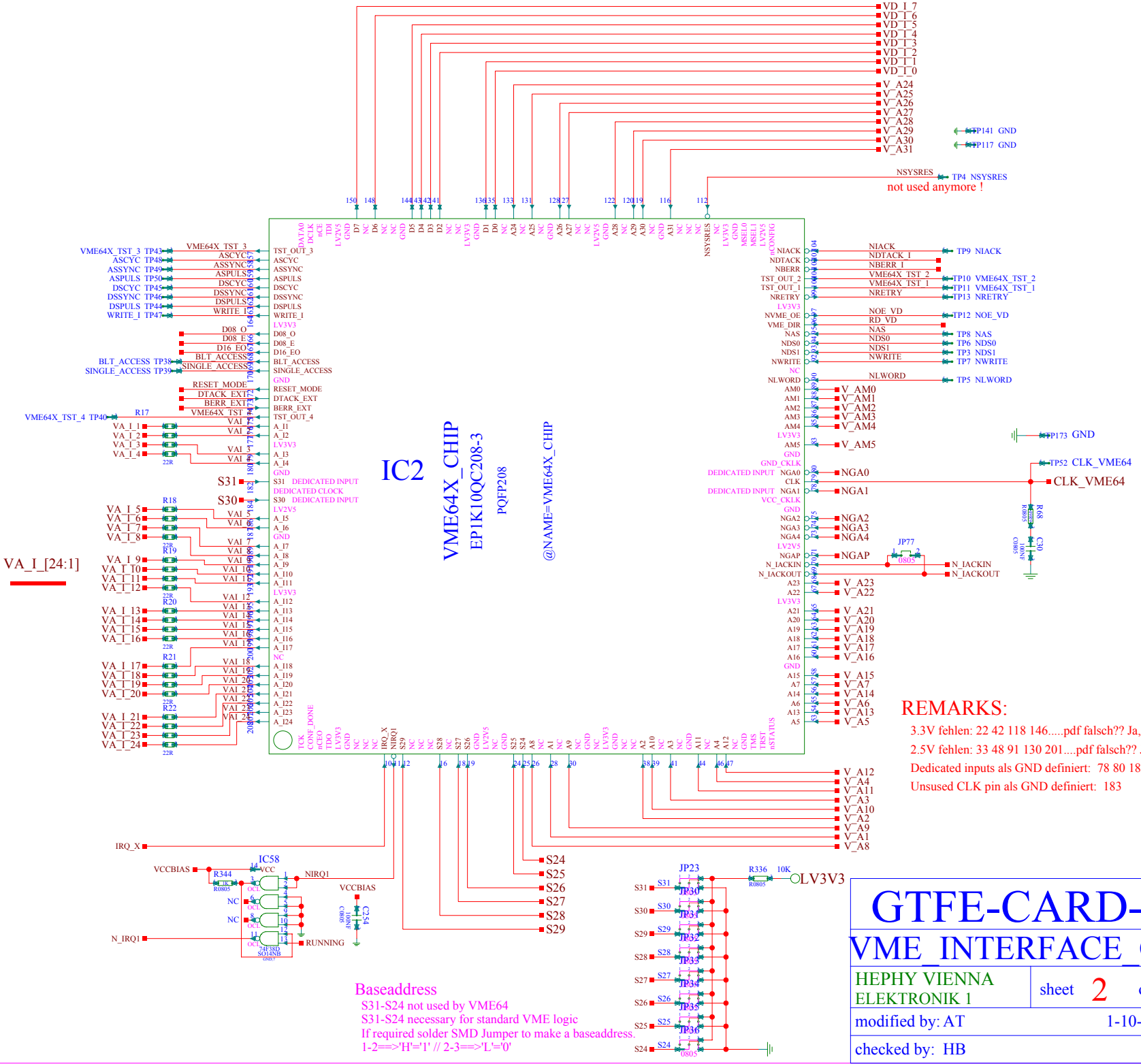
LV2V5 and LV1V8 will not be connected on the Backplane-9U

Stecker und Signale mit GTL und TIM schematic vergleichen

GTFE-CARD-9U

VME_INTERFACE_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3	
modified by: H. BERGAUER		1-4-2005_15:43
checked by: HB		221204



REMARKS:

3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Refere

2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Ref

Dedicated inputs als GND definiert: 78 80 182 184

Unsused CLK pin als GND definiert: 183

Baseaddress

S31-S24 not used by VME64

S31-S24 necessary for standard VME logic

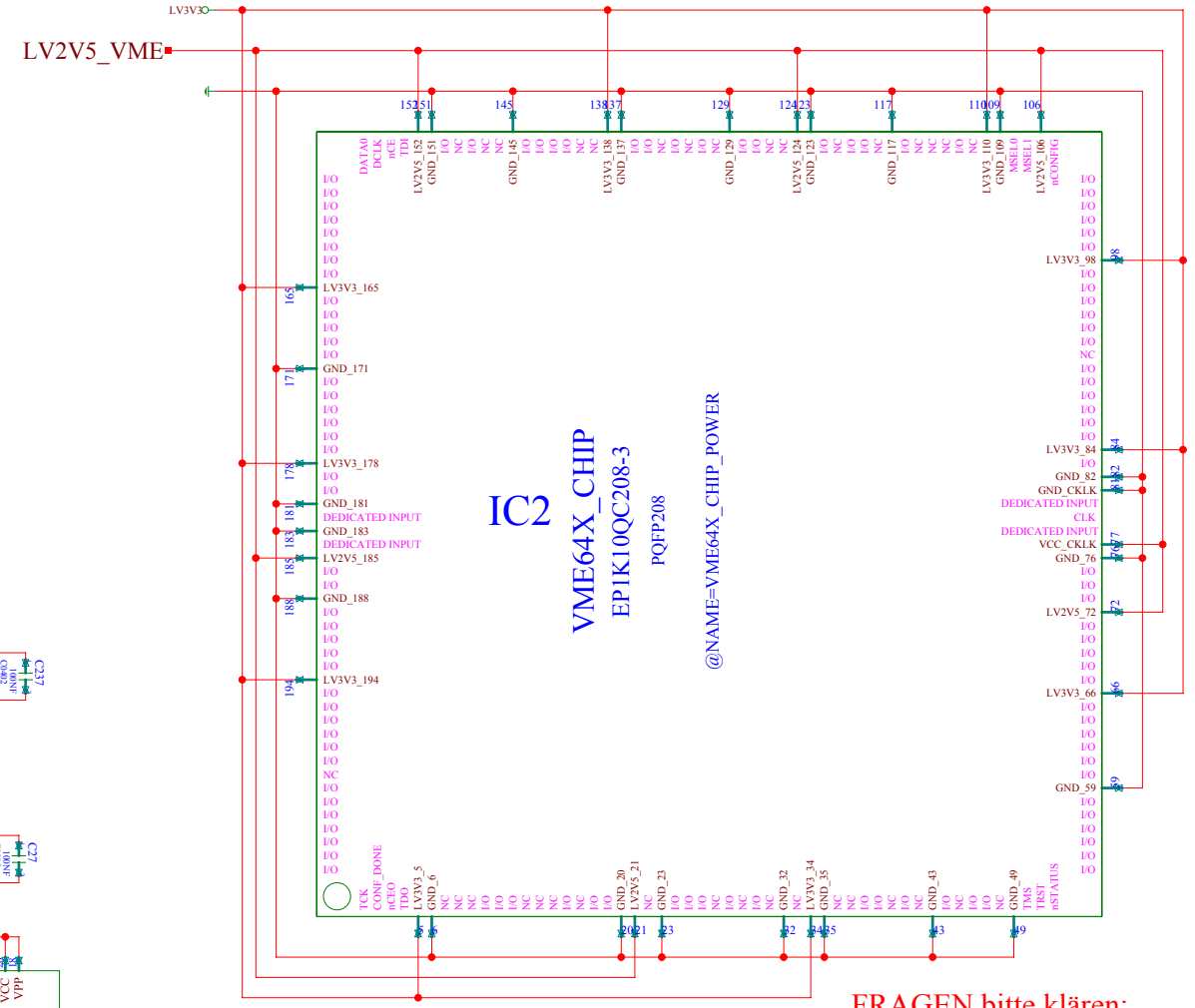
If required solder SMD Jumper to make a baseaddress.

1-2==>'H'='1' // 2-3==>'L'='0'

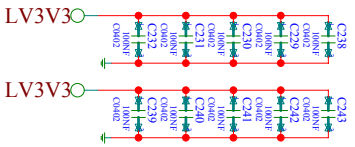
GTFE-CARD-9U

VME_INTERFACE_GTFE

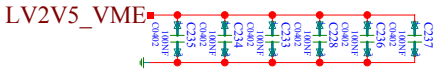
HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: AT	1-10-2005_14:46
checked by: HB	221204

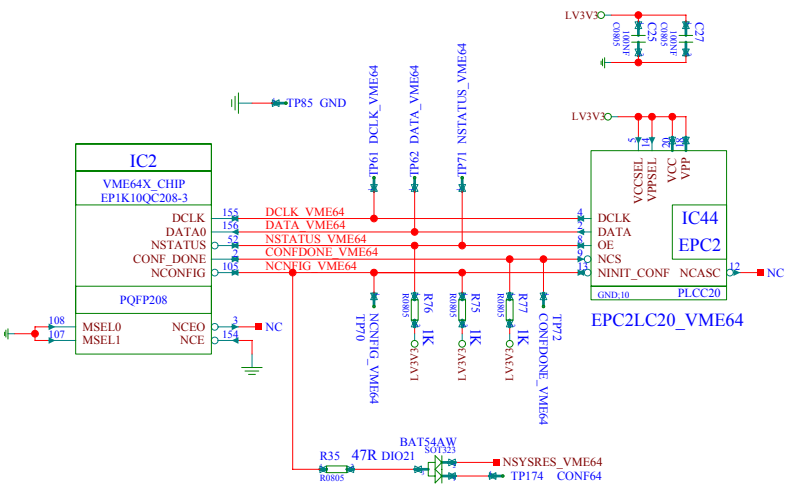


10 pins for 3.3V



6 pins for 2.5V





See configdevices.pdf:
Do not insert 1K resistor when internal pullup R are used in IC20: EPC2

FRAGEN bitte klären:

3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Referenz, HB 200803

2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Referenz, HB 200803

Dedicated inputs als GND definiert: 78 80 182 184

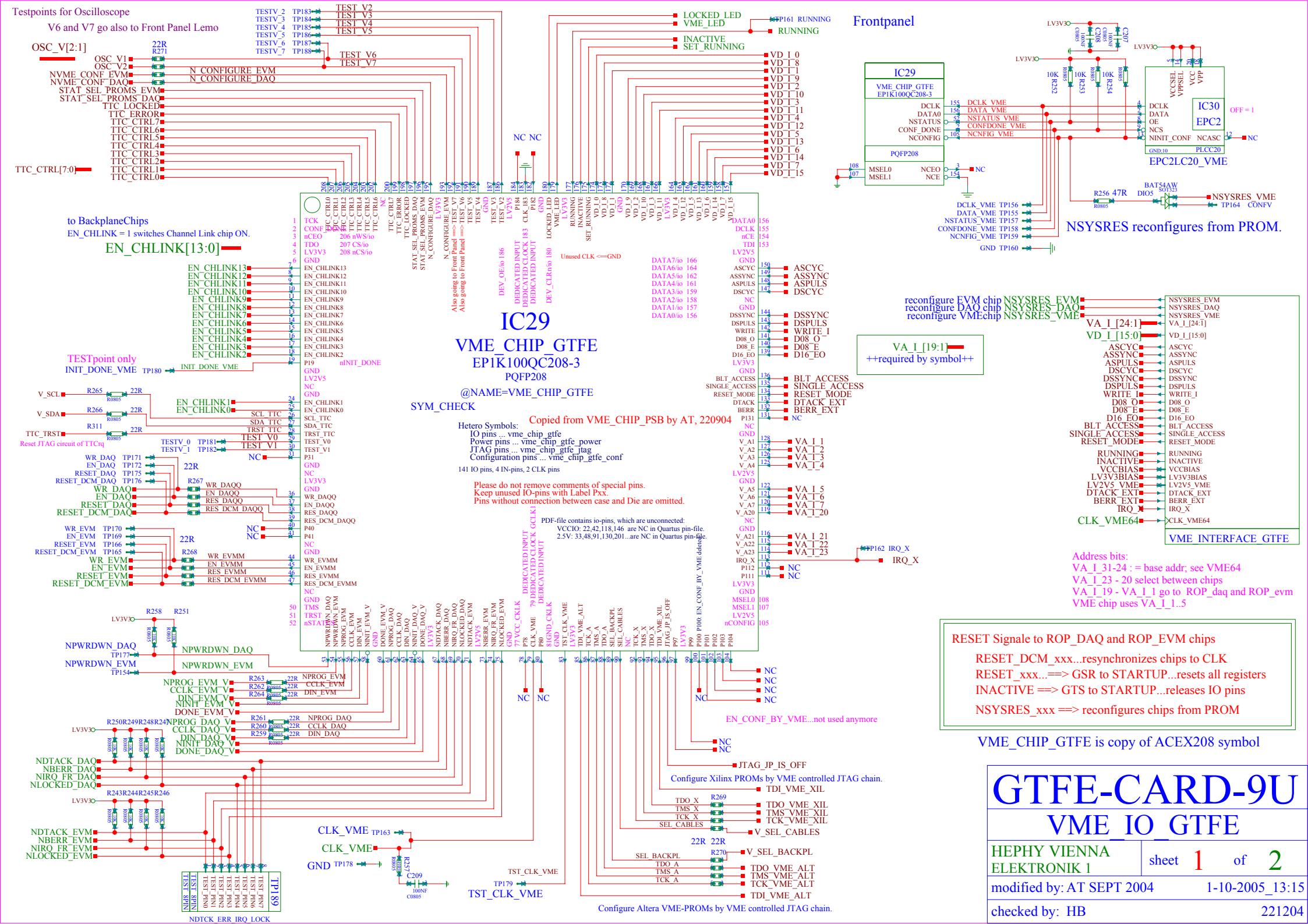
Unsused CLK pin als GND definiert: 183

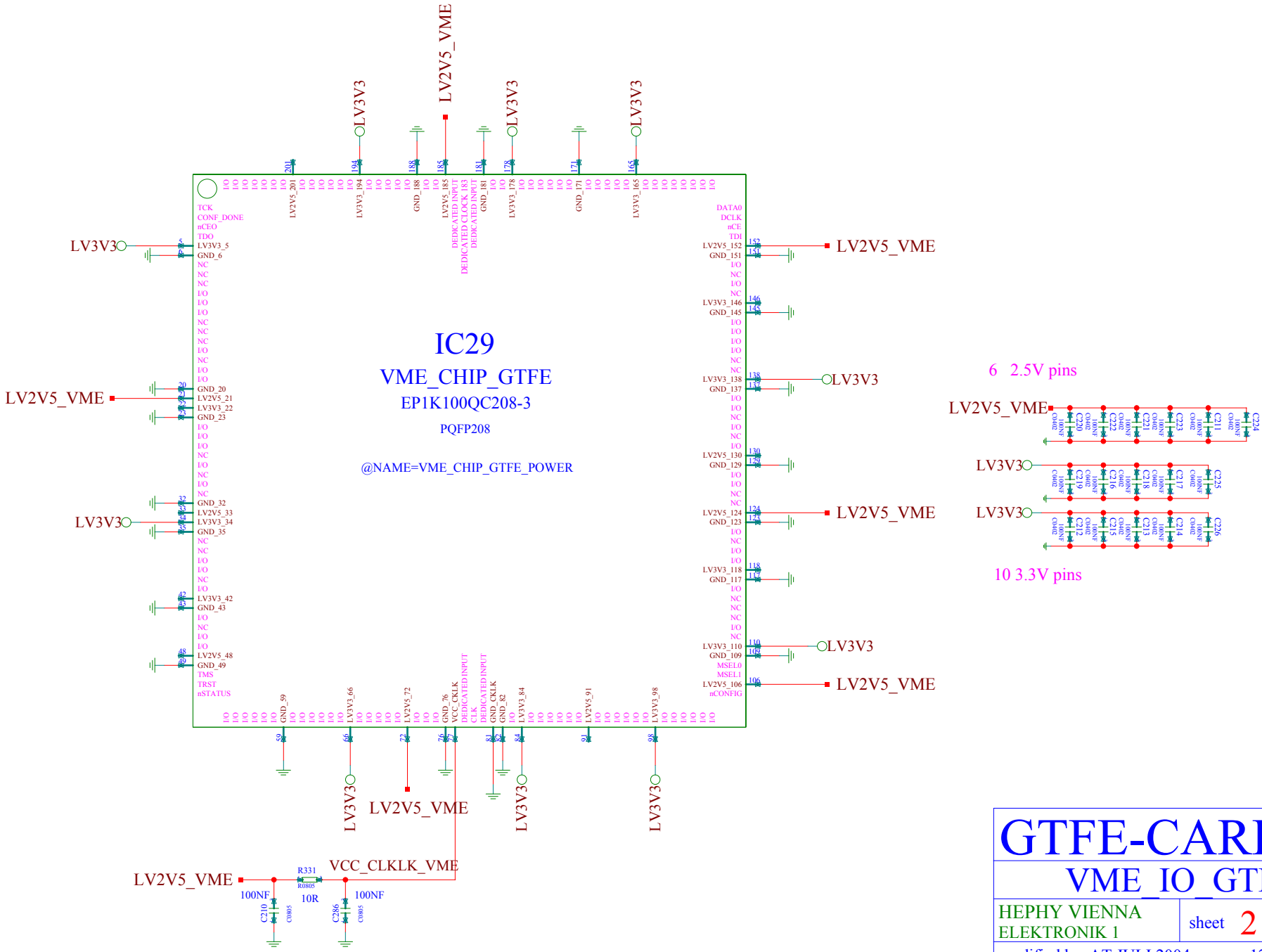
INIT_DONE used as I/O: 19

GTFE-CARD-9U

VME_INTERFACE_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3	
modified by: H. BERGAUER		12-22-2004_15:12
checked by: HB		221204

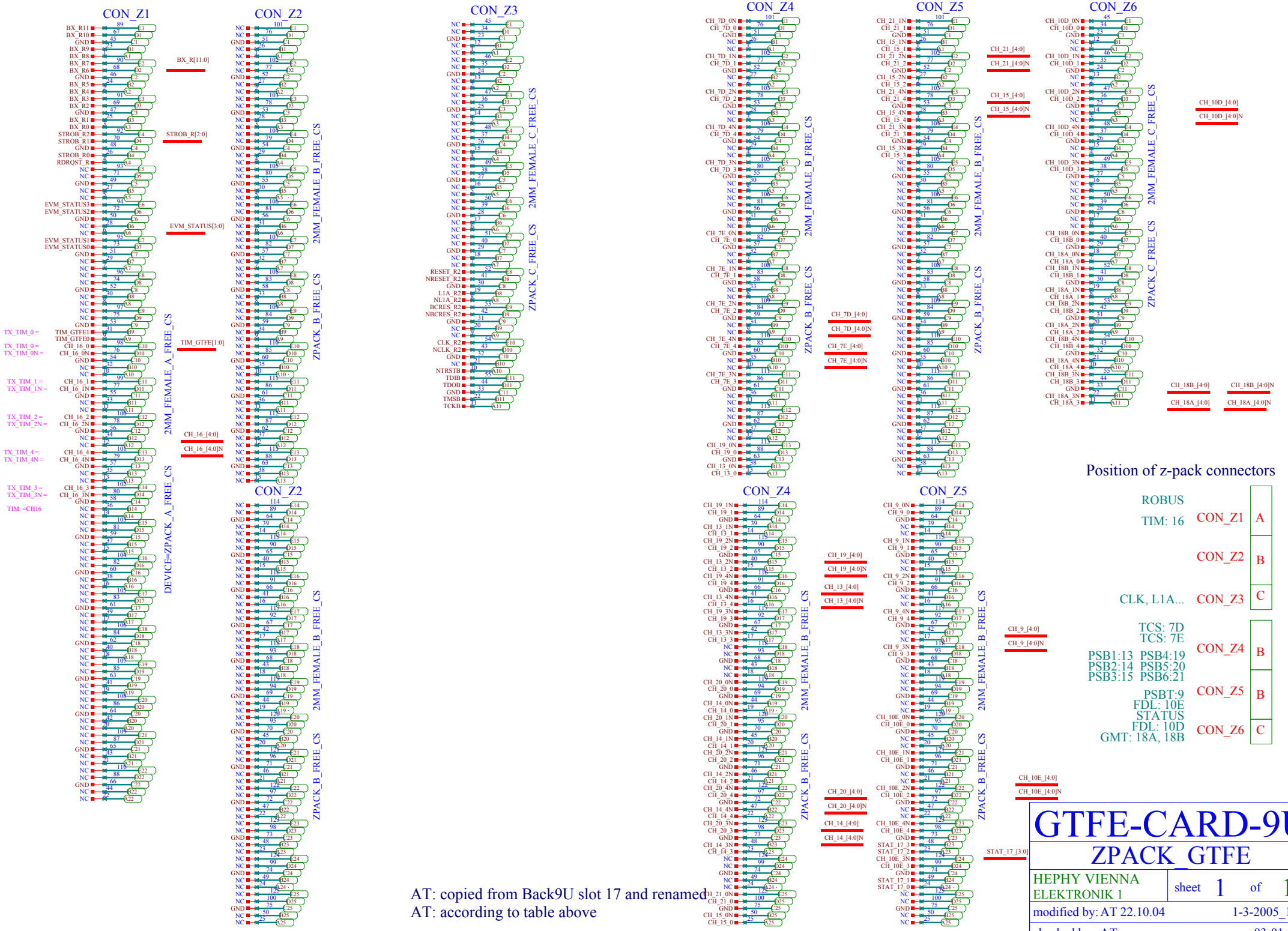

Testpoints for Oscilloscope
V6 and V7 go also to Front Panel Lemo
OSC_V[2:1]
TTC_CTRL[7:0]
N_CONFIGURE_EVM
N_CONFIGURE_DAQ
TEST_V2
TEST_V3
TEST_V4
TEST_V5
TEST_V6
TEST_V7
LOCKED_LED
VME_LED
RUNNING
INACTIVE
SET_RUNNING
Frontpanel
IC29
VME_CHIP_GTFE
EP1K100QC208-3
PQFP208
@NAME=VME_CHIP_GTFE
SYM_CHECK
Copied from VME_CHIP_PSB by AT, 220904
Hetero Symbols:
IO pins ... vme_chip_gtfe
Power pins ... vme_chip_gtfe_power
JTAG pins ... vme_chip_gtfe_jtag
Configuration pins ... vme_chip_gtfe_conf
141 IO pins, 4 IN-pins, 2 CLK pins
Please do not remove comments of special pins.
Keep unused IO-pins with Label Pxx.
Pins without connection between case and Die are omitted.
PDF-file contains io-pins, which are unconnected:
VCCIO: 22,42,118,146 are NC in Quartus pin-file.
2.5V: 33,48,91,130,201...are NC in Quartus pin-file.
to BackplaneChips
EN_CHLINK = 1 switches Channel Link chip ON.
EN_CHLINK[13:0]
TESTpoint only
INIT_DONE_VME
Reset JTAG circuit of TTCrq
EN_CONF_BY_VME...not used anymore
JTAG_JP_IS_OFF
Configure Xilinx PROMs by VME controlled JTAG chain.
Configure Altera VME-PROMs by VME controlled JTAG chain.
NSYSRES reconfigures from PROM.
reconfigure EVM chip NSYSRES_EVM
reconfigure DAQ chip NSYSRES_DAQ
reconfigure VMEchip NSYSRES_VME
VA_I_[19:1]
++required by symbol++
VME_INTERFACE_GTFE
Address bits:
VA_I_31-24 : = base addr; see VME64
VA_I_23 - 20 select between chips
VA_I_19 - VA_I_1 go to ROP_daq and ROP_evm
VME chip uses VA_I_1..5
RESET Signale to ROP_DAQ and ROP_EVM chips
RESET_DCM_xxx...resynchronizes chips to CLK
RESET_xxx...==> GSR to STARTUP...resets all registers
INACTIVE ==> GTS to STARTUP...releases IO pins
NSYSRES_xxx ==> reconfigures chips from PROM
VME_CHIP_GTFE is copy of ACEX208 symbol
NDTACK_ERR_IRQ_LOCK
GTFE-CARD-9U
VME_IO_GTFE
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 2
modified by: AT SEPT 2004
1-10-2005_13:15
checked by: HB
221204



GTFE-CARD-9U

VME_IO_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 2
modified by: AT JULI 2004	12-22-2004_15:11
checked by: HB	221204



AT: copied from Back9U slot 17 and renamed
AT: according to table above

Position of z-pack connectors

ROBUS TIM: 16	CON_Z1	A
	CON_Z2	B
CLK, L1A...	CON_Z3	C
TCS: 7D TCS: 7E PSB1:13 PSB4:19 PSB2:14 PSB5:20 PSB3:15 PSB6:21	CON_Z4	B
PSBT:9 FDL: 10E STATUS FDL: 10D GMT: 18A, 18B	CON_Z5	B
	CON_Z6	C

GTFE-CARD-9U

ZPACK_GTFE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1	
modified by: AT 22.10.04		1-3-2005_15:16
checked by: AT		03-01-2005