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CMS Internal Note

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TOTEM Trigger Signals for the Level-1 Global Trigger of CMS – Interface Specification

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??????? to be inserted ????

CMS Collaboration

Abstract

This note specifies the hardware interface between the TOTEM trigger electronics and the CMS Global Trigger. Cabling, data format and timing are described.

Version: 0.3

Version 0.1: first version

~~Version 0.2: *LVDS receiver chips on the PSB board invert the signals to get same input data for bits =0000(binary) as well as for a disconnected cable. (A.Taurok)*~~

Version 0.3: The GT expects negative voltage difference for '1' and positive voltage so that the PSB FPGA receive the same signals for '0000' data *as for a disconnected cable (A.Taurok)*

Introduction

- The TOTEM trigger electronics sends up to 16 trigger signals to the Level-1 Global Trigger to combine TOTEM and CMS data.
- Each trigger signal is the result of calculations in the Totem Trigger electronics.
- Any rate counting of Totem trigger signals will be done by the Totem Trigger electronics.
- The Global Trigger does not calculate any relation between Totem Trigger signals.
- The TOTEM Trigger bits are included into the combinatorial Algorithm logic and can be used either as accept or reject conditions.
- Totem sends the trigger bits as LVDS signals via shielded TP cables (4 pairs) and RJ45-8 connectors to the Global Trigger input board (PSB). The pin assignment is different from normal Ethernet cables, which should not be used.

Global Trigger hardware

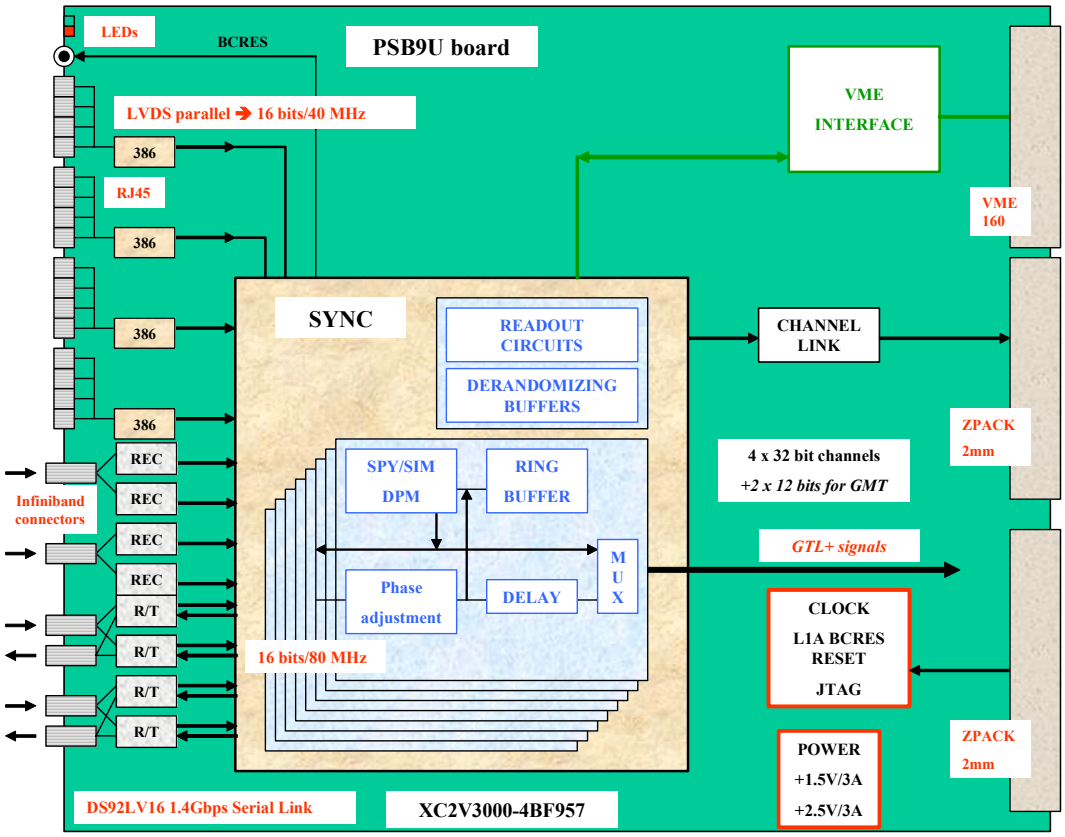

Figure 1 PSB9U input board

In the Global Trigger crate a PSB input board accepts Totem Trigger bits as LVDS signals using RJ45 (Ethernet) connectors, each cable carrying 4 trigger bits. Receiver chips convert the differential signals to LVTTL-level signals to send them to the synchronization chip (SYNC).

The PSB board expects **negative logic for differential signals**. Trigger bit =1 is sent as a negative voltage difference and bit = 0 is sent as a positive voltage difference *to get the same value for 'zero' bits (=0000 binary) as for a disconnected cable at the entry of the FPGA chip.*

As the precise arrival time of the data bits is unknown the SYNC chip first samples the input bits 4 times per bunch-crossing period (~25 ns) to find the switching point of the input data.

Phase selection and delay adjustment are done separately for each 4-bit group to consider time skew between cables and link chips. The SYNC chip also writes the input data into a RING BUFFER and in addition into a SPY memory for monitoring. The Ring Buffer runs continuously overwriting old data. If a Level-1 Accept (L1A) signal arrives at the PSB board, data are moved from the Ring Buffer into a Derandomizing Memory to be transferred later by the Readout Processor (ROP) to the readout board (GTFE).

The SYNC chip takes the sample furthest away from the switching time, delays it for a programmable time, multiplexes the data into a 80 MHz data stream and sends the data as GTL+ signals over the back-plane to the logic board (GTL). If programmed, the GTL board combines the TOTEM with Muon and Calorimeter data to generate a L1A signal for the CMS readout electronics. The Totem trigger data have to arrive in time to be combined with CMS trigger data of the same bunch crossing.

Alternatively, TOTEM Trigger bits could also be connected like Technical Trigger bits to run the TOTEM detector independently from other CMS sub-detectors as a separate DAQ-partition using the standard DAQ resources. See also the CMS-IN note about the interface for Technical Trigger signals.

Interface definition

- **4 trigger bits per cable;**
- **Up to 16 bits are foreseen for Totem Trigger signals**
- **RJ45 connectors.** See also Figure 2.
- **Cable:**

  100 Ohm, overall shield; 4 shielded twisted pairs (STP) preferred; halogen-free.

  Length - 10 to 15 m expected - depends on positions of both trigger crates.
- **Pin Assignment according to table 1 below does not agree with Ethernet standard.**
- **LVDS signal levels**

  have to be compatible to Texas Instruments SN75LVDT386 or equivalent receiver chips.

  Negative logic for differential signals:

  BIT =1 is sent as negative voltage difference.

  BIT =0 is sent as positive voltage difference.
- **Pulse shape:**

  Pulse Length =25 ns per trigger *//has to be confirmed by test measurements.*

The non-standard pin assignment has been chosen to minimize pulse shape distortions at the RJ45 connectors.

Therefore it is forbidden to connect standard Ethernet cables for data transfer.

Table 1 Non-standard Pin Assignment

PIN	BIT NR	**Uninet 5502** **Uninet flex 4P** (600 MHz)	UTP (unshielded) Cat5e cable	
1	- bit0	red	White/orange	
2	+ bit0	orange	orange	
3	- bit1	olive	White/green	
4	+ bit1	green	green	
5	- bit2	white	White blue	
6	+ bit2	blue	blue	
7	- bit3	yellow	White/brown	

8	+ bit3	brown	brown	

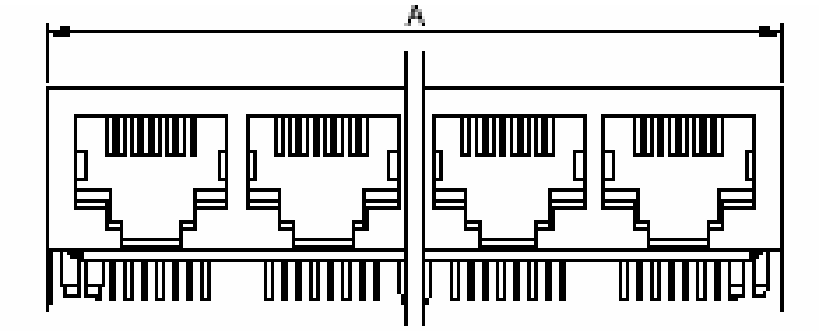

Figure 2 Shielded R45 connector on PSB board (front view) ERNI MJHS-G cat5e

Cable Examples

of Daetwyler, Switzerland: http://www.daetwyler.de

Uninet 5502 flex 4P SF/UTP

Article Number: 181 100 Orange

4 x 2 x AWG26 HF-4245-F FRNC/LSOH* 1000m/roll

Description: halogen-free, overall shield (=SF), pairs not shielded (=UTP)

Uninet flex 4P (600 MHz) S/FTP

Article Number: 177 329 Orange

4 x 2 x AWG28 HF-4232-F FRNC/LSOH* 1000m/roll

Description: halogen-free, overall shield (=SF), pairs shielded (=FTP)

Uninet 2002 flex 4P .....old type replaced by 177329 above

Article Number: 175021 blue

FR/LSOH 1000m/roll*

Description:Cat5, halogen-free, overall shield, pairs shielded (=FTP)

**) FRNC/LSOH = Flame Retardant Non Corrosive/Low Smoke Zero Halogen*

Data Sheets

- **SN75LVDS386**/388A/390, High-Speed Differential Line Receivers, SLLS394D, Sept 1999 – Revised Sept 2002, Texas Instruments
- **SN75LVDS387**/389/391, High-Speed Differential Line Drivers, SLLS362D, Sept 1999 – Revised May 2001, Texas Instruments