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CMS Internal Note

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November 22, 2004

Interface Specification for Technical Trigger Signals in the CMS Level-1 Global Trigger

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Abstract

Some CMS sub-detectors and TOTEM may send special trigger signals called “Technical Trigger Signals” for calibration, tests and other purposes to the Global Trigger. This note describes the specification of the hardware interface for these signals. .

Version 1.3

1 Global Trigger Hardware

CMS sub-detectors and TOTEM might send special trigger signals for calibration, tests and other purposes. The signals are called “Technical Trigger signals” or “Technical Triggers”. The Global Trigger can presently receive up to 32 Technical Trigger bits, but could be upgraded to 63 (64) bits. A PSB (Pipelined Synchronizing Buffer) input board accepts Technical Trigger bits as LVDS signals using RJ45 (Ethernet) connectors. Each cable will carry 4 trigger bits and 8 (16) cables can be connected to the PSB board.

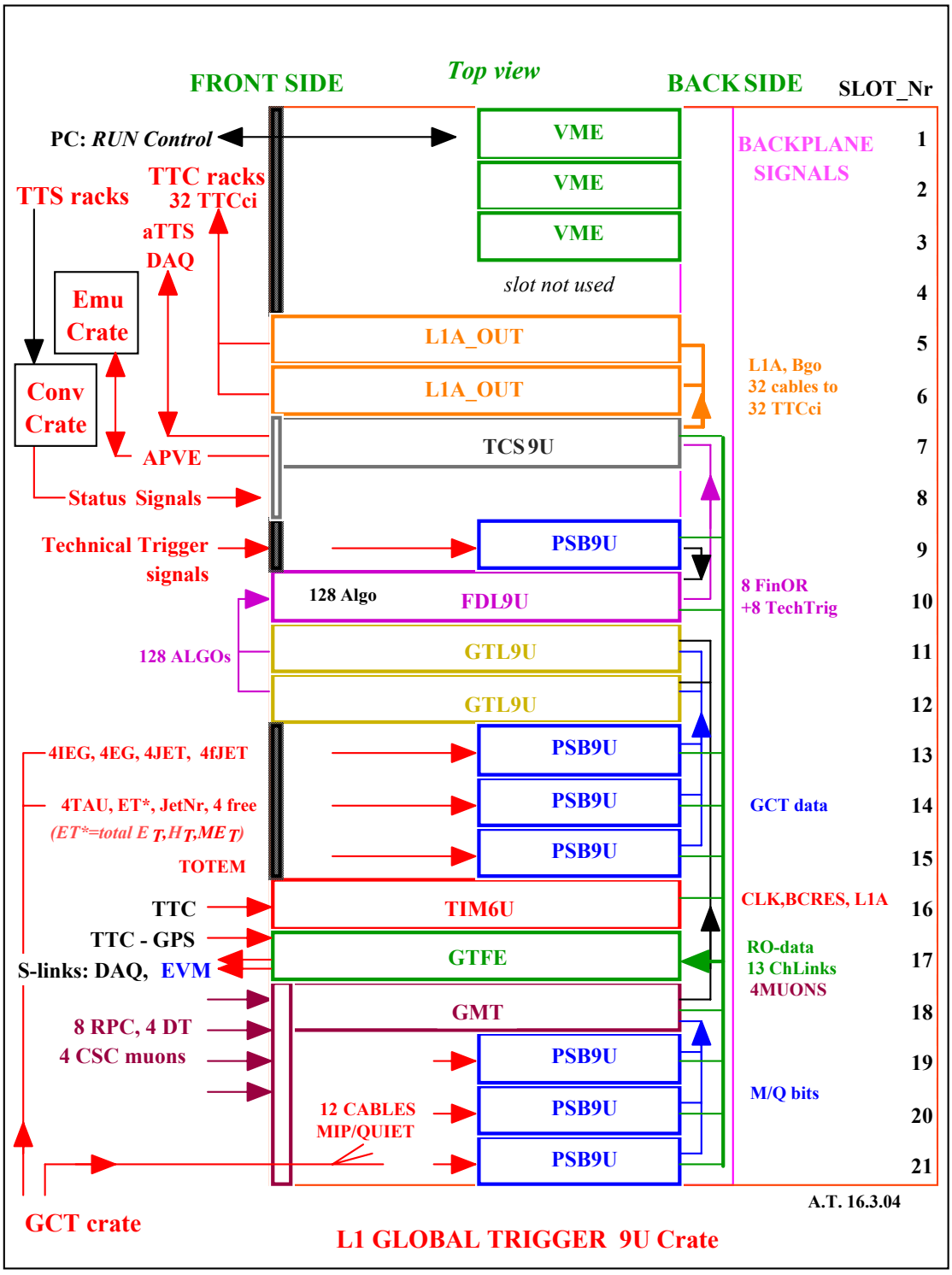


Figure 1: Global Trigger Crate

Figure 1 shows the layout of the Global Trigger crate. Slot 9 contains the board that receives technical trigger bits. A PSB input module synchronizes the technical trigger bits to the local 40 MHz clock and to the LHC orbit. The trigger bits are then forwarded to the Final Decision Logic (FDL) board. The FDL board contains a rate counter for each technical trigger bit and 32 (63) Mask bits merging them into the Final-OR signals, one for each DAQ-partition.

PSB Input Board

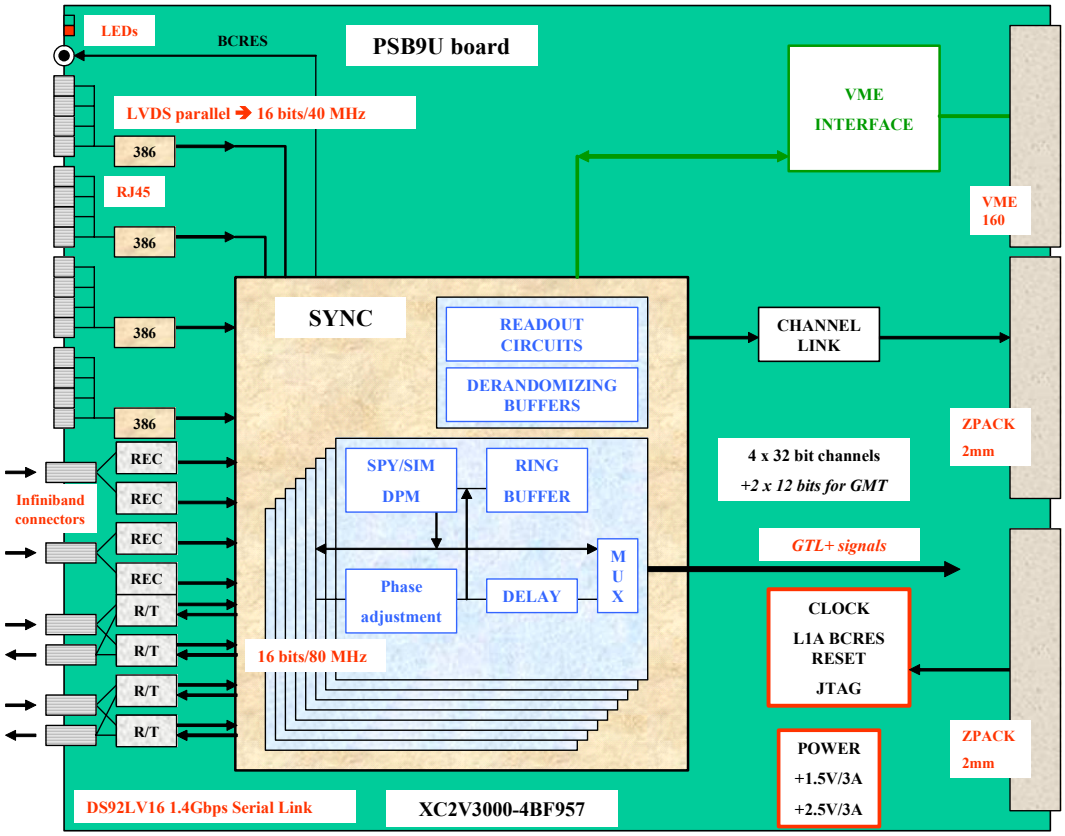


Figure 2: PSB9U input board

On the PSB board 4 Texas Instruments high-speed SN75LVDT386 differential line receiver chips convert the LVDS signals to LVTTL levels and send them to the SYNC chip. The SYNC chip senses either the **rising or falling edge** of a technical trigger bit to generate a trigger pulse with a width of 1 bunch-crossing (=BC). The pulse can be delayed optionally for up to 16 BCs. The SYNC chip also writes the input data into a RING BUFFER and in addition into a SPY memory. The RING BUFFER runs continuously, overwriting old data. A counter provides the write address for the RING BUFFER and the common BCRES signal resets the counter to synchronize the technical trigger bits to the LHC orbit. If an L1A signal arrives at the PSB board, data of the corresponding BC are moved from the Ring Buffer into a Derandomizing Memory and are later transferred by the Readout Processor (ROP) to the Global Trigger Frontend (GTFE) readout board.

During data acquisition a monitoring program can force the SPY memory to run continually and, in case of an error, to stop to check the history of the input data.

Interface definition

- **Edge sensing and synchronization to the local 40 MHz clock.**
- **4 trigger bits per cable**
- **RJ45 connectors**
- **LVDS signal levels:**

  Have to be compatible to SN75LVDT386 receiver chips from Texas Instruments.

- **Cable: 4 pairs**

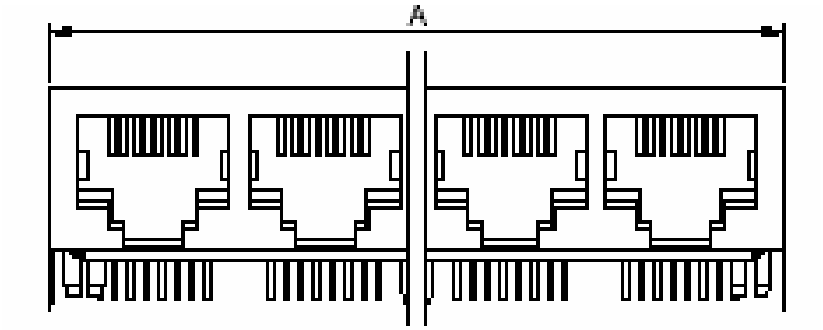
  100 Ohm, overall shield; shielded twisted pairs (STP) preferred; halogen-free.

- **Pin Assignment: does not agree with Ethernet standard. See table 1 below.**

Table 1 Non standard Pin Assignment

PIN	BIT NR	**Uninet 5502** **Uninet flex 4P** (600 MHz)	Unshielded Cat5e cable	
1	- bit0	red	white/orange	
2	+ bit0	orange	orange	
3	- bit1	olive	white/green	
4	+ bit1	green	green	
5	- bit2	white	white blue	
6	+ bit2	blue	blue	
7	- bit3	yellow	white/brown	
8	+ bit3	brown	brown	

Figure 3 Shielded R45 connector on PSB board (front view) ERNI MJHS-G cat5e



Cable Examples

by Daetwyler, Switzerland: http://www.daetwyler.de/

Uninet 5502 flex 4P SF/UTP

Article Number: 181 100 Orange

4 x 2 x AWG26 HF-4245-F FRNC/LSOH* 1000m/roll

Description: halogen-free, overall shield (=SF), pairs not shielded (=UTP)

Uninet flex 4P (600 MHz) S/FTP

Article Number: 177 329 Orange

4 x 2 x AWG28 HF-4232-F FRNC/LSOH* 1000m/roll

Description: halogen-free, overall shield (=SF), pairs shielded (=FTP)

Uninet 2002 flex 4P ..... obsolete type, replaced by 177329 above

Article Number: 175021 blue

FR/LSOH 1000m/roll*

Description: Cat5, halogen-free, overall shield, pairs shielded (=FTP)

**) FRNC/LSOH = Flame Retardant Non Corrosive/Low Smoke Zero Halogen*

Data Sheets

- **SN75LVDS386**/388A/390, High-Speed Differential Line Receivers, SLLS394D, Sept 1999 – Revised Sept 2002,, Texas Instruments
- **SN75LVDS387**/389/391, High-Speed Differential Line Drivers, SLLS362D, Sept 1999 – Revised May 2001, Texas Instruments