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Specification of the Interface Between the Regional Muon Triggers and the Global Muon Trigger

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Abstract

The CMS detector contains three independent muon systems: Drift Tubes in the barrel region, Cathode Strip Chambers in the end-cap region and Resistive Plate Chambers both in the barrel and end-cap region. All three systems participate in the Level-1 Trigger. Regional Triggers independently find muon candidates in the three muon-systems and send them to the Global Muon Trigger that combines them in order to find the best candidates in the entire detector. The interface between the Regional Muon Triggers and the Global Muon Trigger is defined in the present document.

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1 Introduction

The regional Level-1 muon triggers in CMS independently reconstruct muon candidates on the basis of trigger primitives generated in the respective muon systems [1]. Muon candidates consist of measurements of transverse momentum, sign of charge, pseudorapidity η, azimuthal angle ϕ and quality code. The Drift Tube (DT) Track Finder identifies up to four muon candidates in the barrel region ($|\eta| < 1.04$), while the Cathode Strip Chamber (CSC) Track Finder identifies up to four candidates in both end-cap regions ($|\eta| > 1.04$). The Resistive Plate Chamber (RPC) Pattern Comparator Trigger independently identifies up to four muons candidates in its barrel region ($|\eta| < 1.04$), and up to four candidates (in total) in the two end-cap regions ($|\eta| > 1.04$). All 16 muon candidates are sent to the Global Muon Trigger (GMT), which combines them in order to identify the best four over-all candidates in the detector. The present document defines the interface between the three regional Muon Triggers and the Global Muon Trigger. It includes agreements on the bit fields, their interpretation (scales), the connector types, pin assignments and the cable types as well as estimated cable lengths.

In addition to the muon candidates, the GMT receives bits from the Global Calorimeter Trigger denoting for each calorimeter region whether the energy deposit is below a certain threshold and whether it is compatible with the passage of a minimum ionizing particle. The interface between the Global Calorimeter Trigger and the Global Muon Trigger is defined in a separate document [2].

The output of the GMT is sent to the Global Trigger (GT): a separate document [3] details this interface.

It is assumed that muon trigger data are produced later than calorimeter trigger data [1, Chap 17]. The interface between the regional muon triggers and the GMT is therefore on the time critical path. Several measures are taken in order to keep latency as small as possible. Cable lengths are kept as short as possible. Racks containing the Regional Muon Triggers and the GMT are located as close as possible in the underground counting room. Muons are transferred as parallel low-voltage differential signals (LVDS) at 40 Mwords/s and go directly to the main Global Muon Trigger processing board mounted in the Global Trigger crate (1 candidate per cable). In order to feed all 16 cables to the main GMT processing board, a special input board is utilized. The Input board is mounted in parallel to the front panel of the crate and covers four slots. It is connected to the main GMT processing board using edge connectors.

2 Cables and Data Format

One cable transfers data of one muon candidate. The RPC-trigger sends 4 muon candidates from the barrel and another 4 muon candidates from the forward region. The Barrel-DT and the Forward-CSC Triggers send 4 muon candidates each.

The four muon candidates are sorted. That means that the candidates of rank 1, 2, 3, 4 are sent always on the same cables 1, 2, 3, 4. The sorting procedure is defined by the regional muon trigger systems. The muon with the highest rank is sent on channel (cable) 1, the one with the lowest rank on channel (cable) 4. If less than 4 particles are found, the channels for lower ranks are empty (see remarks on the following page).

Shielded cables and differential signals are used in order suppress errors as much as possible. Links from the DT and RPC systems contain a parity bit. Additionally the transmitted and the received data are compared by online software to monitor the reliability of the links.

Data of one muon candidate is transmitted using 34 (32) bits (differential wire pairs) as detailed in Table 1. The interpretation of the data fields is discussed in Section 3 of this document.

Table 1: Data format of the 34 cable pairs used to transmit data of one muon candidate.

Bit nr. 33 32	31 30 29 28	27 26 25 24
G G	*CLK PAR SE BC0*	*B2 B1 B0* **VCH**

<table>
<tr><td colspan="4">23 22 21 20</td><td colspan="4">19 18 17 16</td><td colspan="4">15 14 13 12</td><td colspan="4">11 10 9 8</td><td colspan="4">7 6 5 4</td><td colspan="4">3 2 1 0</td></tr>
<tr><td>CH</td><td>HF</td><td colspan="6">ETA 5..........0</td><td colspan="3">QU2,1,0</td><td colspan="5">PT 4.........0</td><td colspan="8">PHI 7......0</td></tr>
</table>

7 Control bits:

CLK = Clock
PAR = Parity bit (not sent from CSC Trigger). Even parity over bits 30..0.
SE = Synchronization Error: 1= error, 0= ok
BC0 = Bunch Crossing zero bit (= sync bit): 1= bunch crossing zero of orbit, 0= any other crossing
B2,1,0 = 3 lowest bits of bunch crossing counter
G = GND

25 Data bits:

VCH = sign of charge is valid: 1= valid, 0= not valid
CH = sign of charge: 1= negative, 0= positive
H/F = Halo bit for CSC, H/F= Fine-eta bit for DT
ETA = pseudorapidity: 6 bits (for CSC the MSB is a pseudo-sign: 1= neg. endcap, 0= pos endcap)
QU = 3 quality bits (sent inverted)
PT = transverse momentum: 5 bits (sent inverted)
PHI = azimuthal angle, 8 bits (not inverted)

Remarks:

- **P_T and QU** are sent inverted, all other bits are not inverted. This way a disconnected cable (all 1's from the LVDS receiver) indicates the lowest p_T code (empty muon) and the lowest quality code.
- **Empty candidates:** An empty candidate is a candidate with p_T code = 0 (inverted p_T-code = all 1's) and Phi code = all 1's. As a measure to make the system more robust against errors on a single bit, the receiver (GMT) checks whether both p_T and Phi indicate an empty candidate and classifies a candidate as empty if either of the conditions is met. This way an error on a single bit cannot create "fake" candidates. The remaining bits of empty candidate have to be set as follows (also see Table 2): the quality code is 0 (inverted quality = all 1's). Bits 16 to 24 are set to 0's. Bits 25 to 33 have their usual meaning.
- For a correct muon candidate, the **parity** over bits 0 to 30 is even, i.e. the number of 1's has to be even. By using this convention, a disconnected cable (all 1's from the LVDS receiver) automatically causes a parity error. Parity errors are counted by the GMT and monitored by the monitoring software. In case of a parity error the GMT optionally clears and ignores the candidate. The parity bit is generated at the senders after inverting p_T and quality bits. At the receiver (GMT) it is checked before inverting p_T and quality back.
- The CSC Trigger does not send a parity bit. The links from the CSC trigger are monitored by comparing the output data of the CSC trigger with the input data of the Global Muon Trigger in the monitoring software.
- The **synchronization error (SE) bit** indicates that the sender detected a synchronization error. Synchronization errors are counted by the GMT and monitored by the monitoring software. In case of a synchronization error the GMT optionally clears and ignores the candidate.
  The GMT optionally signals the SE condition to the Trigger Control System. The SE condition is not forwarded to the Global Trigger. It is recorded to DAQ for triggered events.
- The GMT compares the **bunch crossing counter bits (B2,1,0)** with its own internal bunch counter. In case of disagreement it internally generates a bunch counter error. Bunch counter errors are counted by the GMT and monitored by the monitoring software. In case of a bunch counter error the GMT optionally clears and ignores the candidate.
- A disconnected cable (all 1's from the LVDS receiver) indicates an empty candidate, parity error, synchronization error and (for most crossings) a bunch counter error.

Table 2: Coding of empty muons.

Bit Nr	33	32	31	30	29	28	27	26	25	24	23	22	21 .. 16	15.. 13	12 ..8	7 ..0
Field	G	G	CLK	PAR	SE	BC0	B2	B1	B0	V CH	CH	HF	ETA	QUAL	PT	PHI
Bit Code*	G	G	CLK	PAR	SE	BC0	B2	B1	B0	0	0	0	000000	000	00000	11111111
Signal sent on LVDS**	G	G	CLK	PAR	SE	BC0	B2	B1	B0	L	L	L	LLLLLL	HHH	HHHHH	HHHHHHHH

* Bit code of the field without taking into account any inversions.
** L=low, H-high, G=ground

3 Coding of Data Bits and Scales

This section deals with the coding and scales of the data bits and bit fields defined in the previous section. The scales for ϕ and p_T need to be common between the three regional triggers. The η coordinates may differ depending on the exact geometry and segmentation of the respective regional muon trigger system. Quality bits and the halo/fine-eta bit also have specific meanings for the three regional triggers.

The following coordinate system is used for the spatial coordinates ϕ and η:

- CMS is north of centre of LHC; right handed system with origin in collision point
- Horizontal x-axis pointing to centre of LHC (south),
- Vertical y-axis pointing upwards,
- Horizontal z-axis horizontal pointing to west, parallel to beam, parallel to B-field.
- $\phi = 0°$corresponding to x-axis, $\phi = 90°$ corresponding to y axis
- $\eta = 0$ in x-y plane, $\eta > 0$ for positive z-axis

The regional muon triggers determine the ϕ and η coordinates at a reference plane in the muon system. For the barrel, the reference plane is a cylinder going through the centre of the second muon station. For the endcaps, the reference plane is a plane going to the centre of the second disc of muon chambers.

3.1 Phi Scale

A common linear 8-bit ϕ scale has been agreed for all the regional muon triggers: ϕ codes range from 0 to 143, each code representing a bin of 2.5° in ϕ. Bin 0 represents a ϕ value between 0° and +2.5°, bin 1 represents a ϕ value between 2.5° deg and +5.0° deg and so forth. When converting from a more precise ϕ to the common scale, the regional triggers should avoid introducing an extra error, as the matching windows in the GMT are very small (they may be as small as only +/- 1 bin in ϕ). For example in the CSC system, the ϕ coordinate is of 5-bit resolution (2.5 deg units) inside a 60deg sector. The precise ϕ coordinate before conversion is of 7-bit resolution so that the maximum error is ¼ of a bin (0.625 deg).

Parts of the GMT logic make use of the fact that one count in the ϕ scale corresponds to exactly 2.5°. The agreed ϕ scale therefore has to remain fixed.

3.1.1 Eta Scales

The regional muon triggers send the η coordinates in their specific 6-bit scale that is given by their geometry. The GMT uses the η coordinates in the original scale for most operations. Before being sent to the Global Trigger, the η coordinates are converted to a common output scale.

In the GMT, all operations that depend on η use the η–coordinate as an input to a memory-based look-up table. It is possible to accommodate for changes in the η scales by re-programming these tables. In the following, the currently agreed η scales are detailed:

3.1.2 DT Eta Scale

The DT Track Finder uses a linear 6-bit η scale. The bin number is coded in 2’s complement notation. Bins 0 to 31 represent positive pseudorapidity values between 0 and 1.2 while bins –1 to –32 represent negative pseudorapidity values between 0 and –1.2. Additionally, the fine-eta bit indicates whether the fine assignment method based on η-layers of the DT chambers or the coarse method based on the positions of the ϕ segments was used [4]. Both the fine and the coarse η-assignment use the same scale so that the 6-bit η value may be used independent of the fine-eta bit. Optionally, the fine-eta bit may be used in the GMT in order to widen the matching windows for DT candidates with coarse η assignment or to select the better η assignment for matched DT/RPC candidates (The fine DT η assignment is more accurate than the RPC assignment, but the RPC η-assignment is in most cases more accurate than the coarse DT η-assignment.). The measurement η=0 in the coarse η assignment corresponds to a track that does not leave the central wheel (wheel zero). It is mapped to code 0 in the scale.

3.1.3 CSC Eta Scale

The CSC Track Finder uses two linear scales which are symmetric with respect to η=0. The lower 5 bits of the η code represent the bin number in a linear scale ranging from |η|=0.9 to |η|=2.5, each count representing 0.05 units in η. Bin 0 ranges from |η|=0.90 to |η|=0.95 and so forth. The most significant bit is a pseudo-sign indicating which endcap the muon is in. Code 0 represents the positive endcap (positive z and η), code 1 the negative endcap.

3.1.4 RPC Eta Scale

The RPC Pattern Comparator Triggers is segmented in regions of pseudorapidity called trigger towers. The η-assignment is given by the number of the tower containing the candidate, thereby defining a symmetric non-linear scale. The tower number ranges from -16 to 16 and is coded as a 6-bit value in 2’s complement notation. The tower boundaries and widths of the RPC trigger towers are given in Table 3.

Table 3: η-boundaries of RPC trigger towers for positive η. The RPC Trigger is symmetric with respect to η=0. Bin 0 ranges from η=-0.07 to η=0.07.

Tower nr	η-max	η-center	Bin width in η
0	0.07	0	0.14
1	0.27	0.17	0.2
2	0.44	0.355	0.17
3	0.58	0.51	0.14
4	0.72	0.65	0.14
5	0.83	0.775	0.11
6	0.93	0.88	0.1
7	1.04	0.985	0.11
8	1.14	1.09	0.1
9	1.24	1.19	0.1
10	1.36	1.3	0.12
11	1.48	1.42	0.12
12	1.61	1.545	0.13
13	1.73	1.67	0.12
14	1.85	1.79	0.12
15	1.97	1.91	0.12
16	2.1	2.035	0.13

3.2 Transverse Momentum (p_T) Scale

The regional triggers and the GMT use a common 5-bit non-linear p_T scale. The scale has to be the same in all systems for a given running condition. If running conditions require it, the scale may be changed simultaneously in all the regional triggers.

Table 4 shows the default scale, that has been agreed [1, Chap. 14] upon for the start-up of LHC: the p_T scale is defined at 90% efficiency, i.e. setting a certain trigger threshold means that the trigger is 90% efficient for muons with a real p_T equal to the selected threshold. P_T-code 0 is reserved to denote an empty muon candidate.

Table 4: Default transverse momentum (p_T) scale agreed for LHC start-up.

P_T code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Low edge of p_T bin /GeV/c	No muon	0.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	6.0	7.0	8.0	10	12	14
P_T code	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Low edge of p_T bin /GeV/c	16	18	20	25	30	35	40	45	50	60	70	80	90	100	120	140

3.3 Quality Scale

The three-bit quality code defines the quality of a muon candidate. The quality gives an indication of the accuracy of the p_T assignment and the probability of the muon candidate to be a ghost or fake candidate. The quality code is used in the GMT to calculate the sort rank and merge rank of the candidate and to classify unconfirmed candidates in certain regions of pseudorapidity as very-low-quality. Very-low-quality muons may then be excluded in certain trigger algorithms. The current definition of the quality codes is given in Table 5.

Table 5: Current meaning of quality bits of muon candidates from the DT, CSC and RPC Triggers.

Quality code	**DTBX**	**CSC**	**RPC**	**RPC**
	Stations in track	# of stations in track	$p_T \geq$ 6 GeV/c	p_T <6 GeV/c
7	1234	-	--	
6	123, 124, 12-ME13	-	--	
5	134	-	--	
4	234	-	--	
3	12, 13, 14, 1-ME13	$\geq$ 3	4 stations	4 planes
2	23, 24, 2-ME13	2, one being ME1	3 stations, missing stn. 3 or 4	-
1	34	anything else	3 stations, missing stn. 1	–
0	no track	no track	3 stations, missing stn. 2	3 planes

3.4 Sign of Charge and Charge-Valid Bit

The sign of charge bit (CH) denotes the sign of muon charge, 0 indicating a positive charge, code 1 indicating a negative charge. In some circumstances (for example straight tracks of high p_T) the regional triggers cannot determine the charge. This case is indicated by clearing the charge-valid (VCH) bit, which otherwise has to be 1. The level of certainty of the charge assignment above which the charge-valid bit is set has to be common among all the regional triggers sending a charge-valid bit. The GMT may use the valid-charge bit in order to select the better charge assignment for matched candidates. The GMT also forwards the charge-valid information to the Global Trigger.

3.5 Halo / Fine-Eta Bit

For DT candidates this bit is used to indicate the type of η assignment (see Section 3.1.2). The fine assignment method is indicated by a code of 1 while the coarse assignment method is indicated by a code of 0. For CSC candidates the bit indicates whether the candidate was identified as a beam halo muon (1) or a normal muon coming from the interaction region (0). For RPC candidates the bit is currently not used.

4 Pin Assignment

At the GMT input, 68-pin SCSI-3 connectors are used for the muon candidate cables. The pin assignment has been chosen so that each differential pair in the cable transfers the LVDS signals of one bit (Table 6). The pin and wire numbers on the footprints of SCSI-3 right angle connectors are shown in Figure 1.

Table 6: Pin assignment on a 68-pin SCSI-3 connector.

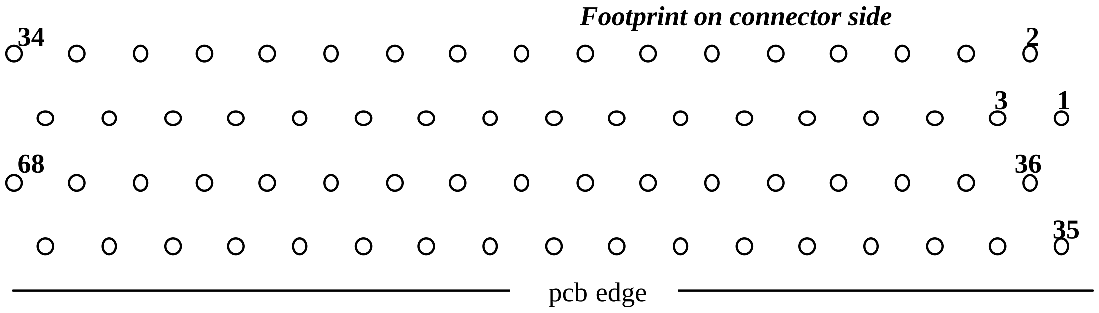
BIT	Pin	Signal		Pin	Signal	
0	1	+	Phi_0	35	-	Phi_0
1	2	+	Phi_1	36	-	Phi_1
2	3	+	Phi_2	37	-	Phi_2
3	4	+	Phi_3	38	-	Phi_3
4	5	+	Phi_4	39	-	Phi_4
5	6	+	Phi_5	40	-	Phi_5
6	7	+	Phi_6	41	-	Phi_6
7	8	+	Phi_7	42	-	Phi_7
8	9	+	Pt_0	43	-	Pt_0
9	10	+	Pt_1	44	-	Pt_1
10	11	+	Pt_2	45	-	Pt_2
11	12	+	Pt_3	46	-	Pt_3
12	13	+	Pt_4	47	-	Pt_4
13	14	+	Qu_0	48	-	Qu_0
14	15	+	Qu_1	49	-	Qu_1
15	16	+	Qu_2	50	-	Qu_2
16	17	+	Eta_0	51	-	Eta_0
17	18	+	Eta_1	52	-	Eta_1
18	19	+	Eta_2	53	-	Eta_2
19	20	+	Eta_3	54	-	Eta_3
20	21	+	Eta_4	55	-	Eta_4
21	22	+	Eta_5	56	-	Eta_5
22	23	+	Halo/Fine-eta	57	-	Halo/Fine-eta
23	24	+	Charge	58	-	Charge
24	25	+	VCH	59	-	VCH
25	26	+	Bx0	60	-	Bx0
26	27	+	Bx1	61	-	Bx1
27	28	+	Bx2	62	-	Bx2
28	29	+	BC0	63	-	BC0
29	30	+	SE	64	-	SE
30	31	+	Parity	65	-	Parity
31	32	+	CLK	66	-	CLK
32	33	+	GND	67	-	GND
33	34	+	GND	68	-	GND

4.1 Connector types

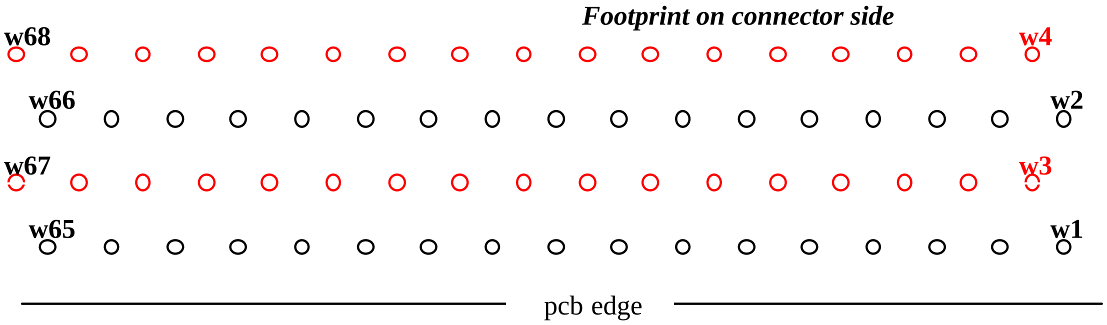
It is foreseen to use connectors of type AMP/Tyco 787171-7 [5]. The footprint of the foreseen connectors is shown in Figure 1. If cables with the foreseen connector type cannot be procured then a different type of connectors with the same footprint will be used.

- **SCSI-3 connector: receptable, right angle**

Manufacturer‘s pin numbers



Wire numbers of a connected flat cable



Wire pairs: w1-w2 = pin 35 - 1,   w3-w4 = pin 36 - 2, ...

Figure 1: Footprints of SCSI-3 connector, right angle.

5 Estimated cable lengths and latency

Cable lengths and latency have been estimated according to version 4.9 of the CMS rack layout [6]. For cables a time delay of 1.6ns/ft = about 5ns/m was assumed. The locations of the regional trigger sorters and the GMT as well as the types of LVDS drivers/receivers and their delays are detailed in Table 7. The contributions to the link latencies and total link latencies of the links from the regional trigger sorters to the GMT are summarized in Table 8.

Table 7: Interface information.

	LVDS driver / receiver	**Delay LVDS driver / receiver**	**Location of crate**	**Position of connectors front / back side of crate**
GMT	SN75LVDT386	4 ns*	S1E04: GT crate	front
CSC	SN75LVDS387	2.9 ns**	S1D05	back
DT	SN75LVDS387	2.9 ns**	S1D02	front
RPC	SN75LVDS387	2.9 ns**	S1F06	back

Table 8: Delay of links from Muon Sorters to GMT.

	RACK location	**Sorter FPGA t_{cko}^{++}/ ns**	**Sorter PCB delay / ns**	**Sorter LVDS driver**	**Cable Length & Delay**	**GMT LVDS receiver delay / ns**	**GMT PCB delay / ns**	**GMT FPGA t_{setup} / ns**	**Total delay/ ns**	**Total delay / BC**
CSC	S1D05	3.5***	1.5^{+}	2.9**	9 m = 45 ns	4 ns	1.5 ns	2.0***	60.4	3
DT	S1D02	3.5***	1.5^{+}	2.9**	10 m = 50 ns	4 ns	1.5 ns	2.0***	65.4	3
RPC	S1F06	3.5***	1.5^{+}	2.9**	9 m = 45 ns	4 ns	1.5 ns	2.0***	60.4	3

*) SN75LVDT386: differential input threshold: +/- 100mV

➔Allowed attenuation: 100/240=> -7,6 dB...min for 50 MHz (=worst case for driver output)

**) LVDS driver SN75LVDS387 assumed: differential output: 240-300-460 mV

***) Xilinx Virtex-II speed grade-4 assumed

+) about 20 cm wire length on PCB assumed as worst case.

++) Delay from clock to output

The estimation of the cable lengths is based on the assumptions given below and on version 4.9 of the CMS rack layout. This first approximation may still be subject to changes for example due to changes in the rack layout. In order to shorten the cable paths, cables may alternatively be routed through additional cable trays installed above the racks.

General Assumptions:

Racks 90x60 cm, crate depth = 80 cm, cable tray= 50 cm below the floor

Holes below the racks in the middle of the base: ➔ 45 cm from hole to front- or back-side

Distances: racks D to E (front to front) = 150 cm, racks E to F (back to back) =100 cm

CSC – GMT cable length estimation: 250 + 125 + 240 + 250 = 865 cm ➔ **9 m cable**
(actual cables may be shorter due to possible routing in trays above the racks)

1.) Vertical: CSC-Sorter crate down to cable tray below the floor …250 cm
    150cm Sorter crate to floor + 50 cm back side to CSC-hole + 50 cm floor to cable tray
2.) Horizontal: between S1D05 and S1D04 … 125 cm
3.) Horizontal between S1D04 (CSC Sorter) and S1E04 (GT) holes ...240 cm
    45 cm from hole to CSC-back side
    150 cm CSC-back side to GT-back side
    45 cm from GT-back side to hole
4.) Vertical from cable tray below the floor to the GMT/GT crate in S1E4 rack about …250 cm
    50 cm cable tray up to floor level
    50 cm GT-hole to front side
    150 cm floor to GMT boards

DT – GMT cable length estimation: 250 + 250 + 240 + 250 = 990 cm ➔ **10 m cable**

1.) Vertical: DT-Sorter crate down to cable tray below the floor …250 cm
    150cm Sorter crate to floor + 50 cm back side to DT-hole + 50 cm floor to cable tray
2.) Horizontal between S1D02 (DT Sorter) and S1D04… 250 cm
3.) Horizontal between S1D04 and S1E04 (GT) holes ... 240 cm
    45 cm from hole to DT-back side
    150 cm DT-back side to GT-back side
    45 cm from GT-back side to hole
4.) Vertical from cable tray below the floor to the GMT/GT crate in S1E4 rack about …250 cm
    50 cm cable tray up to floor level
    50 cm GT-hole to front side
    150 cm floor to GMT boards

RPC - GMT cable length estimation: 170 + 250 + 190 + 250 = 860 cm ➔ **9 m cable**

1.) S1F6-S1F5-S1F4 (via holes between racks) 50cm + 2*60cm = 170cm
2.) Vertical: RPC-Sorter crate down to cable tray below the floor …250 cm
    150cm Sorter crate to floor + 50 cm back side to RPC-hole + 50 cm floor to cable tray
3.) Horizontal between S1F04 and S1E04 (GT) holes …190 cm
    45 cm from hole to RPC-front side
    100 cm RPC-front side to GT–front side
    45 cm from GT-front side to hole
4.) Vertical from cable tray below the floor to the GMT/GT crate in S1E4 rack about …250 cm
    50 cm cable tray up to floor level
    50 cm GT-hole to front side
    150 cm floor to GMT boards

5.1 Halogen-Free Cables for Parallel Transfer

To transfer 40 MHz LVDS data over less than 15m a skew between pairs of 0.035 ns / ft = 1.6 ns/15m or slightly more can be accepted and attenuation should be below 0.5 dB/m=7.5 dB/15m. The low attenuation requires 28AWG, 50mil cables. In line with these requirements, 68 pin halogen-free SCSI-3 cables manufactured by Technical Cable Concepts, Inc [7] will be used as for the data links (the same type as used between the Regional Calorimeter and GCT crates).

In case of difficulties in the procurement of the above cables, cables from an alternative manufacturer may be used:

Madison company

68SDK00060 (Electrical data probably as for SCSI-2 cables 68SDK00057 until –59)

34 pairs, AWG 28 (7/36 TC) Diameter=0.490” [12.45mm], Z_diff= 123, Zo=79, C= 16.0 pF mutual , C= 25.0 pF single ended

68KDK00064 (Electrical data probably as for SCSI-3 cables 68KDK00043 until –45)

34 pairs, AWG 28 (7/36 TC) Diameter=0.490” [12.45mm], Z_diff= 132, Zo=85, C= 12.0 pF mutual , C= 20.0 pF single ended

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[6] CMS Rack Layout in USC55 (version 4.9), http://cmsdoc.cern.ch/~wsmith/USC55_racks_v49.html

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