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2006 Interface Specification for the CMS Level-1 Regional Calorimeter Trigger to Calorimeter Global Trigger

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Abstract

An update to the interface between the CMS Level-1 Regional Calorimeter Trigger electronics crates and the Global Calorimeter Trigger (GCT) is specified. The cabling, data format, and timing are described. It includes the provision that the GCT will include the functionality of the Cluster Crate and supersedes documents CMS IN/2001-017 and CMS IN/2004-009, and includes changes due to the revision of the GCT.

1 Interface Specification

The general design and function of the Level-1 Regional Calorimeter Trigger (RCT) has been described in several references [1][2][3]. The design of the Level 1 Global Calorimeter Trigger (GCT) as described elsewhere [3][4][5][6] has changed. The function remains the same, but the hardware has been revised [7]. This document respecifies the cabling, data, and electrical interface between the RCT and the GCT and supersedes the CMS Internal Notes 2001/017 and 2004/009 [8][9].

The RCT is located a floor above the main GCT rack in the CMS underground counting room in USC55 [10]. It will consist of 18 regional crates (9U in height) and a RCT central clock distribution crate (6U). These 19 crates will be housed in 10 LHC racks. The GCT's 66 Source Cards will be located in six 6U crates in the RCT racks, to convert parallel Negative-ECL (NECL) to serial optical data (Figure 1). The fibers will be routed through the floor to the GCT rack. The data transfer between the Regional Calorimeter Trigger's 18 Jet/Summary Cards (one per regional crate) and the GCT will take place on 108 twisted-pair cables of length not greater than 20 meters[1], at a transmission rate of 80 MHz using differential NECL signals. This configuration provides two 12.5 ns data phases for each 25 ns crossing period.

2 Inter-crate connections

The connectors on the RCT JSC are 68-pin SCSI-2 with clip type attachment, female on the Jet/Summary Card (AMP part number 787362-7 or 787170-7 if the previous one is unavailable) and male on the connecting cable. They were chosen for their high density and physical robustness. The GCT Source Card will use a VHDCI (68-pin) socket on the front panel and the complementary connector on the cable. The 68-conductor cable is a universal SCSI cable from Madison Cable, with a 30 AWG solid-core twisted-pair cable with a halogen-free jacket [11]. The cable shielding at the GCT will couple the connector shields to the GCT chassis ground via surface mount components. On the transmitting end, at the RCT, the cable shield will be directly connected to the logic ground. The pin out numbering for each connector at the Jet/Summary Card (JSC) is as shown in Figure 2. A pair of pins is pins 1 and 2, 3 and 4, etc. (exact pin assignments are specified later in the tables). A similar version of this cable was used in an early GCT integration test and performed according to specification [12].

Six 68-conductor cables per regional crate JSC will carry the isolated and non-isolated electron information, Minimum Ionizing Particle (MIP) bits, quiet bits, τ-bits, and region sums to the GCT. This results in 108 cables from the 18 RCT crates' JSCs to the GCT.

Table 1 lists the crate-by-crate η,ϕ coverage for the electron/photon and regional sum data. Tables 2 and 3 list the electron data transported from the 18 regional crates to the GCT. Each table lists the data bits, pin-by-pin, transported from each JSC to the GCT. In each case the <n> notation refers to the n^{th} bit of the particular quantity. Table 4 defines the position bits as given in Tables 2 and 3. Tables 5, 6, 7 and 8 list the Regional Sum data transported from the JSCs to the GCT by card, region, connector pins, and cycle.

3 Quantity Descriptions

3.1 Electron Cables

The isolated and non-isolated electron 6-bit E_T values sent from the 18 regional crates' JSCs to the GCT in Tables 2 and 3 will be in a non-linear scale, but they will be unsigned and monotonically increasing, with a programmable LSB (e.g. 0.5 GeV). The values of E_T will be set by a lookup table, and will depend on the values of the thresholds set at the Global Trigger. Four bits of positional information will be sent as well, using the region position encoding given in Table 4, identical for each crate of the RCT. The top four e/γ candidates will be delivered in no predetermined order, due to the algorithm implemented in the Sort ASIC.

The 14 MIP bits (two for each region covered by a receiver card) will be sent in cycle 0 over the two electron cables from the JSC. The MIP bit is set to ON (logic one) for a tower with E_T consistent with passage of a minimum ionizing particle through it and ORed for each 4 tower by 4 tower (4x4) region. The isolated electron

[1] The cable and path will be shorter than this.

cable will carry the bits for receiver cards 0-3, and the non-isolated electron cable will carry the bits for receiver cards 4-6. The Quiet bits (two per receiver card) will be sent over the isolated and non-isolated cable in the same manner as the MIP bits, but on cycle 1. Quiet bits are determined by thresholding 4x4 energy sums received from the Receiver cards on the JSC. When E_T<Threshold the Quiet Bit will be set to logic one (high) for a region, and logic zero (low) when E_T>Threshold.

In each table, the *Bunch Crossing Zero* (BC0), a half-cycle ECL signal, will equal one when the data simultaneously accompanying it corresponds to the data from LHC bunch crossing zero. For all other bunch crossings, BC0=0. It is synchronized with BC0 from the TTC but offset by a fixed phase. It will be on the first cycle (cycle 0) for all of the electron, jet, and E_T sum cables. On the second cycle (cycle 1), the ECL signal will be one. This pattern is used as a check of RCT to GCT alignment. This results in a 0,1 pattern for all bunch crossings *except* for BC0 which will have a 1,1 pattern. The BC0 on the electron cables will line up with the electron data and *not* the MIP/Quiet bits.

3.2 Region Sum Cables

Individual Region Sums will be sent from the RCT's 18 regional crates' JSCs to the GCT [5]. The data sent are shown in Tables 5, 6, 7, and 8 (corresponding to cables 5, 6, 4, and 3). Additionally, a map showing the E_T regions and approximate borders defined by the cables for each regional crate is shown in Figure 3. Data transfer will take place on seventy-two 68 conductor SCSI cables (same brand and type as above) at a rate of 80 MHz using differential ECL signals from the 18 JSCs to the GCT's input modules. Figure 2 shows how pins are defined for these cables.

For each of 18 RCT Regional Crates, 10 bits E_T, an E_T overflow bit, and a τ bit (logic high - one - if the towers hit in a region above a given threshold form specific patterns) further defined in reference [13]) are sent for 14 central regions (each one is 4x4 trigger towers - 2 per receiver card) to the GCT input modules. In addition, 8 bits E_T, and a quality bit used for describing the energy profile in the six segments of the HF tower, are sent for eight forward regions of the HF. These 168 bits require four 68-conductor cables from each of 18 JSCs to the GCT, for 72 in total. The configurations of these cables are shown in Tables 5, 6, 7, and 8. The approximate regional borders defined by the regional E_T assignment to the cables are shown in Figure 3. Pin assignments given in the tables are shown in Figure 2. These E_T values will be linear, unsigned with a programmable LSB (e.g. 1.0 GeV). Each cable will also carry a '1' and a BC0 in the same way as for the electron cables, but aligned with the correct crossing for the region sums.

In total, seventy-two cables will carry regional E_T values and relevant bits from the 18 RCT regional crates' JSCs to the GCT. Including the 36 electron cables coming from the 18 regional crates' JSCs described previously, sending these cables from the regional crates to the GCT will result in 108 cables in total .

4 Timing

Within a single cable, the relative phases of individual bits will be kept within ±1 ns at the transmitting end. Over the entire RCT time variations between cables of up to ±4 ns are possible.

Latency is measured from the input to the RCT at the Receiver Mezzanine Card VGA connector to the output at the Jet/Summary Card SCSI connector. All electron information will be aligned to the same bunch crossing, with a latency of 20 crossings. The 4x4 region data will arrive with a latency of 11 crossings and then transferred to the GCT. MIP and Quiet bits will arrive with a latency of 11.5 crossings and will arrive offset with respect to the electron information (earlier by 8.5 crossings) and any delay will be handled by the Global Muon Trigger and not the RCT or GCT [5].

5 Termination Scheme

Each individual output signal is biased on the JSC to -5V through an approximately 300 Ω resistor. Each differential signal pair anticipates driving a twisted pair with a characteristic impedance in the 100 to 120 Ohm range, within a cable bundle of about 20m in length. The 300 Ohm to -5V bias should be sufficient to allow the ECL output transistors to conduct at both logic levels with cable attached. Assuming a far-end termination between signal pairs to match the impedance of cable, and a high DC common-mode input impedance at the GCT end, the net DC common-mode current flow between the RCT and GCT subsystems should be very small. Differential currents will flow on the cable, being both sourced and sunk at the RCT end.

6 Error Detection

There will be no error detection bits. However, offline and online running of test pattern generation, transmission, and decoding will be used. Provisions for fast and efficient offline (but synchronized) testing will be made in both the regional and global calorimeter triggers. During timing setup, i.e. synchronization of the RCT and the GCT, test patterns will be sent from the RCT to GCT in lieu of normal trigger data.

References

[1] J. Lackey, et al., *CMS Level 1 Calorimeter Trigger Design,* CMS TN/94-284

[2] J. Lackey, et al., *CMS Level 1 Calorimeter Regional Trigger Design,* CMS Note/98-074, 1 December 1998.

[3] CMS, *The TRIDAS Project Technical Design Report, Volume 1: The Trigger Systems*, CERN/LHCC 2000-38, CMS TDR 6.1.

[4] G. Heath, Et al., *CMS Global Calorimeter Trigger Conceptual Design,* CMS TN/95-049, 11 May 1995.

[5] A. Mass, et al., *The Global Calorimeter Trigger for CMS,* Proceeding of the LEB '98 Meeting (Rome).
D. M. Newbold, et al. *An FPGA-Based Implementation of the CMS Global Calorimeter Trigger*, Proceedings of the LEB '00 Meeting (Crakow).
J. Brooke, et al. *Hardware, Firmware and Software Implementation of an FPGA-based trigger system for CMS*, Proceedings of the LECC 2003 Meeting (Amsterdam).

[6] J. J. Brooke, D. G. Cussans, R Frazier, G. P. Heath, D. M. Newbold, S Galagedera, et al., *Design and Implementation of the Global Calorimeter Trigger for CMS,* Proceedings of the 10th Workshop on Electronics for the LHC Experiments (Boston) and *Global Calorimeter Trigger Technical Documentation*, obsolete.

[7] C. Foudas, M. Hansen, G. Iles, J. Jones, A. Rose, M. Stettler, *Proposal for an alternative design of the Global Calorimeter Trigger Version II,* February 2006, available at http://www.hep.ph.ic.ac.uk/~foudas/GCT/GCT-Proposal-V9.pdf.

[8] J. Brooke, et al. CMS Calorimeter Level 1 Regional Trigger to Calorimeter Global Trigger Interface, CMS IN/01-017, 19 April 2001.

[9] J. Brooke, et al. Updated Interface Specification for the CMS Level-1 Regional Calorimeter Trigger to Calorimeter Global Trigger, CMS IN/04-009, 23 March 2004.

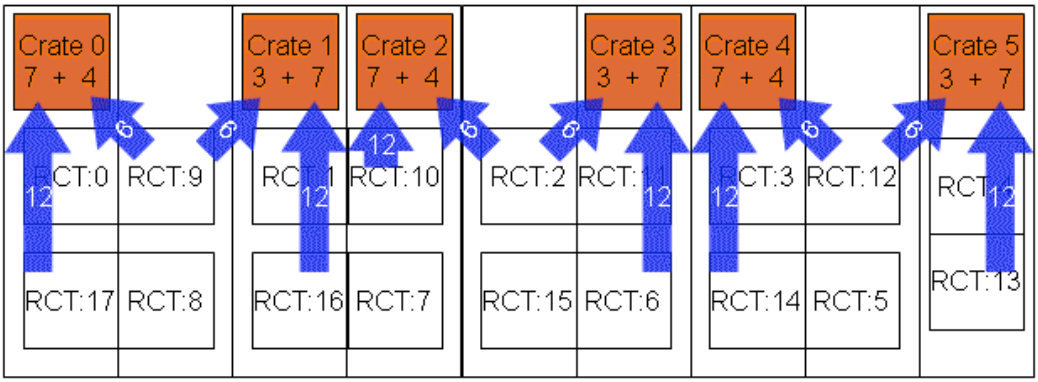
[10] http://cmsdoc.cern.ch/~wsmith/USC55_racks.html

[11] D. Newbold, November 2003 CPT Week, http://cmsdoc.cern.ch/%7ewsmith/Agenda1103.html

[12] J. Brooke, et al. Tests of RCT to GCT Link, 2003, in preparation.

[13] P. Chumney et al., *Updated Regional Calorimeter Trigger Baseline Thresholds and Rates for a LHC Luminosity of 2×1033 cm^{-2} s^{-1},* CMS IN/02-019, 29 March 2002. Dasu et al., *CMS Level-1 Regional Calorimeter Trigger Tau Jet Trigger*, in preparation.

Figure 1: Position of the GCT Source Card crates with respect to the RCT crates and the assignment of RCT crates to Source Card crates.



Crate Number	Number of RCT crate pairs	Number of RCT cables	Number of source cards	Number of USB hubs	Number of hub cards	TTCoc cards	Spare slots	Current (A)
0	1 1/2	18	11	2	1	1	8	61
1	1 1/2	18	11	2	1	1	8	61
2	1 1/2	18	11	2	1	1	8	61
3	1 1/2	18	11	2	1	1	8	61
4	1 1/2	18	11	2	1	1	8	61
5	1 1/2	18	11	2	1	1	8	61
Total	9	108	66	12	6	6	48	366

Source card (@5A) and hubs only

Current for TTCoc unknown

Figure 2: Diagram showing the pin numbering for a 68-pin connector. This represents the female connector as seen from the front of the Jet/Summary card. A pair of pins on the cables is defined in tables 2, 3, 5, 6, 7, and 8.

Connector Mating Face: Jet/Summary Front

Table 1: The η,ϕ coverage of each of the RCT crates for the 36 isolated and non-isolated electron cables (one of each type per crate) and 72 region sum cables (four per crate).

Regional Crate Number	ϕ Coverage	η Coverage e/γ	η Coverage Region Sums
0	+90° to +50°	–2.5 to 0.0	–5 to 0.0
1	+50° to +10°	–2.5 to 0.0	–5 to 0.0
2	+10° to –30°	–2.5 to 0.0	–5 to 0.0
3	–30° to –70°	–2.5 to 0.0	–5 to 0.0
4	–70° to –110°	–2.5 to 0.0	–5 to 0.0
5	–110° to –150°	–2.5 to 0.0	–5 to 0.0
6	–150° to +170°	–2.5 to 0.0	–5 to 0.0
7	+170° to +130°	–2.5 to 0.0	–5 to 0.0
8	+130° to +90°	–2.5 to 0.0	–5 to 0.0
9	+90° to +50°	0.0 to 2.5	0.0 to +5
10	+50° to +10°	0.0 to 2.5	0.0 to +5
11	+10° to –30°	0.0 to 2.5	0.0 to +5
12	–30° to –70°	0.0 to 2.5	0.0 to +5
13	–70° to –110°	0.0 to 2.5	0.0 to +5
14	–110° to –150°	0.0 to 2.5	0.0 to +5
15	–150° to +170°	0.0 to 2.5	0.0 to +5
16	+170° to +130°	0.0 to 2.5	0.0 to +5
17	+130° to +90°	0.0 to 2.5	0.0 to +5

Table 2: All of the isolated electron cables have the same configuration. Each cable carries four isolated electrons. The isolated electron data channels require one cable from each regional crate to the GCT for a total of 18 cables. In addition, the MIP bits and Quiet bits for receiver cards 0 to 3 will be carried on the isolated electron cables. The '1' and BC0 are described in the text. Unused pins are tied to ground. The first wire of the wire pair is the ordinary NECL signal and the second wire is the complement.

All isolated electron cables		
Wire Pair	Cycle 0	Cycle 1
1,2	Electron 0 rank <0> LSB	Electron 2 rank <0> LSB
3,4	Electron 0 rank <1>	Electron 2 rank <1>
5,6	Electron 0 rank <2>	Electron 2 rank <2>
7,8	Electron 0 rank <3>	Electron 2 rank <3>
9,10	Electron 0 rank <4>	Electron 2 rank <4>
11,12	Electron 0 rank <5> MSB	Electron 2 rank <5> MSB
13,14	Electron 0 Region ID <0>	Electron 2 Region ID <0>
15,16	Electron 0 Card ID <0>	Electron 2 Card ID <0>
17,18	Electron 0 Card ID <1>	Electron 2 Card ID <1>
19,20	Electron 0 Card ID <2>	Electron 2 Card ID <2>
21,22	Unused	
23,24	Electron 1 rank <0> LSB	Electron 3 rank <0> LSB
25.26	Electron 1 rank <1>	Electron 3 rank <1>
27,28	Electron 1 rank <2>	Electron 3 rank <2>
29,30	Electron 1 rank <3>	Electron 3 rank <3>
31,32	Electron 1 rank <4>	Electron 3 rank <4>
33,34	Electron 1 rank <5> MSB	Electron 3 rank <5> MSB
35,36	Electron 1 Region ID <0>	Electron 3 Region ID <0>
37,38	Electron 1 Card ID <0>	Electron 3 Card ID <0>
39,40	Electron 1 Card ID <1>	Electron 3 Card ID <1>
41,42	Electron 1 Card ID <2>	Electron 3 Card ID <2>
43,44	Unused	
45,46	Rec. Card 0: MIP Bit 0	Quiet Bit 0
47,48	Rec. Card 0: MIP Bit 1	Quiet Bit 1
49.50	Rec. Card 1: MIP Bit 0	Quiet Bit 0
51,52	Rec. Card 1: MIP Bit 1	Quiet Bit 1
53,54	Rec. Card 2: MIP Bit 0	Quiet Bit 0
55,56	Rec. Card 2: MIP Bit 1	Quiet Bit 1
57,58	Rec. Card 3: MIP Bit 0	Quiet Bit 0
59,60	Rec. Card 3: MIP Bit 1	Quiet Bit 1
61,62	Unused	
63,64	Unused	
65,66	Unused	
67,68	BC0	'1'

Table 3: All of the non-isolated electron cables have the same configuration. Each cable carries four non-isolated electrons. The non-isolated electron data channels require one cable from each regional crate to the GCT for a total of 18 cables. The MIP and Quiet bits for receiver cards 4 to 6 will also be carried on the non-isolated electron cables. The '1' and BC0 are described in the text. Unused pins are tied to ground. The first wire of the wire pair is the ordinary NECL signal and the second wire is the complement.

All non-isolated electron cables		
Pair	Cycle 0	Cycle 1
1,2	Electron 0 rank <0> LSB	Electron 2 rank <0> LSB
3,4	Electron 0 rank <1>	Electron 2 rank <1>
5,6	Electron 0 rank <2>	Electron 2 rank <2>
7,8	Electron 0 rank <3>	Electron 2 rank <3>
9,10	Electron 0 rank <4>	Electron 2 rank <4>
11,12	Electron 0 rank <5> MSB	Electron 2 rank <5> MSB
13,14	Electron 0 Region ID <0>	Electron 2 Region ID <0>
15,16	Electron 0 Card ID <0>	Electron 2 Card ID <0>
17,18	Electron 0 Card ID <1>	Electron 2 Card ID <1>
19,20	Electron 0 Card ID <2>	Electron 2 Card ID <2>
21,22	Unused	
23,24	Electron 1 rank <0> LSB	Electron 3 rank <0> LSB
25,26	Electron 1 rank <1>	Electron 3 rank <1>
27,28	Electron 1 rank <2>	Electron 3 rank <2>
29,30	Electron 1 rank <3>	Electron 3 rank <3>
31,32	Electron 1 rank <4>	Electron 3 rank <4>
33,34	Electron 1 rank <5> MSB	Electron 3 rank <5> MSB
35,36	Electron 1 Region ID <0>	Electron 3 Region ID <0>
37,38	Electron 1 Card ID <0>	Electron 3 Card ID <0>
39,40	Electron 1 Card ID <1>	Electron 3 Card ID <1>
41,42	Electron 1 Card ID <2>	Electron 3 Card ID <2>
43,44	Unused	
45,46	Rec. Card 4: MIP Bit 0	Quiet Bit 0
47,48	Rec. Card 4: MIP Bit 1	Quiet Bit 1
49,50	Rec. Card 5: MIP Bit 0	Quiet Bit 0
51,52	Rec. Card 5: MIP Bit 1	Quiet Bit 1
53,54	Rec. Card 6: MIP Bit 0	Quiet Bit 0
55,56	Rec. Card 6: MIP Bit 1	Quiet Bit 1
57,58	Unused	
59.60	Unused	
61,62	Unused	
63,64	Unused	
65,66	Unused	
67,68	BC0	‘1’

Table 4: Each electron candidate has four position bits defining their location. Region ID bit <0> defines which region the candidate is in, and Card ID bits <0> to <2> define which card it originated on, making η/ϕ determination possible using a lookup table for each cable. The order is reversed, so that the hexidecimal representation is more easily derived.

Receiver/EISO Card	Card ID <2>	Card ID <1>	Card ID <0>	Region ID <0>
0	0	0	0	0 or 1
1	0	0	1	0 or 1
2	0	1	0	0 or 1
3	0	1	1	0 or 1
4	1	0	0	0 or 1
5	1	0	1	0 or 1
6	1	1	0	0 or 1

Figure 3: Diagram showing approximate borders defined by cables in Tables 5, 6, 7, and 8. Cable numbers are shown in gray (or orange). HF numbering is shown over the appropriate η,ϕ-regions.

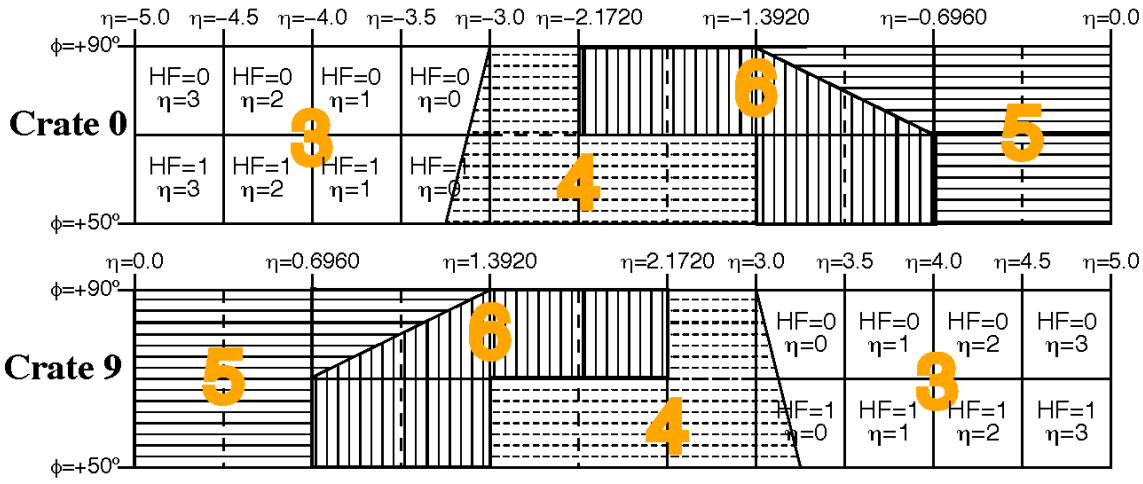


Table 5: Configuration of cable 5 from the JSC to GCT by receiver card (RC) and region. Ten bits of E_T, overflow (o/f) bit, and τ bit for RC 0 and 1 (Regions 0 and 1) and bits <0> to <5> for RC 2 (Regions 0 and 1) are sent. The assignment of ϕ and η is shown in Figure 3. Bit <0> is the LSB for each E_T and bit <10> is the MSB. The first wire of the wire pair is the ordinary NECL signal and the second wire is the complement. The '1' and BC0 are described in the text. Unused pins are tied to ground.

Jet Summary Card to GCT		
Cable 5 pin pair	Cycle 0	Cycle 1
1,2	RC 0 Region 0 <0>	RC 0 Region 1 <0>
3,4	RC 0 Region 0 <1>	RC 0 Region 1 <1>
5,6	RC 0 Region 0 <2>	RC 0 Region 1 <2>
7,8	RC 0 Region 0 <3>	RC 0 Region 1 <3>
9,10	RC 0 Region 0 <4>	RC 0 Region 1 <4>
11,12	RC 0 Region 0 <5>	RC 0 Region 1 <5>
13,14	RC 0 Region 0 <6>	RC 0 Region 1 <6>
15,16	RC 0 Region 0 <7>	RC 0 Region 1 <7>
17,18	RC 0 Region 0 <8>	RC 0 Region 1 <8>
19,20	RC 0 Region 0 <9>	RC 0 Region 1 <9>
21,22	RC 0 Region 0 <10> - o/f	RC 0 Region 1 <10> - o/f
23,24	RC 0 Region 0 <11> - τ	RC 0 Region 1 <11> - τ
25,26	RC 1 Region 0 <0>	RC 1 Region 1 <0>
27,28	RC 1 Region 0 <1>	RC 1 Region 1 <1>
29,30	RC 1 Region 0 <2>	RC 1 Region 1 <2>
31,32	Unused	
33,34	Unused	
35,36	RC 2 Region 0 <5>	RC 2 Region 1 <5>
37,38	RC 2 Region 0 <4>	RC 2 Region 1 <4>
39,40	RC 2 Region 0 <3>	RC 2 Region 1 <3>
41,42	RC 2 Region 0 <2>	RC 2 Region 1 <2>
43,44	RC 2 Region 0 <1>	RC 2 Region 1 <1>
45,46	RC 2 Region 0 <0>	RC 2 Region 1 <0>
47,48	RC 1 Region 0 <11> - τ	RC 1 Region 1 <11> - τ
49,50	RC 1 Region 0 <10> - o/f	RC 1 Region 1 <10> - o/f
51,52	RC 1 Region 0 <9>	RC 1 Region 1 <9>
53,54	RC 1 Region 0 <8>	RC 1 Region 1 <8>
55,56	RC 1 Region 0 <7>	RC 1 Region 1 <7>
57,58	RC 1 Region 0 <6>	RC 1 Region 1 <6>
59,60	RC 1 Region 0 <5>	RC 1 Region 1 <5>
61,62	RC 1 Region 0 <4>	RC 1 Region 1 <4>
63,64	RC 1 Region 0 <3>	RC 1 Region 1 <3>
65,66	Unused	
67,68	BC0	'1'

Table 6: Configuration of cable 6 from the JSC to GCT by receiver card (RC) and region. Ten bits of E_T, overflow (o/f) bit, and τ bit for RC 3 and 4 (Regions 0 and 1) and bits <6> to <11> for RC 2 (Regions 0 and 1) are sent. The assignment of ϕ and η is shown in Figure 3. Bit <0> is the LSB for each E_T and bit <10> is the MSB. The first wire of the wire pair is the ordinary NECL signal and the second wire is the complement. The '1' and BC0 are described in the text. Unused pins are tied to ground.

Jet Summary Card to GCT		
Cable 6 pin pair	Cycle 0	Cycle 1
1,2	RC 2 Region 0 <6>	RC 2 Region 1 <6>
3,4	RC 2 Region 0 <7>	RC 2 Region 1 <7>
5,6	RC 2 Region 0 <8>	RC 2 Region 1 <8>
7,8	RC 2 Region 0 <9>	RC 2 Region 1 <9>
9,10	RC 2 Region 0 <10> - o/f	RC 2 Region 1 <10> - o/f
11,12	RC 2 Region 0 <11> - τ	RC 2 Region 1 <11> - τ
13,14	RC 3 Region 0 <0>	RC 3 Region 1 <0>
15,16	RC 3 Region 0 <1>	RC 3 Region 1 <1>
17,18	RC 3 Region 0 <2>	RC 3 Region 1 <2>
19,20	RC 3 Region 0 <3>	RC 3 Region 1 <3>
21,22	RC 3 Region 0 <4>	RC 3 Region 1 <4>
23,24	RC 3 Region 0 <5>	RC 3 Region 1 <5>
25,26	RC 3 Region 0 <6>	RC 3 Region 1 <6>
27,28	RC 3 Region 0 <7>	RC 3 Region 1 <7>
29,30	RC 3 Region 0 <8>	RC 3 Region 1 <8>
31,32	Unused	
33,34	Unused	
35,36	RC 4 Region 0 <11> - τ	RC 4 Region 1 <11> - τ
37,38	RC 4 Region 0 <10> - o/f	RC 4 Region 1 <10> - o/f
39,40	RC 4 Region 0 <9>	RC 4 Region 1 <9>
41,42	RC 4 Region 0 <8>	RC 4 Region 1 <8>
43,44	RC 4 Region 0 <7>	RC 4 Region 1 <7>
45,46	RC 4 Region 0 <6>	RC 4 Region 1 <6>
47,48	RC 4 Region 0 <5>	RC 4 Region 1 <5>
49,50	RC 4 Region 0 <4>	RC 4 Region 1 <4>
51,52	RC 4 Region 0 <3>	RC 4 Region 1 <3>
53,54	RC 4 Region 0 <2>	RC 4 Region 1 <2>
55,56	RC 4 Region 0 <1>	RC 4 Region 1 <1>
57,58	RC 4 Region 0 <0>	RC 4 Region 1 <0>
59,60	RC 3 Region 0 <11> - τ	RC 3 Region 1 <11> - τ
61,62	RC 3 Region 0 <10> - o/f	RC 3 Region 1 <10> - o/f
63,64	RC 3 Region 0 <9>	RC 3 Region 1 <9>
65,66	Unused	
67,68	BC0	'1'

Table 7: Configuration of cable 4 from the JSC to GCT by the receiver card (RC) and region or HF. Ten bits of E_T, overflow (o/f) bit, and τ bit for RC 5 and 6 (Regions 0 and 1) and the <0> and Quality (Q) bits for the HF are sent. The assignment of ϕ and η is shown in Figure 3. Bit <0> is the LSB for each E_T and bit <10> (Barrel and Endcap) or <7> (HF) is the MSB. The first wire of the wire pair is the ordinary NECL signal and the second wire is the complement.. The '1' and BC0 are described in the text. Unused pins are tied to ground.

Jet Summary Card to GCT		
Cable 4 pin pair	Cycle 0	Cycle 1
1,2	RC 5 Region 0 <0>	RC 5 Region 1 <0>
3,4	RC 5 Region 0 <1>	RC 5 Region 1 <1>
5,6	RC 5 Region 0 <2>	RC 5 Region 1 <2>
7,8	RC 5 Region 0 <3>	RC 5 Region 1 <3>
9,10	RC 5 Region 0 <4>	RC 5 Region 1 <4>
11,12	RC 5 Region 0 <5>	RC 5 Region 1 <5>
13,14	RC 5 Region 0 <6>	RC 5 Region 1 <6>
15,16	RC 5 Region 0 <7>	RC 5 Region 1 <7>
17,18	RC 5 Region 0 <8>	RC 5 Region 1 <8>
19,20	RC 5 Region 0 <9>	RC 5 Region 1 <9>
21,22	RC 5 Region 0 <10> - o/f	RC 5 Region 1 <10> - o/f
23,24	RC 5 Region 0 <11> - τ	RC 5 Region 1 <11> - τ
25,26	RC 6 Region 0 <0>	RC 6 Region 1 <0>
27,28	RC 6 Region 0 <1>	RC 6 Region 1 <1>
29,30	RC 6 Region 0 <2>	RC 6 Region 1 <2>
31,32	Unused	
33,34	Unused	
35,36	HF 0 η 1 <0>	HF 0 η 3 <0>
37,38	HF 0 η 0 <0>	HF 0 η 2 <0>
39,40	HF 1 η 1 – Q bit	HF 1 η 3 – Q bit
41,42	HF 1 η 0 – Q bit	HF 1 η 2 – Q bit
43,44	HF 0 η 1 – Q bit	HF 0 η 3 – Q bit
45,46	HF 0 η 0 – Q bit	HF 0 η 2 – Q bit
47,48	RC 6 Region 0 <11> - τ	RC 6 Region 1 <11> - τ
49,50	RC 6 Region 0 <10> - o/f	RC 6 Region 1 <10> - o/f
51,52	RC 6 Region 0 <9>	RC 6 Region 1 <9>
53,54	RC 6 Region 0 <8>	RC 6 Region 1 <8>
55,56	RC 6 Region 0 <7>	RC 6 Region 1 <7>
57,58	RC 6 Region 0 <6>	RC 6 Region 1 <6>
59,60	RC 6 Region 0 <5>	RC 6 Region 1 <5>
61,62	RC 6 Region 0 <4>	RC 6 Region 1 <4>
63,64	RC 6 Region 0 <3>	RC 6 Region 1 <3>
65,66	Unused	
67,68	BC0	‘1’

Table 8: Configuration of cable 3 from the JSC to GCT by the region's receiver card (RC). Eight bits of E_T for HF 0 η 0,1,2,3 and eight bits of E_T for HF 1 η 0,1,2,3 are sent. The assignment of ϕ and η is shown in Figure 3. Bit <0> is the LSB for each E_T and bit <7> is the MSB. The first wire of the wire pair is the ordinary NECL signal and the second wire is the complement. The '1' and BC0 are described in the text. Unused pins are tied to ground.

Jet Summary Card to GCT		
Cable 3 pin pair	Cycle 0	Cycle 1
1,2	HF 0 η 0 <1>	HF 0 η 2 <1>
3,4	HF 0 η 1 <1>	HF 0 η 3 <1>
5,6	HF 0 η 0 <2>	HF 0 η 2 <2>
7,8	HF 0 η 1 <2>	HF 0 η 3 <2>
9,10	HF 0 η 0 <3>	HF 0 η 2 <3>
11,12	HF 0 η 1 <3>	HF 0 η 3 <3>
13,14	HF 0 η 0 <4>	HF 0 η 2 <4>
15,16	HF 0 η 1 <4>	HF 0 η 3 <4>
17,18	HF 0 η 0 <5>	HF 0 η 2 <5>
19,20	HF 0 η 1 <5>	HF 0 η 3 <5>
21,22	HF 0 η 0 <6>	HF 0 η 2 <6>
23,24	HF 0 η 1 <6>	HF 0 η 3 <6>
25,26	HF 0 η 0 <7>	HF 0 η 2 <7>
27,28	HF 0 η 1 <7>	HF 0 η 3 <7>
29,30	HF 1 η 0 <0>	HF 1 η 2 <0>
31,32	Unused	
33,34	Unused	
35,36	HF 1 η 1 <7>	HF 1 η 3 <7>
37,38	HF 1 η 0 <7>	HF 1 η 2 <7>
39,40	HF 1 η 1 <6>	HF 1 η 3 <6>
41,42	HF 1 η 0 <6>	HF 1 η 2 <6>
43,44	HF 1 η 1 <5>	HF 1 η 3 <5>
45,46	HF 1 η 0 <5>	HF 1 η 2 <5>
47,48	HF 1 η 1 <4>	HF 1 η 3 <4>
49,50	HF 1 η 0 <4>	HF 1 η 2 <4>
51,52	HF 1 η 1 <3>	HF 1 η 3 <3>
53,54	HF 1 η 0 <3>	HF 1 η 2 <3>
55,56	HF 1 η 1 <2>	HF 1 η 3 <2>
57,58	HF 1 η 0 <2>	HF 1 η 2 <2>
59,60	HF 1 η 1 <1>	HF 1 η 3 <1>
61,62	HF 1 η 0 <1>	HF 1 η 2 <1>
63,64	HF 1 η 1 <0>	HF 1 η 3 <0>
65,66	Unused	
67,68	BC0	'1'