Global Muon Trigger Module

MIP/ISO(Quiet) Assignment Units
(AUB/AUF-chip)

Version V1

(Firmware testversion for MQ connections)

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09 April 2010

Revision 0.0

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1 Assignment Unit chips - interconnection test version

1.1 Document updates

1.1.1 Revision 0.0

First design (09 April 2010).

1.2 Description of firmware

- This version of the Assignment Unit chips of GMT board is used only for interconnection tests between PSB boards on slot 19-21 and the GMT system, to check the connections of the MIP and QUIET (ISO) bits.
- The logic of the Assignment Unit chips is not implemented in this version, because the block memories are occupied by the spy-memories, not enough memory-space for LUTs.
- The spy-memories for the MIP and QUIET (ISO) bits are implemented as 36 x 1k x 16 bits, read-writeable via VME bus (16 bits data), 18 memories for MIP and 18 memories for QUIET (6 for each PSB). The depth is fixed to 1k (register MIAU_SpyDepth_addr is not in use in this version).

1.3 Interconnection test procedure

- Filling simulation-memories on PSBs with testpattern and starting data-transfer.
- Setting register `ROP_dummy_cmd_addr` of ROP-chip to 0xC00 (with mask 0xC00) to enable BCRES from TIM to AUB/AUF (on signal DUMMY_AUB and DUMMY_AUF).
- Configuration of AUB/AUF-chips with version V1.
- Setting register `MIAU_ReadoutSyncReg_addr` to 0x11 to get the right BCRES delay for the test.
- Setting register `MIAU_SimuSpyConfig_addr` to 0x2 to enable BCRES from ROP (on signal DUMMY_AUB and DUMMY_AUF).
- Setting register `MIAU_SpyArmPulse_waddr` to 0x1 to start spying on all spy-memories (Writing 1 makes a pulse that sets a ‘spy_armed’ FF so that spying is started with the next BCReset signal (or with next dummy_pulse). The FF is cleared afterwards by the 2nd BCreset. Spying ends after 1k words).
- Reading register `MIAU_SpyDone_raddr` indicates that spying is done (bit 0 = 1).
- Reading spy-memories as described in Table 2.2 and Table 2.3 and check with simulation-data from testpattern.

2 VME Addresses Overview

2.1 VME-Addresstable

Table 2.1: VME-Addresstable

key	description	space	map	address	mask	read	write
AUF_base		memory	0	00500000	0000ffff	1	1
AUB_base		memory	0	00800000	0000ffff	1	1
MIAU_chip_id0_raddr		memory	0	00000000	0000ffff	1	0
MIAU_chip_id1_raddr		memory	0	00000002	0000ffff	1	0
MIAU_chip_rev0_raddr		memory	0	00000004	0000ffff	1	0
MIAU_chip_rev1_raddr		memory	0	00000006	0000ffff	1	0
MIAU_dummy_raddr		memory	0	00000020	0000ffff	1	0
MIAU_ReadoutSyncReg_addr		memory	0	00000028	0000ffff	1	1
MIAU_SimuSpyConfig_addr		memory	0	00000032	0000ffff	1	1
MIAU_SpyDepth_addr		memory	0	00000034	0000ffff	1	1
MIAU_SpyArmPulse_waddr		memory	0	00000036	0000ffff	0	1
MIAU_SpyDone_raddr		memory	0	00000038	0000ffff	1	0
MIAU_DistrRam_base		memory	0	00000400	0000ffff	1	1
MIAU_EtaConvLUT_base0		memory	0	00000400	0000ffff	1	1
MIAU_EtaConvLUT_base1		memory	0	00000600	0000ffff	1	1
MIAU_EtaConvLUT_base2		memory	0	00000800	0000ffff	1	1
MIAU_EtaConvLUT_base3		memory	0	00000A00	0000ffff	1	1
MIAU_SimuRAM_base		memory	0	00002000	0000ffff	1	1
MIAU_BlockRam_base		memory	0	00010000	0000ffff	1	1
MIAU_PhiPro1LUT_base0		memory	0	00010000	0000ffff	1	1
MIAU_PhiPro1LUT_base1		memory	0	00014000	0000ffff	1	1
MIAU_PhiPro1LUT_base2		memory	0	00018000	0000ffff	1	1
MIAU_PhiPro1LUT_base3		memory	0	0001C000	0000ffff	1	1
MIAU_PhiPro2LUT_base0		memory	0	00020000	0000ffff	1	1
MIAU_PhiPro2LUT_base1		memory	0	00024000	0000ffff	1	1
MIAU_PhiPro2LUT_base2		memory	0	00028000	0000ffff	1	1
MIAU_PhiPro2LUT_base3		memory	0	0002C000	0000ffff	1	1
MIAU_EtaProLUT_base0		memory	0	00030000	0000ffff	1	1
MIAU_EtaProLUT_base1		memory	0	00038000	0000ffff	1	1
MIAU_EtaProLUT_base2		memory	0	00040000	0000ffff	1	1
MIAU_EtaProLUT_base3		memory	0	00048000	0000ffff	1	1

2.2 Registers and memories

All registers are 16 bit data register.

2.2.1 ID register

2.2.1.1 MIAU_chip_id0_raddr

Address: 0x00000000, read only

…

2.2.1.2 MIAU_chip_id1_raddr

Address: 0x00000002, read only

…

2.2.1.3 MIAU_chip_rev0_raddr

Address: 0x00000004, read only

…

2.2.1.4 MIAU_chip_rev1_raddr

Address: 0x00000006, read only

…

2.2.1.5 MIAU_chip_month_day

Address: 0x00000008, read only

…

2.2.1.6 MIAU_chip_year_raddr

Address: 0x0000000A, read only

…

2.2.1.7 MIAU_chip_hour_min

Address: 0x0000000C, read only

…

2.2.1.8 MIAU_ffff_sec

Address: 0x0000000E, read only

…

2.2.2 MIAU_dummy_raddr

Address: 0x00000020, read only
Data: 0xABCD (fixed)

2.2.3 MIAU_ReadoutSyncReg_addr

Address: 0x00000028, read/write

D15 - D5	D4
not used	USE_BCRES_DELAY

D3	D2	D1	D0
BCRES_DELAY			

D0-D3: **BCRES_DELAY ...**
D4: **USE_BCRES_DELAY = 1,** use BCRES_DELAY, minimal delay = 1.
USE_BCRES_DELAY = 0 do not use BCRES_DELAY, minimal delay = 0.
D5-D15: not used.

2.2.4 MIAU_SimuSpyConfig_addr

Address: 0x00000032, read/write

D15 – D4
not used

D3	D2	D1	D0
not used		DUMMY_IS_ BCRES	SIMU_MODE

D0: **SIMU_MODE = 0,** spy-memory

SIMU_MODE = 1, sim-memory (do not use in this version)

D1: **DUMMY_IS_BCRES = 0**, use BCRES
DUMMY_IS_BCRES = 1, use dummy as BCRES

D3-D15: not used.

2.2.5 MIAU_SpyDepth_addr

Address: 0x00000034, read/write

D0-D11: define depth of spy-memory (do not use in this version, depth is fixed to 1k)

D12-D15: not used.

2.2.6 MIAU_SpyArmPulse_waddr

Address: 0x00000036, write only

D0: Writing 1 makes a pulse that sets a 'spy_armed' FF so that spying is started with the next BCReset signal (or with next dummy_pulse). The FF is cleared afterwards by the 2nd BCreset. Spying ends after 1k words.

D1-D15: not used.

2.2.7 MIAU_SpyDone_raddr

Address: 0x00000038, read only

D0: After the spying the Done-FF is set.

D1-D15: not used.

2.2.8 MIAU_BlockRam_base

Address: 0x00010000, read/write

Baseaddress of the spy-memories, for ranges see the following tables.

2.2.8.1 AUB-Spy memory-ranges

Table 2.2: AUB spy memory-ranges

AUB-SPY-MEM					PATTERN-FILE						
mem name	**index**	**mem range**		**mem mask**	**ETA/PHI-sector**	**columns**	**PSB slot**	**PSB mem**	**MQ names**		**PSB mem mask**
MIP_MEM_0	0	0x10000	0x107FE	0x0FFF	MQB1_01	53	#19	ch0	MQB1	01M	0x0FFF
MIP_MEM_1	1	0x10800	0x10FFE	0x0FFF	MQB1_23	54	#19	ch1	MQB1	23M	0x0FFF
MIP_MEM_2	2	0x11000	0x117FE	0x0FFF	MQB2_01	49	#19	ch2	MQB2	01M	0x0FFF
MIP_MEM_3	3	0x11800	0x11FFE	0x0FFF	MQB2_23	50	#19	ch3	MQB2	23M	0x0FFF
MIP_MEM_4	4	0x12000	0x127FE	0x3F00	MQB3_6	46	#19	ch5	MQF3	6M	0x3F00
MIP_MEM_5	5	0x12800	0x12FFE	0x3F00	MQB4_6	42	#19	ch7	MQF4	6M	0x3F00
MIP_MEM_6	6	0x13000	0x137FE	0x0FFF	MQB5_01	69	#20	ch0	MQB5	01M	0x0FFF
MIP_MEM_7	7	0x13800	0x13FFE	0x0FFF	MQB5_23	70	#20	ch1	MQB5	23M	0x0FFF
MIP_MEM_8	8	0x14000	0x147FE	0x0FFF	MQB6_01	65	#20	ch2	MQB6	01M	0x0FFF
MIP_MEM_9	9	0x14800	0x14FFE	0x0FFF	MQB6_23	66	#20	ch3	MQB6	23M	0x0FFF
MIP_MEM_10	10	0x15000	0x157FE	0x3F00	MQB7_6	62	#20	ch5	MQF7	6M	0x3F00
MIP_MEM_11	11	0x15800	0x15FFE	0x3F00	MQB8_6	58	#20	ch7	MQF8	6M	0x3F00
MIP_MEM_12	12	0x16000	0x167FE	0x0FFF	MQB9_01	85	#21	ch0	MQB9	01M	0x0FFF
MIP_MEM_13	13	0x16800	0x16FFE	0x0FFF	MQB9_23	86	#21	ch1	MQB9	23M	0x0FFF
MIP_MEM_14	14	0x17000	0x177FE	0x0FFF	MQB10_01	81	#21	ch2	MQB10	01M	0x0FFF
MIP_MEM_15	15	0x17800	0x17FFE	0x0FFF	MQB10_23	82	#21	ch3	MQB10	23M	0x0FFF
MIP_MEM_16	16	0x18000	0x187FE	0x3F00	MQB11_6	78	#21	ch5	MQF11	6M	0x3F00
MIP_MEM_17	17	0x18800	0x18FFE	0x3F00	MQB12_6	74	#21	ch7	MQF12	6M	0x3F00
QUIET_MEM_0	0	0x19000	0x197FE	0x0FFF	MQB1_01	55	#19	ch0	MQB1	01Q	0x0FFF
QUIET_MEM_1	1	0x19800	0x19FFE	0x0FFF	MQB1_23	56	#19	ch1	MQB1	23Q	0x0FFF
QUIET_MEM_2	2	0x1A000	0x1A7FE	0x0FFF	MQB2_01	51	#19	ch2	MQB2	01Q	0x0FFF
QUIET_MEM_3	3	0x1A800	0x1AFFE	0x0FFF	MQB2_23	52	#19	ch3	MQB2	23Q	0x0FFF
QUIET_MEM_4	4	0x1B000	0x1B7FE	0x3F00	MQB3_6	48	#19	ch5	MQF3	6Q	0x3F00
QUIET_MEM_5	5	0x1B800	0x1BFFE	0x3F00	MQB4_6	44	#19	ch7	MQF4	6Q	0x3F00
QUIET_MEM_6	6	0x1C000	0x1C7FE	0x0FFF	MQB5_01	71	#20	ch0	MQB5	01Q	0x0FFF
QUIET_MEM_7	7	0x1C800	0x1CFFE	0x0FFF	MQB5_23	72	#20	ch1	MQB5	23Q	0x0FFF
QUIET_MEM_8	8	0x1D000	0x1D7FE	0x0FFF	MQB6_01	67	#20	ch2	MQB6	01Q	0x0FFF
QUIET_MEM_9	9	0x1D800	0x1DFFE	0x0FFF	MQB6_23	68	#20	ch3	MQB6	23Q	0x0FFF
QUIET_MEM_10	10	0x1E000	0x1E7FE	0x3F00	MQB7_6	64	#20	ch5	MQF7	6Q	0x3F00
QUIET_MEM_11	11	0x1E800	0x1EFFE	0x3F00	MQB8_6	60	#20	ch7	MQF8	6Q	0x3F00
QUIET_MEM_12	12	0x1F000	0x1F7FE	0x0FFF	MQB9_01	87	#21	ch0	MQB9	01Q	0x0FFF
QUIET_MEM_13	13	0x1F800	0x1FFFE	0x0FFF	MQB9_23	88	#21	ch1	MQB9	23Q	0x0FFF
QUIET_MEM_14	14	0x20000	0x207FE	0x0FFF	MQB10_01	83	#21	ch2	MQB10	01Q	0x0FFF
QUIET_MEM_15	15	0x20800	0x20FFE	0x0FFF	MQB10_23	84	#21	ch3	MQB10	23Q	0x0FFF
QUIET_MEM_16	16	0x21000	0x217FE	0x3F00	MQB11_6	80	#21	ch5	MQF11	6Q	0x3F00
QUIET_MEM_17	17	0x21800	0x21FFE	0x3F00	MQB12_6	76	#21	ch7	MQF12	6Q	0x3F00

2.2.8.2 AUF-Spy memory-ranges

Table 2.3: AUF spy memory-ranges

AUF-SPY-MEM					PATTERN-FILE						
mem name	**index**	**mem range**		**mem mask**	**ETA/PHI-sector**	**columns**	**PSB slot**	**PSB mem**	**MQ names**		**PSB mem mask**
MIP_MEM_0	0	0x10000	0x107FE	0x0FFF	MQB1_23	54	#19	ch1	MQB1	23M	0x0FFF
MIP_MEM_1	1	0x10800	0x10FFE	0x0FFF	MQB2_23	50	#19	ch3	MQB2	23M	0x0FFF
MIP_MEM_2	2	0x11000	0x117FE	0x0FFF	MQF3_45	45	#19	ch4	MQF3	45M	0x0FFF
MIP_MEM_3	3	0x11800	0x11FFE	0x003F	MQF3_6	46	#19	ch5	MQF3	6M	0x003F
MIP_MEM_4	4	0x12000	0x127FE	0x0FFF	MQF4_45	41	#19	ch6	MQF4	45M	0x0FFF
MIP_MEM_5	5	0x12800	0x12FFE	0x003F	MQF4_6	42	#19	ch7	MQF4	6M	0x003F
MIP_MEM_6	6	0x13000	0x137FE	0x0FFF	MQB5_23	70	#20	ch1	MQB5	23M	0x0FFF
MIP_MEM_7	7	0x13800	0x13FFE	0x0FFF	MQB6_23	66	#20	ch3	MQB6	23M	0x0FFF
MIP_MEM_8	8	0x14000	0x147FE	0x0FFF	MQF7_45	61	#20	ch4	MQF7	45M	0x0FFF
MIP_MEM_9	9	0x14800	0x14FFE	0x003F	MQF7_6	62	#20	ch5	MQF7	6M	0x003F
MIP_MEM_10	10	0x15000	0x157FE	0x0FFF	MQF8_45	57	#20	ch6	MQF8	45M	0x0FFF
MIP_MEM_11	11	0x15800	0x15FFE	0x003F	MQF8_6	58	#20	ch7	MQF8	6M	0x003F
MIP_MEM_12	12	0x16000	0x167FE	0x0FFF	MQB9_23	86	#21	ch1	MQB9	23M	0x0FFF
MIP_MEM_13	13	0x16800	0x16FFE	0x0FFF	MQB10_23	82	#21	ch3	MQB10	23M	0x0FFF
MIP_MEM_14	14	0x17000	0x177FE	0x0FFF	MQF11_45	77	#21	ch4	MQF11	45M	0x0FFF
MIP_MEM_15	15	0x17800	0x17FFE	0x003F	MQF11_6	78	#21	ch5	MQF11	6M	0x003F
MIP_MEM_16	16	0x18000	0x187FE	0x0FFF	MQF12_45	73	#21	ch6	MQF12	45M	0x0FFF
MIP_MEM_17	17	0x18800	0x18FFE	0x003F	MQF12_6	74	#21	ch7	MQF12	6M	0x003F
QUIET_MEM_0	0	0x19000	0x197FE	0x0FFF	MQB1_23	56	#19	ch1	MQB1	23Q	0x0FFF
QUIET_MEM_1	1	0x19800	0x19FFE	0x0FFF	MQB2_23	52	#19	ch3	MQB2	23Q	0x0FFF
QUIET_MEM_2	2	0x1A000	0x1A7FE	0x0FFF	MQF3_45	47	#19	ch4	MQF3	45Q	0x0FFF
QUIET_MEM_3	3	0x1A800	0x1AFFE	0x003F	MQF3_6	48	#19	ch5	MQF3	6Q	0x003F
QUIET_MEM_4	4	0x1B000	0x1B7FE	0x0FFF	MQF4_45	43	#19	ch6	MQF4	45Q	0x0FFF
QUIET_MEM_5	5	0x1B800	0x1BFFE	0x003F	MQF4_6	44	#19	ch7	MQF4	6Q	0x003F
QUIET_MEM_6	6	0x1C000	0x1C7FE	0x0FFF	MQB5_23	72	#20	ch1	MQB5	23Q	0x0FFF
QUIET_MEM_7	7	0x1C800	0x1CFFE	0x0FFF	MQB6_23	68	#20	ch3	MQB6	23Q	0x0FFF
QUIET_MEM_8	8	0x1D000	0x1D7FE	0x0FFF	MQF7_45	63	#20	ch4	MQF7	45Q	0x0FFF
QUIET_MEM_9	9	0x1D800	0x1DFFE	0x003F	MQF7_6	64	#20	ch5	MQF7	6Q	0x003F
QUIET_MEM_10	10	0x1E000	0x1E7FE	0x0FFF	MQF8_45	59	#20	ch6	MQF8	45Q	0x0FFF
QUIET_MEM_11	11	0x1E800	0x1EFFE	0x003F	MQF8_6	60	#20	ch7	MQF8	6Q	0x003F
QUIET_MEM_12	12	0x1F000	0x1F7FE	0x0FFF	MQB9_23	88	#21	ch1	MQB9	23Q	0x0FFF
QUIET_MEM_13	13	0x1F800	0x1FFFE	0x0FFF	MQB10_23	84	#21	ch3	MQB10	23Q	0x0FFF
QUIET_MEM_14	14	0x20000	0x207FE	0x0FFF	MQF11_45	79	#21	ch4	MQF11	45Q	0x0FFF
QUIET_MEM_15	15	0x20800	0x20FFE	0x003F	MQF11_6	80	#21	ch5	MQF11	6Q	0x003F
QUIET_MEM_16	16	0x21000	0x217FE	0x0FFF	MQF12_45	75	#21	ch6	MQF12	45Q	0x0FFF
QUIET_MEM_17	17	0x21800	0x21FFE	0x003F	MQF12_6	76	#21	ch7	MQF12	6Q	0x003F

2.2.9 Unused memory-ranges

Because the logic of the Assignment Unit chips is not implemented in this version, the following memories (LUTs) are not used in this version, whether they are in address-table:

Table 2.4: Unused memory-ranges

MIAU_DistrRam_base	0x00000400
MIAU_EtaConvLUT_base0	0x00000400
MIAU_EtaConvLUT_base1	0x00000600
MIAU_EtaConvLUT_base2	0x00000800
MIAU_EtaConvLUT_base3	0x00000A00
MIAU_SimuRAM_base	0x00002000
MIAU_BlockRam_base	0x00010000
MIAU_PhiPro1LUT_base0	0x00010000
MIAU_PhiPro1LUT_base1	0x00014000
MIAU_PhiPro1LUT_base2	0x00018000
MIAU_PhiPro1LUT_base3	0x0001C000
MIAU_PhiPro2LUT_base0	0x00020000
MIAU_PhiPro2LUT_base1	0x00024000
MIAU_PhiPro2LUT_base2	0x00028000
MIAU_PhiPro2LUT_base3	0x0002C000
MIAU_EtaProLUT_base0	0x00030000
MIAU_EtaProLUT_base1	0x00038000
MIAU_EtaProLUT_base2	0x00040000
MIAU_EtaProLUT_base3	0x00048000

3 MIP/ISO bits from GCT-PSB-Cables

3.1 Mapping GCT cables

Figure 3.1: Block diagram of GTL-9U Module

		-6	-5	-4	-3	-2	-1	0
	0	3_6_0	3_45_1	3_45_0	1_23_1	1_23_0	1_01_1	1_01_0
	1	3_6_1	3_45_3	3_45_2	1_23_3	1_23_2	1_01_3	1_01_2
	2	3_6_8	3_45_9	3_45_8	1_23_9	1_23_8	1_01_9	1_01_8
	3	3_6_9	3_45_11	3_45_10	1_23_11	1_23_10	1_01_11	1_01_10
	4	4_6_4	4_45_5	4_45_4	2_23_5	2_23_4	2_01_5	2_01_4
	5	4_6_5	4_45_7	4_45_6	2_23_7	2_23_6	2_01_7	2_01_6
	6	7_6_0	7_45_1	7_45_0	5_23_1	5_23_0	5_01_1	5_01_0
	7	7_6_1	7_45_3	7_45_2	5_23_3	5_23_2	5_01_3	5_01_2
	8	7_6_8	7_45_9	7_45_8	5_23_9	5_23_8	5_01_9	5_01_8
	9	7_6_9	7_45_11	7_45_10	5_23_11	5_23_10	5_01_11	5_01_10
	10	8_6_4	8_45_5	8_45_4	6_23_5	6_23_4	6_01_5	6_01_4
	11	8_6_5	8_45_7	8_45_6	6_23_7	6_23_6	6_01_7	6_01_6
	12	11_6_0	11_45_1	11_45_0	9_23_1	9_23_0	9_01_1	9_01_0
	13	11_6_1	11_45_3	11_45_2	9_23_3	9_23_2	9_01_3	9_01_2
	14	11_6_8	11_45_9	11_45_8	9_23_9	9_23_8	9_01_9	9_01_8
	15	11_6_9	11_45_11	11_45_10	9_23_11	9_23_10	9_01_11	9_01_10
	16	12_6_4	12_45_5	12_45_4	10_23_5	10_23_4	10_01_5	10_01_4
phi	17	12_6_5	12_45_7	12_45_6	10_23_7	10_23_6	10_01_7	10_01_6

0	1	2	3	4	5	6
1_01_4	1_01_5	1_23_4	1_23_5	3_45_4	3_45_5	3_6_4
1_01_6	1_01_7	1_23_6	1_23_7	3_45_6	3_45_7	3_6_5
2_01_0	2_01_1	2_23_0	2_23_1	4_45_0	4_45_1	4_6_0
2_01_2	2_01_3	2_23_2	2_23_3	4_45_2	4_45_3	4_6_1
2_01_8	2_01_9	2_23_8	2_23_9	4_45_8	4_45_9	4_6_8
2_01_10	2_01_11	2_23_10	2_23_11	4_45_10	4_45_11	4_6_9
5_01_4	5_01_5	5_23_4	5_23_5	7_45_4	7_45_5	7_6_4
5_01_6	5_01_7	5_23_6	5_23_7	7_45_6	7_45_7	7_6_5
6_01_0	6_01_1	6_23_0	6_23_1	8_45_0	8_45_1	8_6_0
6_01_2	6_01_3	6_23_2	6_23_3	8_45_2	8_45_3	8_6_1
6_01_8	6_01_9	6_23_8	6_23_9	8_45_8	8_45_9	8_6_8
6_01_10	6_01_11	6_23_10	6_23_11	8_45_10	8_45_11	8_6_9
9_01_4	9_01_5	9_23_4	9_23_5	11_45_4	11_45_5	11_6_4
9_01_6	9_01_7	9_23_6	9_23_7	11_45_6	11_45_7	11_6_5
10_01_0	10_01_1	10_23_0	10_23_1	12_45_0	12_45_1	12_6_0
10_01_2	10_01_3	10_23_2	10_23_3	12_45_2	12_45_3	12_6_1
10_01_8	10_01_9	10_23_8	10_23_9	12_45_8	12_45_9	12_6_8
10_01_10	10_01_11	10_23_10	10_23_11	12_45_10	12_45_11	12_6_9

Tables show the MIP/ISO bit assignment into cables for both sides of CMS.
Horizontal: ETA values between -6….+6
Vertical: PHI values 0….17 (20° units)
Syntax: CableNr_EtaValues_BitNumberOnCable (starting with zero)

3.2 Mapping GCT cables to PSB channels and backplane signals

PSB in SLOT19: ← GCT Cables 1,2,3,4
blue number = bit# in PSB. The empty PSB bits are not connected to the GMT board.
Red MQ bits are sent parallel, to the barrel as well to the forward GMT Assignment logic

Figure 3.2: PSB #19 GCT cables 1-4

GCT cable 4 ➔ ch6_7
MEM7 ➔ bit31-16, MEM6 ➔ bit15-0

30	31
MQB4_45_8	MQB4_45_10
MQB4_45_4	MQB4_45_6
MQB4_45_0	MQB4_45_2
22	23
MQF4_6_8	MQF4_6_9
MQF4_6_4	MQF4_6_5
MQF4_6_0	MQF4_6_1
14	15
12	13
MQF4_45_10	MQF4_45_11
MQF4_45_8	MQF4_45_9
MQF4_45_6	MQF4_45_7
MQF4_45_4	MQF4_45_5
MQF4_45_2	MQF4_45_3
MQF4_45_0	MQF4_45_1

GCT cable 2 ➔ ch2_3
MEM3 ➔ bit31-16, MEM2 ➔ bit15-0

30	31
28	29
MQB2_23_10	MQB2_23_11
MQB2_23_8	MQB2_23_9
MQB2_23_6	MQB2_23_7
MQB2_23_4	MQB2_23_5
MQB2_23_2	MQB2_23_3
MQB2_23_0	MQB2_23_1
14	15
12	13
MQB2_01_10	MQB2_01_11
MQB2_01_8	MQB2_01_9
MQB2_01_6	MQB2_01_7
MQB2_01_4	MQB2_01_5
MQB2_01_2	MQB2_01_3
MQB2_01_0	MQB2_01_1

GCT cable 3 ➔ ch4_5
MEM5 ➔ bit31-16, MEM4 ➔ bit15-0

30	31
MQB3_45_8	MQB3_45_10
MQB3_45_4	MQB3_45_6
MQB3_45_0	MQB3_45_2
22	23
MQF3_6_8	MQF3_6_9
MQF3_6_4	MQF3_6_5
MQF3_6_0	MQF3_6_1
14	15
12	13
MQF3_45_10	MQF3_45_11
MQF3_45_8	MQF3_45_9
MQF3_45_6	MQF3_45_7
MQF3_45_4	MQF3_45_5
MQF3_45_2	MQF3_45_3
MQF3_45_0	MQF3_45_1

GCT cable 1 ➔ ch0_1
MEM1 ➔ bit31-16, MEM0 ➔ bit15-0

30	31
28	29
MQB1_23_10	MQB1_23_11
MQB1_23_8	MQB1_23_9
MQB1_23_6	MQB1_23_7
MQB1_23_4	MQB1_23_5
MQB1_23_2	MQB1_23_3
MQB1_23_0	MQB1_23_1
14	15
12	13
MQB1_01_10	MQB1_01_11
MQB1_01_8	MQB1_01_9
MQB1_01_6	MQB1_01_7
MQB1_01_4	MQB1_01_5
MQB1_01_2	MQB1_01_3
MQB1_01_0	MQB1_01_1

Figure 3.3: PSB #20 GCT cables 5-8

PSB in SLOT20:

GCT cable 8 ➔ ch6_7

MEM7 ➔ bit31-16, MEM6 ➔ bit15-0

30	31
MQB8_45_8	MQB8_45_10
MQB8_45_4	MQB8_45_6
MQB8_45_0	MQB8_45_2
22	23
MQF8_6_8	MQF8_6_9
MQF8_6_4	MQF8_6_5
MQF8_6_0	MQF8_6_1
14	15
12	13
MQF8_45_10	MQF8_45_11
MQF8_45_8	MQF8_45_9
MQF8_45_6	MQF8_45_7
MQF8_45_4	MQF8_45_5
MQF8_45_2	MQF8_45_3
MQF8_45_0	MQF8_45_1

GCT cable 7 ➔ ch4_5

MEM5 ➔ bit31-16, MEM4 ➔ bit15-0

30	31
MQB7_45_8	MQB7_45_10
MQB7_45_4	MQB7_45_6
MQB7_45_0	MQB7_45_2
22	23
MQF7_6_8	MQF7_6_9
MQF7_6_4	MQF7_6_5
MQF7_6_0	MQF7_6_1
14	15
12	13
MQF7_45_10	MQF7_45_11
MQF7_45_8	MQF7_45_9
MQF7_45_6	MQF7_45_7
MQF7_45_4	MQF7_45_5
MQF7_45_2	MQF7_45_3
MQF7_45_0	MQF7_45_1

GCT cable 6 ➔ ch2_3

MEM3 ➔ bit31-16, MEM2 ➔ bit15-0

30	31
28	29
MQB6_23_10	MQB6_23_11
MQB6_23_8	MQB6_23_9
MQB6_23_6	MQB6_23_7
MQB6_23_4	MQB6_23_5
MQB6_23_2	MQB6_23_3
MQB6_23_0	MQB6_23_1
14	15
12	13
MQB6_01_10	MQB6_01_11
MQB6_01_8	MQB6_01_9
MQB6_01_6	MQB6_01_7
MQB6_01_4	MQB6_01_5
MQB6_01_2	MQB6_01_3
MQB6_01_0	MQB6_01_1

GCT cable 5 ➔ ch0_1

MEM1 ➔ bit31-16, MEM0 ➔ bit15-0

30	31
28	29
MQB5_23_10	MQB5_23_11
MQB5_23_8	MQB5_23_9
MQB5_23_6	MQB5_23_7
MQB5_23_4	MQB5_23_5
MQB5_23_2	MQB5_23_3
MQB5_23_0	MQB5_23_1
14	15
12	13
MQB5_01_10	MQB5_01_11
MQB5_01_8	MQB5_01_9
MQB5_01_6	MQB5_01_7
MQB5_01_4	MQB5_01_5
MQB5_01_2	MQB5_01_3
MQB5_01_0	MQB5_01_1

The empty PSB bits are not connected to the GMT board.

Figure 3.4: PSB #21 GCT cables 9-12

PSB in SLOT21:

GCT cable 12 ➔ ch6_7
MEM7 ➔ bit31-16, MEM6 ➔ bit15-0

30	31
MQB12_45_8	MQB12_45_10
MQB12_45_4	MQB12_45_6
MQB12_45_0	MQB12_45_2
22	23
MQF12_6_8	MQF12_6_9
MQF12_6_4	MQF12_6_5
MQF12_6_0	MQF12_6_1
14	15
12	13
MQF12_45_10	MQF12_45_11
MQF12_45_8	MQF12_45_9
MQF12_45_6	MQF12_45_7
MQF12_45_4	MQF12_45_5
MQF12_45_2	MQF12_45_3
MQF12_45_0	MQF12_45_1

GCT cable 11 ➔ ch4-5,
MEM5 ➔ bit31-16, MEM4 ➔ bit15-0

30	31
MQB11_45_8	MQB11_45_10
MQB11_45_4	MQB11_45_6
MQB11_45_0	MQB11_45_2
22	23
MQF11_6_8	MQF11_6_9
MQF11_6_4	MQF11_6_5
MQF11_6_0	MQF11_6_1
14	15
12	13
MQF11_45_10	MQF11_45_11
MQF11_45_8	MQF11_45_9
MQF11_45_6	MQF11_45_7
MQF11_45_4	MQF11_45_5
MQF11_45_2	MQF11_45_3
MQF11_45_0	MQF11_45_1

GCT cable 10 ➔ ch2_3
MEM3 ➔ bit31-16, MEM2 ➔ bit15-0

30	31
28	29
MQB10_23_10	MQB10_23_11
MQB10_23_8	MQB10_23_9
MQB10_23_6	MQB10_23_7
MQB10_23_4	MQB10_23_5
MQB10_23_2	MQB10_23_3
MQB10_23_0	MQB10_23_1
14	15
12	13
MQB10_01_10	MQB10_01_11
MQB10_01_8	MQB10_01_9
MQB10_01_6	MQB10_01_7
MQB10_01_4	MQB10_01_5
MQB10_01_2	MQB10_01_3
MQB10_01_0	MQB10_01_1

GCT cable 9 ➔ ch0_1
MEM1 ➔ bit31-16, MEM0 ➔ bit15-0

30	31
28	29
MQB9_23_10	MQB9_23_11
MQB9_23_8	MQB9_23_9
MQB9_23_6	MQB9_23_7
MQB9_23_4	MQB9_23_5
MQB9_23_2	MQB9_23_3
MQB9_23_0	MQB9_23_1
14	15
12	13
MQB9_01_10	MQB9_01_11
MQB9_01_8	MQB9_01_9
MQB9_01_6	MQB9_01_7
MQB9_01_4	MQB9_01_5
MQB9_01_2	MQB9_01_3
MQB9_01_0	MQB9_01_1

The empty PSB bits are not connected to the GMT board.