Jumper and switches on FDL-9U-card

JP1: selection of VIO of masterblaster
OFF ➔ no voltage on VIO.
ON ➔ LV3V3 or VCC on VIO (see JP3).

JP2: TRST of VME64X-chip
OFF ➔ always off.

JP3: voltage selection for masterblaster
1-2 (default)➔ LV3V3.
2-3 ➔ VCC.

JP4: VME64X-chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP5: PROM of VME64X -chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP6: VME-FDL-chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP7: PROM of VME-FDL-chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP8: 1st PROM of FDL-chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP9: 2nd PROM of FDL -chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP10: 3rd PROM of FDL -chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP11: 4th PROM of FDL -chip in JTAG-chain
1-2 ➔ in JTAG-chain.
2-3 (default)➔ **not** in JTAG-chain.

JP12: FDL -chip in JTAG-chain
1-2 ➔ FDL -chip in JTAG-chain.
2-3 (default)➔ FDL -chip **not** in JTAG-chain.

JP13, JP14, JP15 and JP16: JTAG-chain - ParallelCableIV or VME-JTAG
1-2 ➔ VME-JTAG.
2-3 ➔ ParallelCableIV.

JP17, JP20, JP21, JP22 and JP23: programming signals for FDL-chip
1-2 (default)➔ programming via VME.
2-3 ➔ programming via PROM (XC18V04).

JP18 and JP19: selection of CLK_TO_PLL
Only one jumper may be ON!
JP18 ON ➔ CLK_OSC (from oscillator).
JP19 ON (default)➔ CLK_FROM_TIM.

JP24: EN_CONF_BY_VME
OFF ➔ Configuration of FDL-chips via VME enabled (EN_CONF_BY_VME=1).
ON ➔ Configuration of FDL-chips via VME disabled (EN_CONF_BY_VME=0).

JP25: HSWAP_EN input of FDL-chip
1-2 (default)➔ enables pull-up-Rs of all I/O-pins in FDL-chip before configuration. In this position **configuration of FDL-chip via VME possible**.
2-3 ➔ keeps jumper in OFF-position (I/O-pins in high-Z before configuration). In this position **configuration of FDL-chip** via **VME not possible**.

JP26: CLK_FB_FDL
OFF ➔ no feedback.
ON ➔ feedback.

JP27, JP28 and JP29: LV1V5
OFF ➔ only for tests.
ON ➔ to supply voltage (jumpers not soldered – solderbridges used).

JP45: N_IACKIN/N_IACKOUT
ON ➔ always on, no interrupt.

SW1: base address switches for VME
base address for extended address mode used in GT-system.

SW2: RUNNIG button
Set the board in RUNNING mode after inserting the board into the crate.

SW3: INACTIVE button
Set the board in INACTIVE mode to remove the board from the crate.

SW4: JTAG-chain selector
1 ➔ S0 of slotnumber of bounary scan
2 ➔ S1 of slotnumber of bounary scan
3 ➔ S2 of slotnumber of bounary scan
4 ➔ S3 of slotnumber of bounary scan
5 ➔ S4 of slotnumber of bounary scan
6 ➔ S5 of slotnumber of bounary scan
7 ➔ ON = enables ParallelCableIV / VME-JTAG
8 ➔ ON = enables MasterBlaster