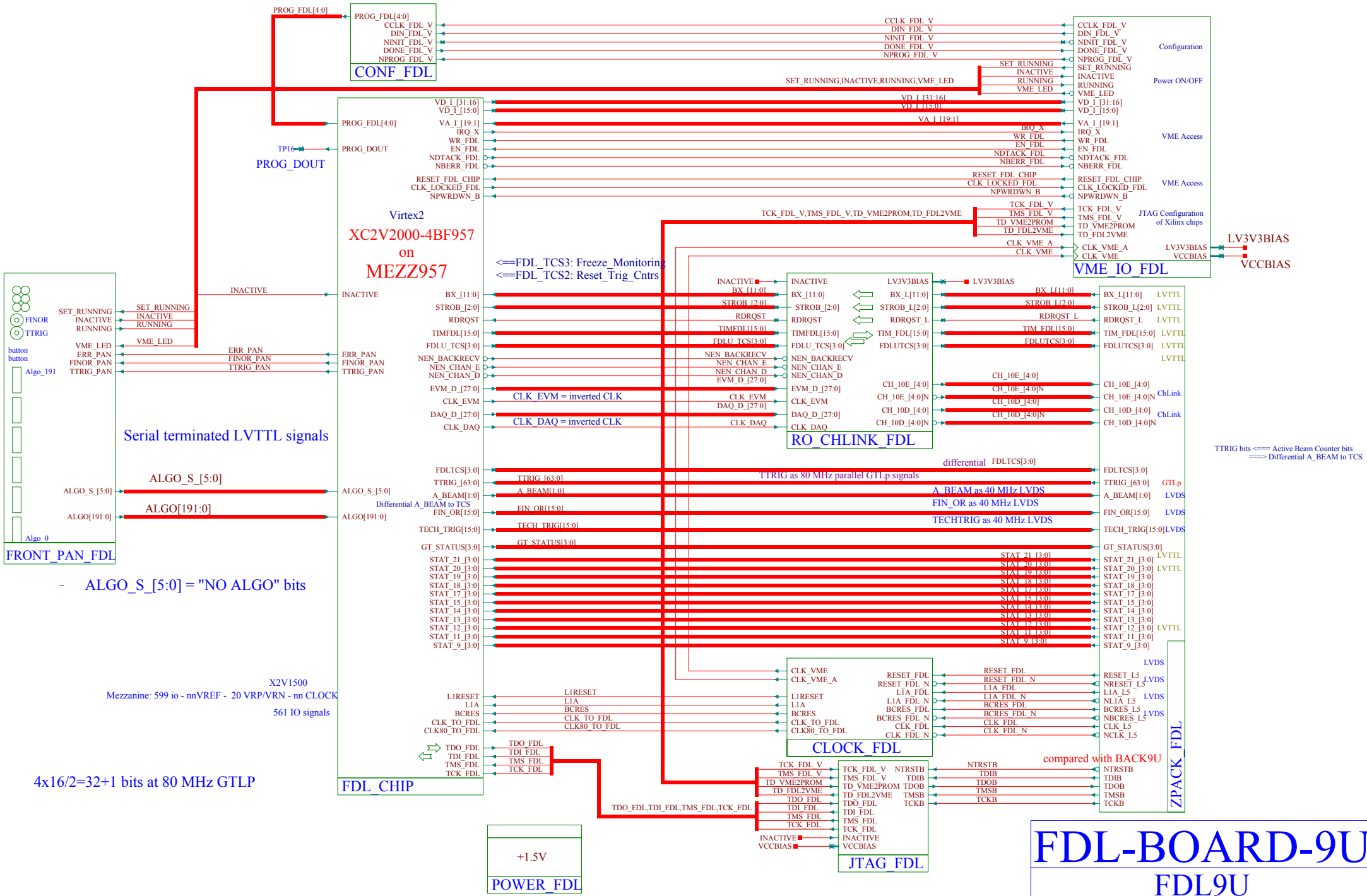
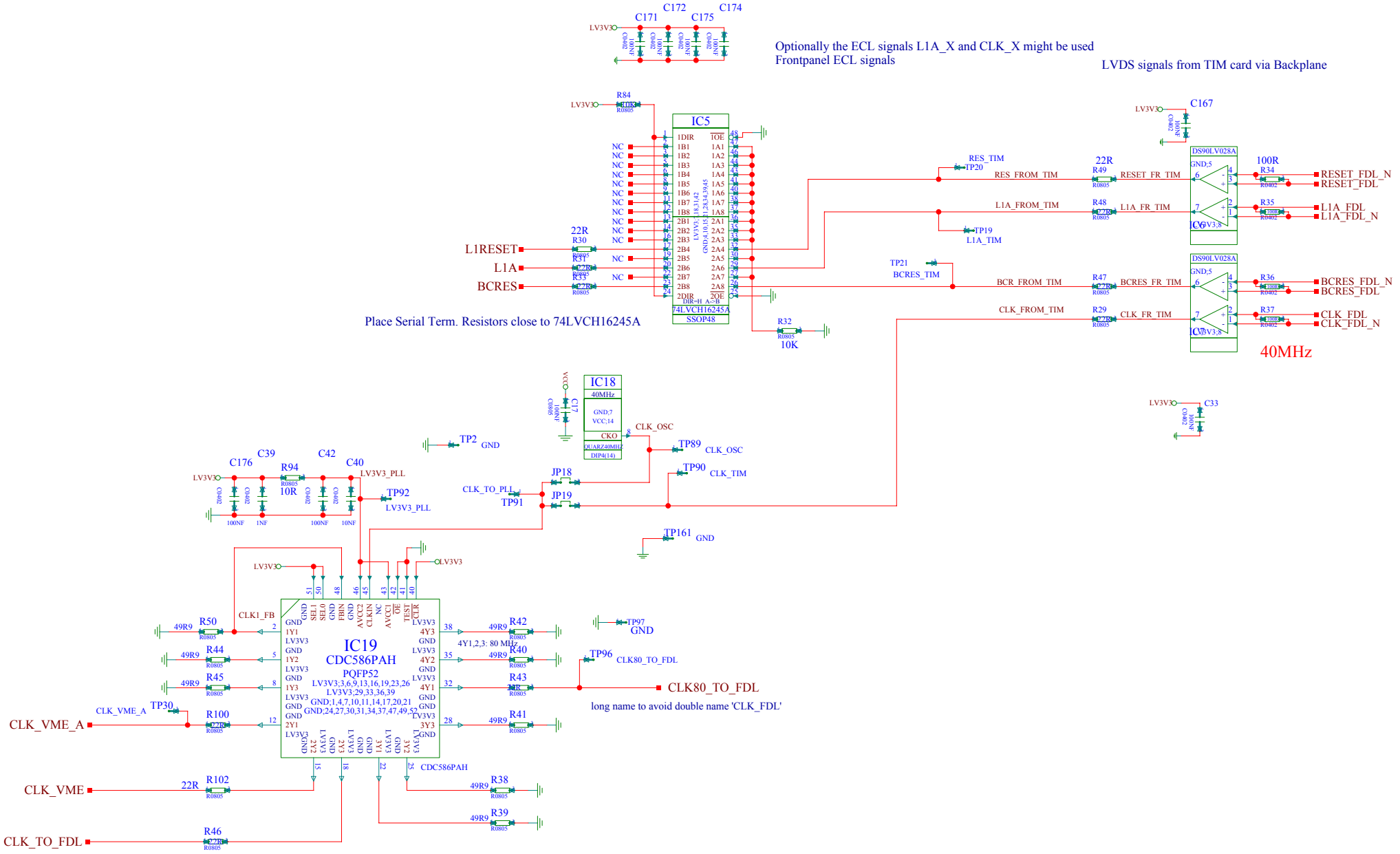


FDL-BOARD-9U

FDL9U

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.T	5-12-2004_14:49
checked by: AT+MP	120504

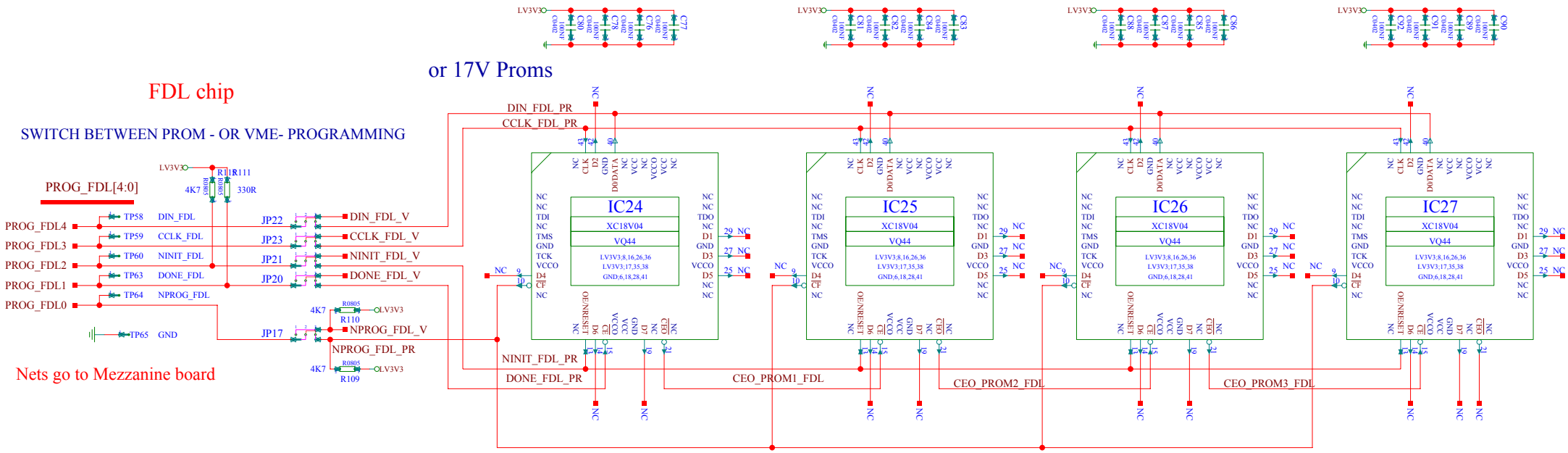
FDL9U_VORGABEN;P:\GLOBALTRIGGER\FDL\FDL9U\DOC\FDL-9U-VORGABEN.DOC



FDL-CARD-9U

CLOCK_FDL

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: AT 7.NOV03	5-14-2004_10:03
checked by: A.TAUROK	110504



Achtung: REFDES in CONF_FDL und JTAG müssen übereinstimmen!!!

How to reconfigure FPGA from prom when already running?
FPGA is in master serial mode.

See FDL_CHIP schematic to find:
HSWAP_EN_FDL
NPWRDWN_B
DOUT_FDL
On Mezzanine board for FDL you find: M0,M1,M2

JTAG pins : See JTAG circuits

Selecting Configuration Modes

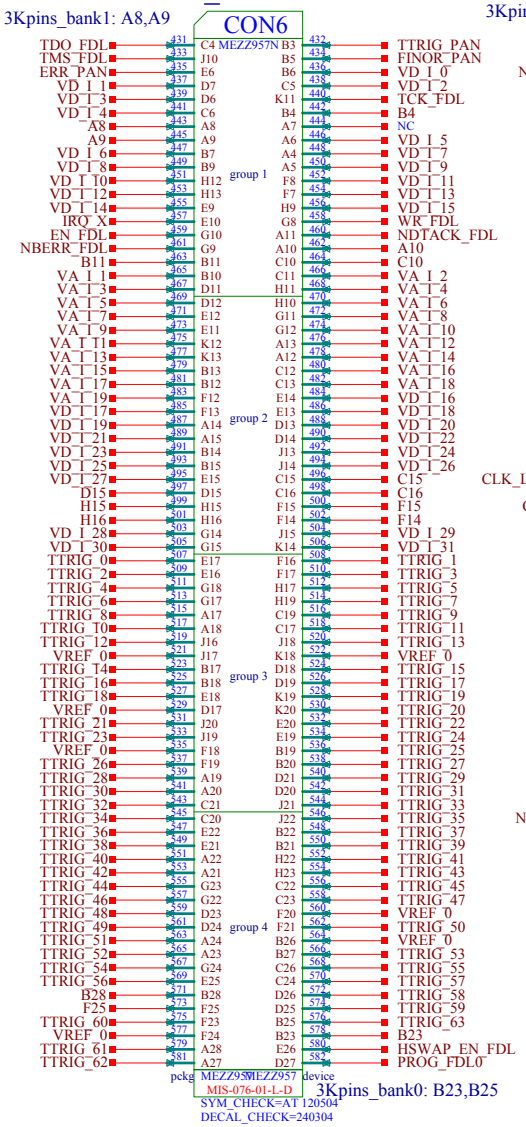
The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx JTAG Programmer software. Serial output is the default programming mode.

We use serial mode only.

FDL-CARD-9U	
CONF_FDL	
HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.TAUROK	5-11-2004_16:40
checked by: A.TAUROK	110504

NORD MIS_076 connector

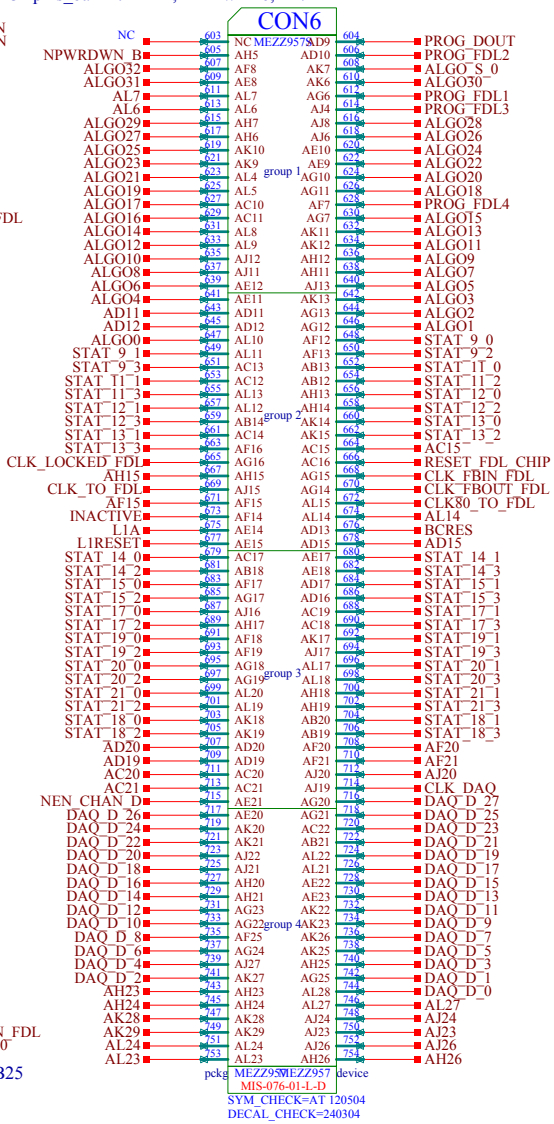
3Kpins_bank1: A8,A9



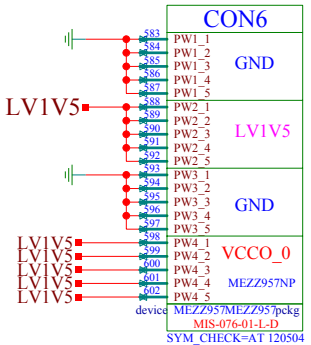
3Kpins_bank0: B23,B25

SOUTH MIS_076 connector

3Kpins_bank4: AD11,AD12 //AL6,AL7

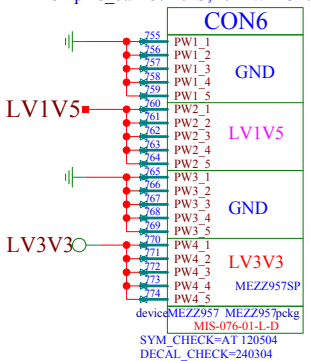


3Kpins_bank5: AJ23,AJ24 // AC20,AC21 // AL23,AL24 // AH23,AH24



Default: Apply 3.3V to VCCO_0 (=Banks 0)

FDL: Apply 1.5V to VCCO_0 (=Banks 0) for GTL+ signals

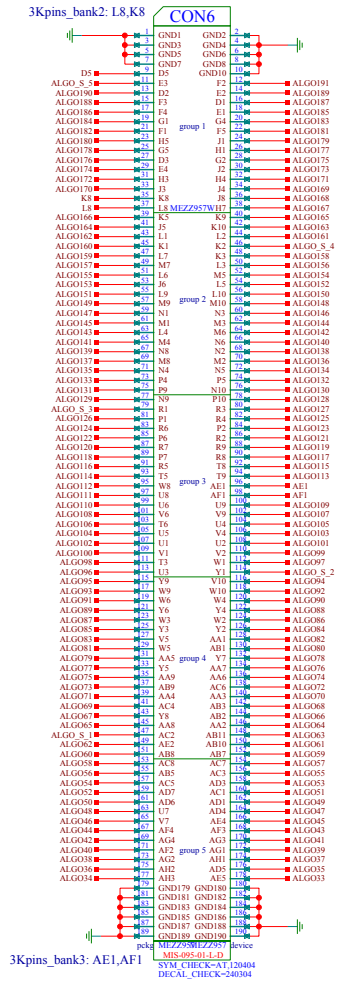


APPLY always 3.3V to Banks 4,5

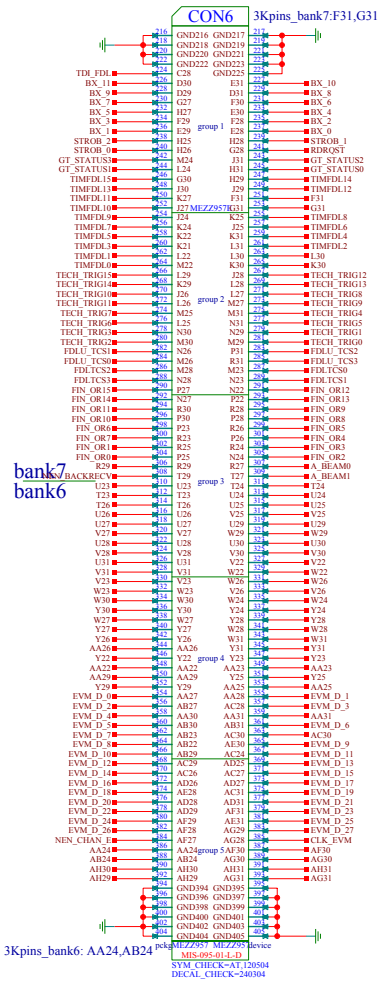
MEZZ957 TEMPLATE for 9U BOARDS

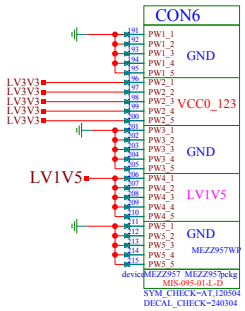
MEZZ957 TEMPLATE		
FDL_CHIP		
HEPHY VIENNA ELEKTRONIK 1	sheet 1	of 3
modified by: A.T 13.2.04	5-12-2004	14:22
checked by: MP+AT 120504	12-05-2004	

WEST MIS_095 connector

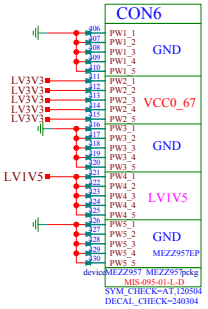


EAST MIS_095 connector





Default: Apply 3.3V to VCCO_123 (=Banks 1,2,3)



Default: Apply 3.3V to VCCO_67 (=Banks 6,7)

MEZZ957 TEMPLATE for 9U BOARDS

MEZZ957 TEMPLATE

FDL_CHIP

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: AT 13.2.04	5-12-2004_14:38
checked by: CHECKER	0-00-0000_00:00

1CLB = 4 slices (as 2x2) 1slice= F+G LUT, 2 FF, hor.cascade OR,

Device	Row x Col.	/Slices/RAM	kbits/Multiplier/RAMBlocks (Kbits)/DCMs/maxIO pads				
XC2V1000	40x32	5120	160	40	40	8	432
XC2V1500	48x40	7680	240	48	48	8	528

XC2V1500: =15360 DFF XC2V2000-4BF957 xxx io
XC2V1500-5FF896 413 $ XC2V3000-4BF957 xxx io

Monitor RAMs: (192+16+68)/16 = 18RAMblocks RingBuf (DPM)
18RAMblocks RO-Buf (Fifo)
1RAMblocks BX-Buf
1RAMblocks L1Aqueue 1 RAMblock =18 kbit DPRAM

RI-BUF VME-access: A15-A1 for 18 1kW-DPMs
FDL chip pins: 369 (without ALGO bits to EVM)

Algo bits to Event Manager:
~~Option1: Send Algo bits to FDL chip and to output drivers ==> NOT enough pins on TCS conn.~~
Option2: L1A extracts data from RI-buf and sends them via ChanLink to EVM-link
Option2: ....and via another ChanLink to GTFE
Option2: 369 +30 pins too many for chip
==> reduce other pins

Monitor: not prescaled algo bits
RATE counters: prescaled algo bits
TCS ==> FDL: L1A for EVM readout

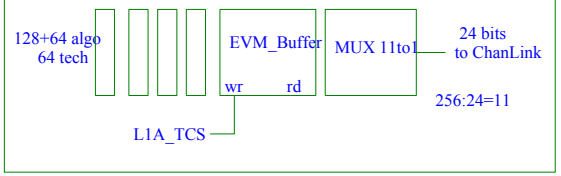
RATE COUNTER monitoring
192 counters 32bits
1sec=>40 Mio=262 5A00
6 sec =E4...=28 bits
107 sec =E4...=32bits
Reset Rate counters every 1 sec or 10 sec
The reset stores all counters into registers.
The reset stores also the overall orbit number
FDL: decodes Reset Orbit instruction to get overall orbit number of run.

Welcher Chip wird denn nun verwendet? Es ist nirgends definiert!! M.P.
XC2V3000????? benötigt 3 Proms XC18V04VQ44C
XC2V4000????? benötigt 4 Proms XC18V04VQ44C A.T: Ich hoffe dass XC2V2000 genügt.
XC2V6000????? benötigt 6 Proms XC18V04VQ44C

LOGIC IDEEN:

to EVM: raw Algos of 1 bx
to DAQ: raw Algos of 3(5) bx

EVM: instead of Ring buffer make 2-3 step pipeline for all Algos
EVM: L1A_TCS moves EVM data into EVM_Buffer FIFO
EVM: MUX applies all bits of an bx to the channel link outputs



Nets copied from fdl9u schematic:

VREF, CLK, Special PINS have to be on same pins on both MEZZ boards.

VD_I_[31:16]...connected

VD_I_[31:16]
VD_I_[15:0]
VA_I_[19:1]
IRQ_X
WR_FDL
EN_FDL
NDTACK_FDL
NBERR_FDL
43 or 59 VME
Bank 1

INACTIVE
CLK_LOCKED_FDL
RESET_FDL_CHIP
CLK_FBOUT_FDL
CLK_FBIN_FDL
NPWRDWN_B
Bank 45

PROG_DOUT
goes to TEST Point
PROG_FDL[4:0]

TTRIG[63:0] connected to Bank 0
TTRIG63 is not connected to XC3V2000
==> VCCO_0 =1.5V for GTL+ signals

To Front side
ERR_PAN
FINOR_PAN
TTRIG_PAN
3 Panel
Bank 1

43 or 59 VME
3 Panel NORD 64 TTRIG
GTLP
GND LV1V5 GND VCCO_0
16 RO-bus
4 GT STATUS
16 to boards
42 differential
VCCO_123 VCCO_67 GTLP
bank1 72/70 bank0 72/70
bank2 84/82 84/82 bank7
WEST MEZZ957 EAST
bank3 84/82 84/82 bank6
76/68 76/68
bank4 bank5
GND LV1V5 GND LV3V3
60 CH Links
198 ALGO
SOUTH
12x4=44 STATUS
5 CLOCK

From Front side
ALGO_S_[5:0]
198 ALGO
ALGO[191:0]
Bank 234
Algo192 oben
Algo0 unten

Bank 0 64 TTRIG
TTRIG_[63:0]
Bank 7 oben 16 RO-bus
BX_[11:0]
STROB_[2:0]
RDRQST
Bank 7 4 GT STATUS
GT_STATUS[3:0]
Bank 7 16 to boards
TIMFDL[15:0]
Bank 7 16 differential
TECH_TRIG[15:0]
Bank 7 4 differential
FDLU_TCS[3:0]
NEN_BACKRECV
FDLTCS[3:0]
4 differential
Bank 7 18 differential
FIN_OR[15:0]
A_BEAM[1:0]

Bank 6
NEN_CHAN_E
CLK_EVM
EVM_D_[27:0]
60 CH Links
NEN_CHAN_D
CLK_DAQ
DAQ_D_[27:0]
Bank 5

Bank 45 CLOCK 5
L1RESET
L1A
BCRES
CLK_TO_FDL
CLK80_TO_FDL

STAT_21_[3:0]
STAT_20_[3:0]
STAT_19_[3:0]
STAT_18_[3:0]
STAT_17_[3:0]
STAT_15_[3:0]
STAT_14_[3:0]
STAT_13_[3:0]
STAT_12_[3:0]
STAT_11_[3:0]
STAT_9_[3:0]
12x4=44 STATUS
Bank 4,5
SUM = 517 io

JTAG SIGNALS
TDI_FDL
TDO_FDL
TMS_FDL
TCK_FDL

TP94 DRILL_2.2MM
TP95 DRILL_2.2MM

CLK_TO_FDL
CLK80_TO_FDL
LV1V5
E96 1% 499R
VREF_0
VREF_0= 1.0V
LV3V0
10K
JP25
HSWAP_EN_FDL
CLK_FBIN_FDL JP26 CLK_FBOUT_FDL

NPWRDWN_B is bidirectional pin!!
NPWRDWN_for each Virtex chip necessary!

FDL-BOARD-9U

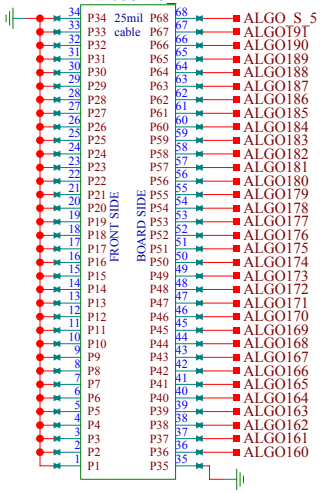
FDL_CHIP

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3	
modified by: M.P.		5-12-2004_14:23
checked by: CHECKER		0-00-0000_00:00

uppermost connector

CON160_191

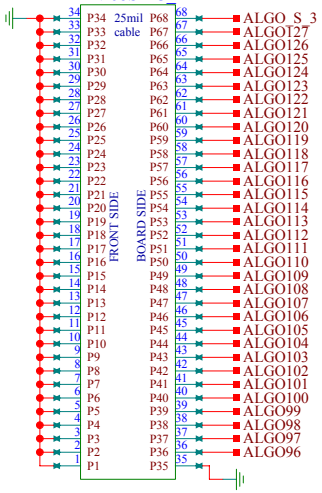
ERNI68SMC_B



ALGO[191:160]

CON127_96

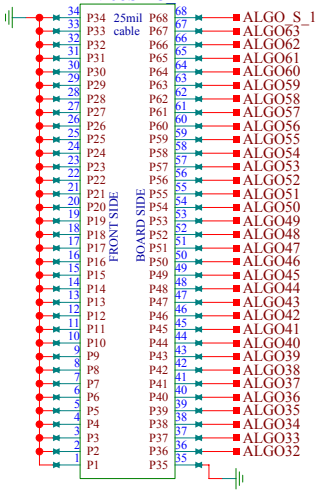
ERNI68SMC_B



ALGO[127:96]

CON63_32

ERNI68SMC_B



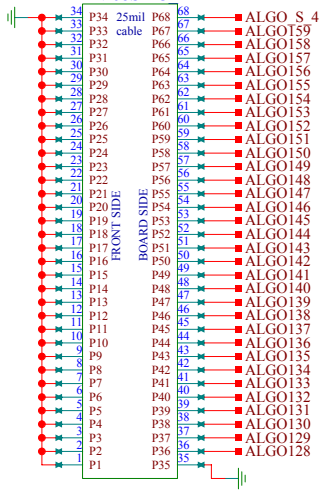
ALGO[63:32]

ALGO[191:0]

ALGO_S_[5:0]

CON128_159

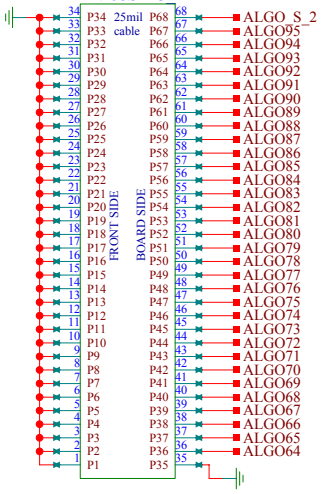
ERNI68SMC_B



ALGO[159:128]

CON95_64

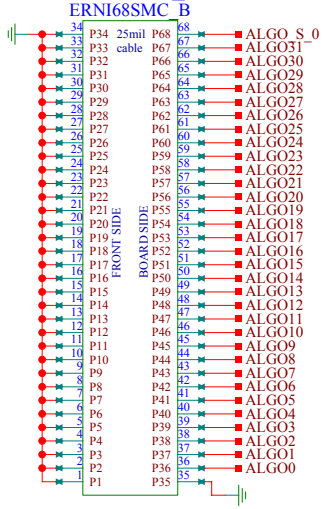
ERNI68SMC_B



ALGO[95:64]

CON31_00

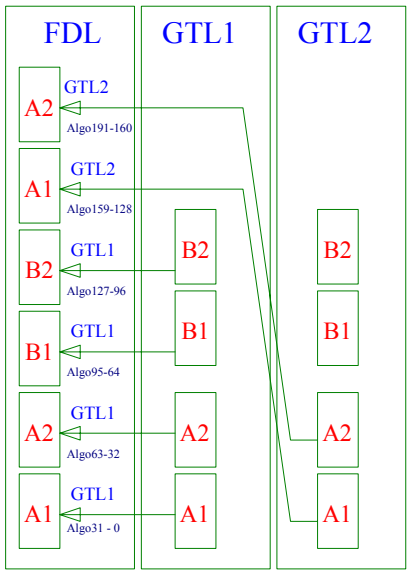
ERNI68SMC_B



ALGO[31:0]

lowest connector

Front Panel cables

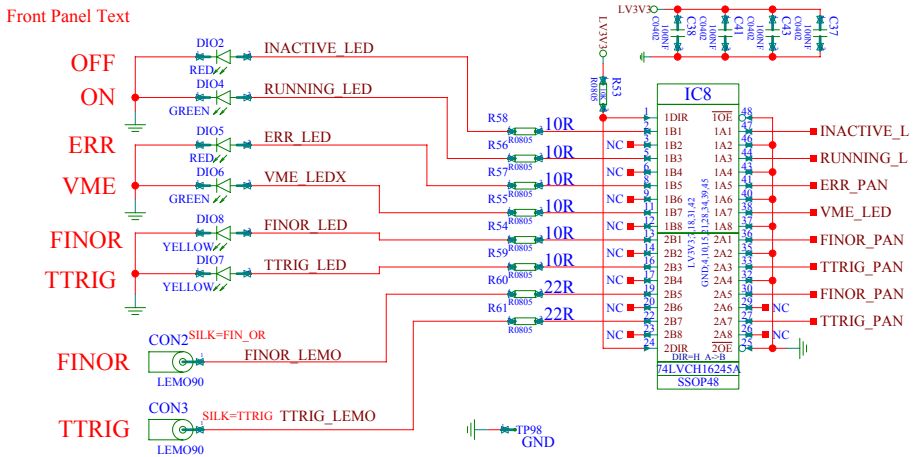


DISPLAY

leds mounted above all connectors on frontpanel

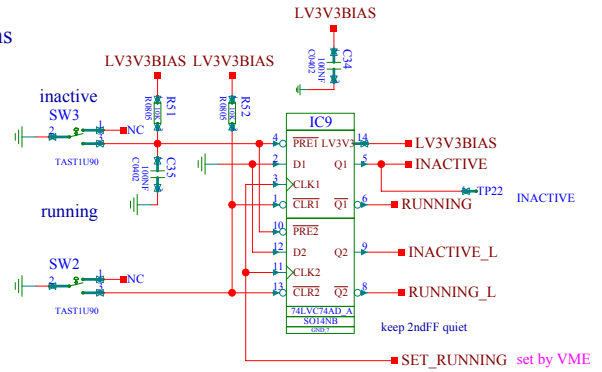
Front Panel Text

OFF
ON
ERR
VME
FINOR
TTRIG



INTERLOCK

Front Panel buttons



Changed to 3.3V chip

Frontpanel

DR1 DRILL_2P8 DR2 DRILL_2P8 DR3 DRILL_2P8 DR4 DRILL_2P8 DR5 DRILL_2P8 DR6 DRILL_2P8

Rail

X5 DRILL_2P8 X4 DRILL_2P8 X3 DRILL_2P8 X2 DRILL_2P8

Front Panel space for 9U: >300 mm

ERNI68B 48 mm

FDL-9U-CARD

FRONT_PAN_FDL

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: AT, OCT03	5-14-2004_10:03
checked by: AT+MP	110504

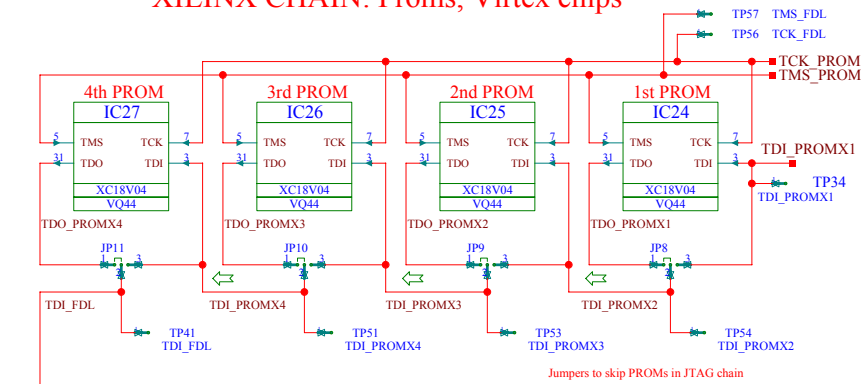
The Virtex chips are mounted on mezzanine boards.
==>There is no JTAG hetero symbol for Virtex chips.

JTAG: Xilinx Config. options: VME, Par_CableIV, Bridge-backplane
JTAG: Altera Config. options: Master Blaster, Bridge-backplane
FDL chip: also directly by VME

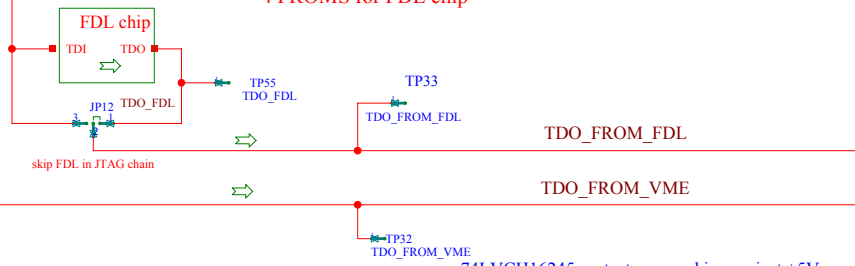
2 4 6 8 10 12 14
1 3 5 7 9 11 13
JTAG_CON_XIL TOP VIEW

JMP 1-2 =ON //configure XILINX chips by VME
JMP 2-3 =ON //configure XILINX chips by PAR_CABLE IV

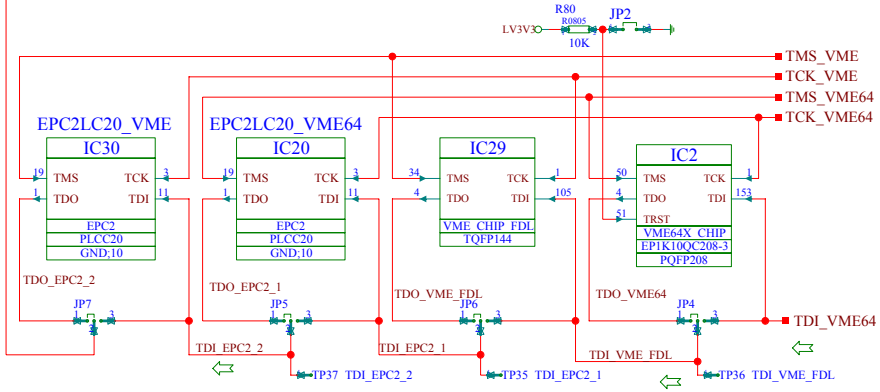
XILINX CHAIN: Proms, Virtex chips



4 PROMS for FDL chip



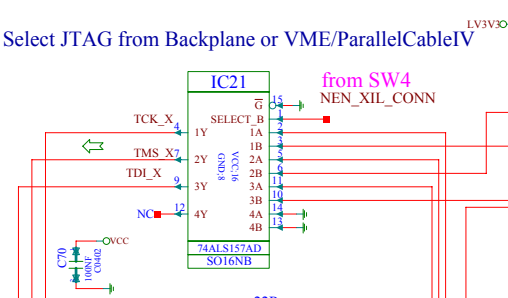
74LVCH16245 protects progr.chips against +5V.



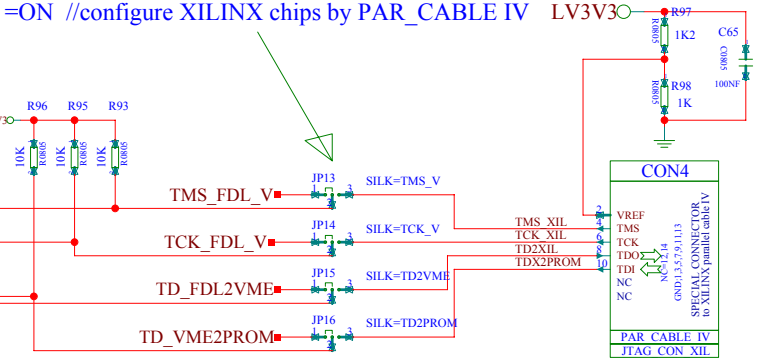
ALTERA CHAIN: Proms, EP1K10 = ACEX chips

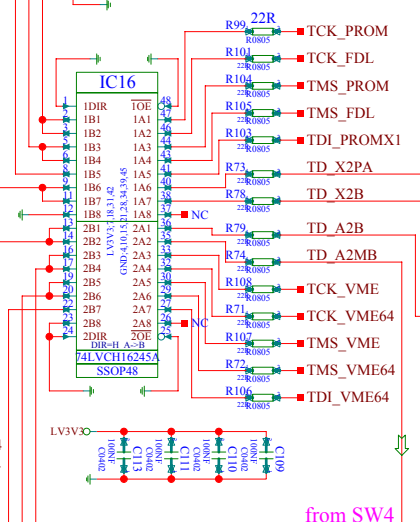
bypass capacitors for proms are on page CONF_FDL

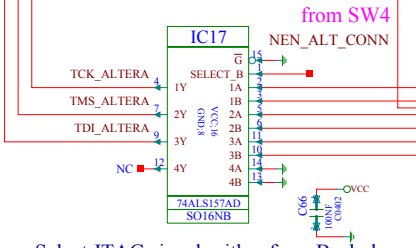
Select JTAG from Backplane or VME/ParallelCableIV

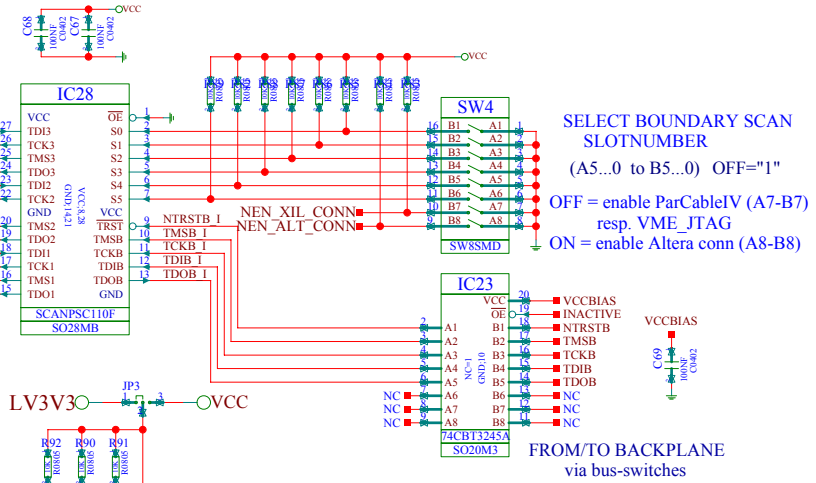


Select JTAG signals either from VME or from Parallel Cable IV









Run MasterBlaster either with 3.3 or 5V

2 4 6 8 10
1 3 5 7 9
JTAG_CON TOP VIEW

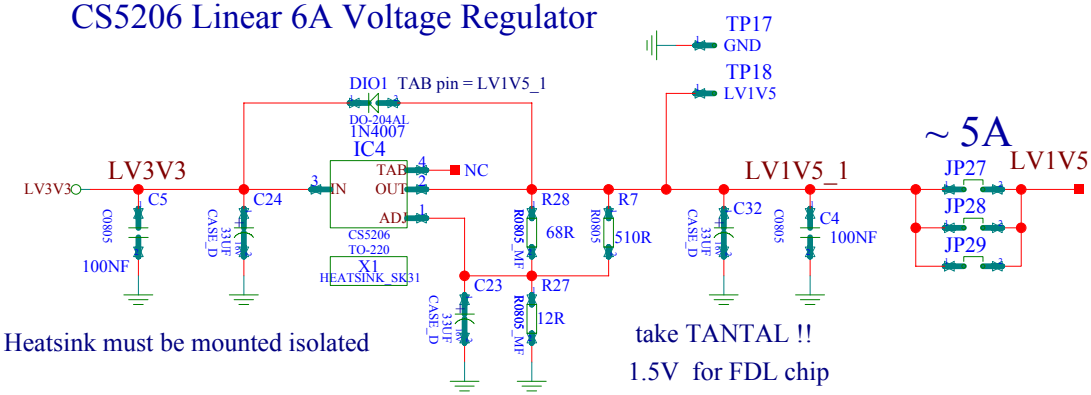
Select JTAG signals either from Backplane or from Master Blaster.

FDL-CARD-9U

JTAG_FDL

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: AT	10-13-2004_13:15
checked by: MP+AT	110504

CS5206 Linear 6A Voltage Regulator



Heatsink must be mounted isolated

take TANTAL !!

1.5V for FDL chip

V_ref

(1.240...1.254..1.266)V/68.1 = 18.2...18.4...18.6 mA >10mA

250 mV /(18.2...18.6 mA) = 13.73...13.44 Ohm

Adjust voltage with R131 = 475....562 Ohm

I_adj=54 uA...can be neglected

all resistors for CS5206 in metalfilm

FDL-CARD-9U

POWER_FDL

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: H. BERGAUER	5-17-2004_10:07
checked by: AT+MP	110504

Alternative Driver for RO-bus

LIVE INSERTION

SN74ABTE16245 HotSwap, incidentwave switching

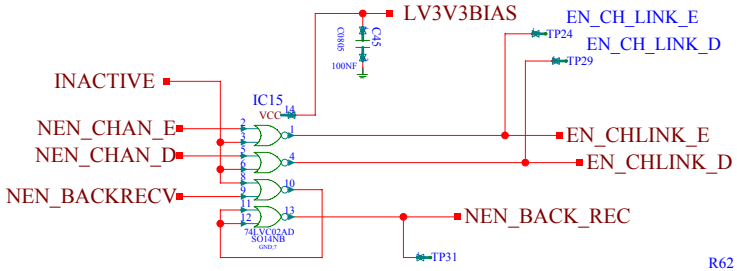
SN74ABTE16245 A-side=bus ETL, B-side=25ohm

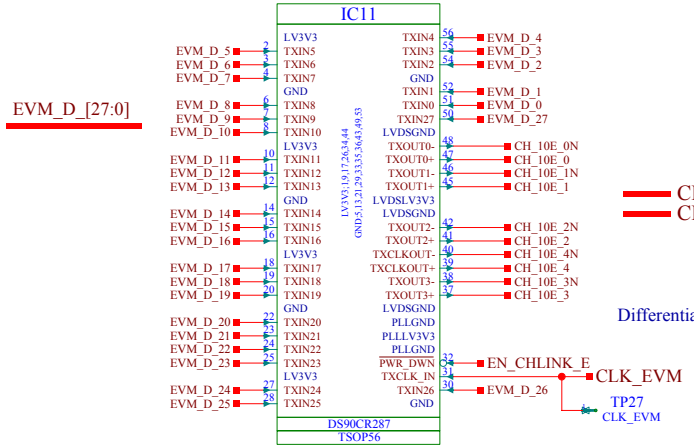
LVCH16245A: OUTPUTS not protected for live insertion [Vout<Vcc(instant.)+0.5V]

ABT,BCT,LVT: Vin<7V,Vout<5.5V, 3-state power-up circuit(Voff=2.5,1.8V)

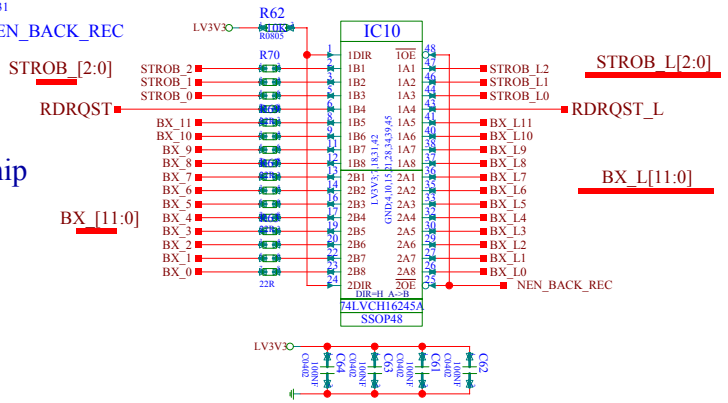
/OE with R-pullup to disable outputs at begin; later enable outputs by FPGA

serial termination for BX_...as protection against 5V

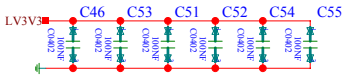


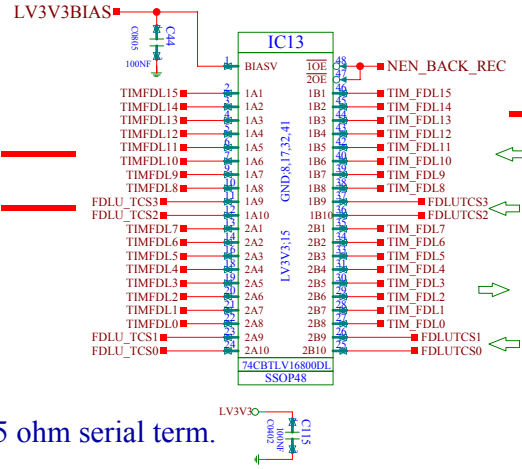


Differential Lines Zo=50 ohm ==> Zdiff =~100



to FDL chip

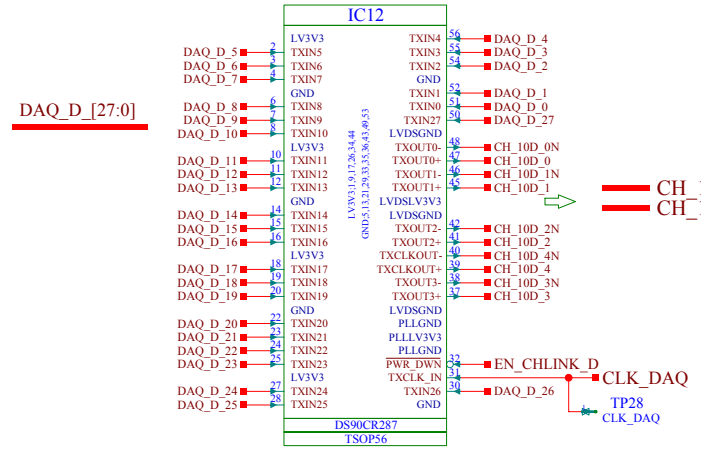




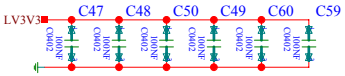
to/from backplane

FDLUTCS[3:0] =LVTTL

Differential Lines 2x50 ohm



to/from FDL chip with internal 25 ohm serial term.

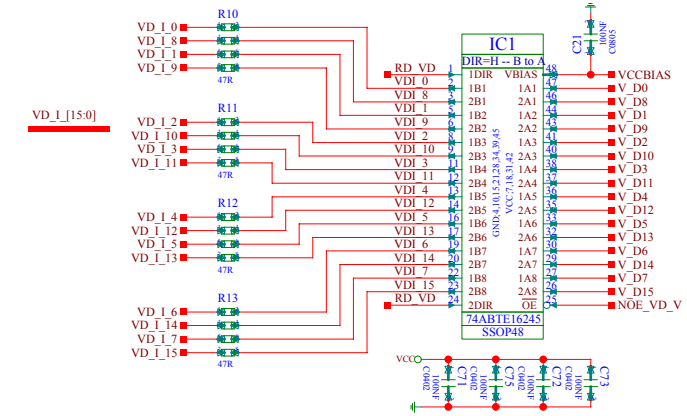


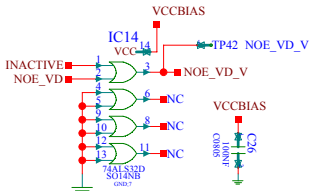
FDL-CARD-9U

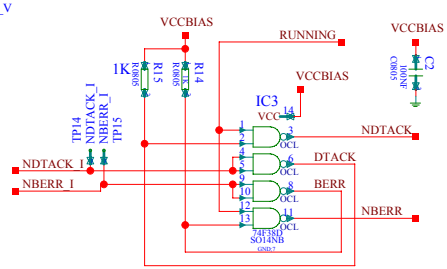
RO_CHLINK_FDL

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 1
modified by: A.T 3NOV03	5-11-2004_17:31
checked by: AT+MP	110504

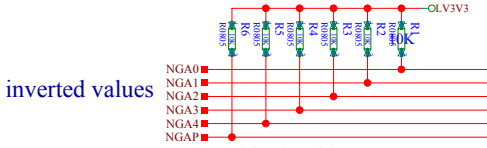
47 Ohm resistors protect the Virtex drivers against overvoltage spikes.







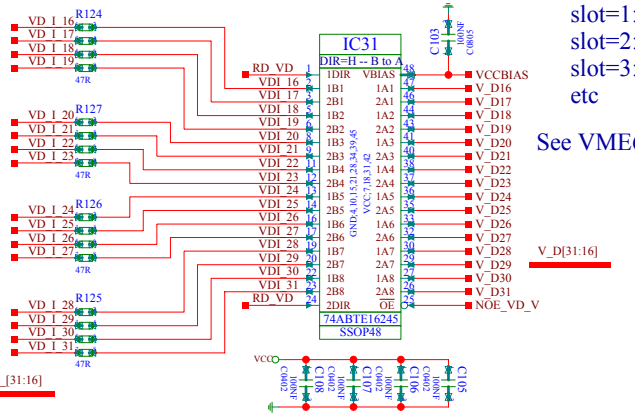
Keep NDTACK NBERR inactive while VME64X chip is unconfigured



inverted values

Geographical Addresses

47 Ohm resistors protect the Virtex drivers against overvoltage spikes.

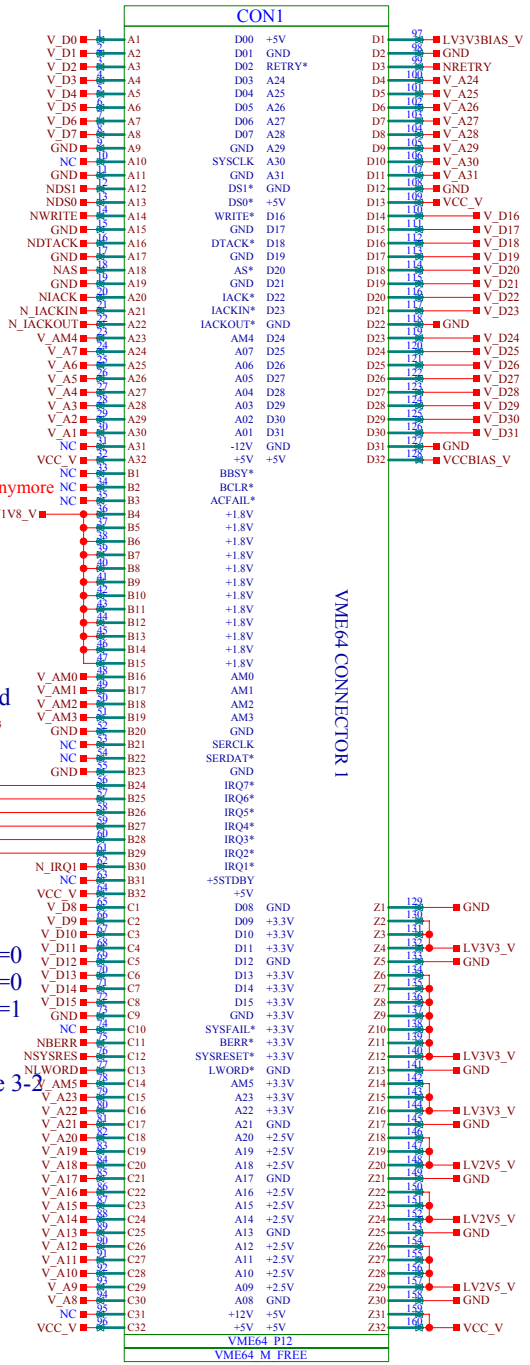


Parity bit: for odd parity

slot=1: GA=0 0001 => GAP=0
slot=2: GA=0 0010 => GAP=0
slot=3: GA=0 0011 => GAP=1
etc

See VME64x.pdf page 10 Table 3-2

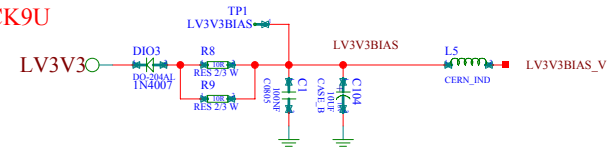
D1 = VCC on BACK6U
D1 = LV3V3bias on BACK9U

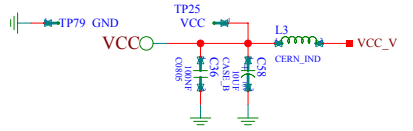


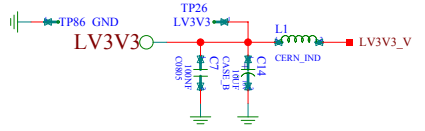
LV1V8_V not used anymore

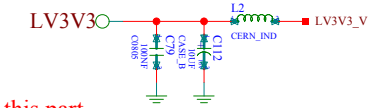
LV2V5_V not used anymore

FDL must not inserted into the 6U Backplane!!!



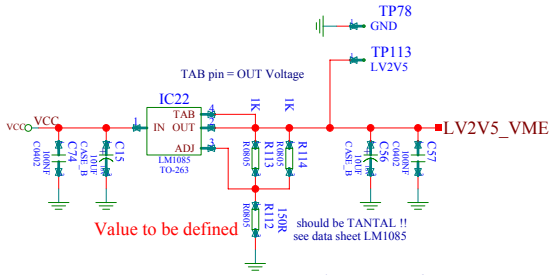






Do not solder this part.

Unused 2.5V plane can be connected to 3.3V optionally on 9U backplane if GTL-6U is not used anymore in Crate



Do not use LV2V5 and LV1V8 from BACKPLANE-6U

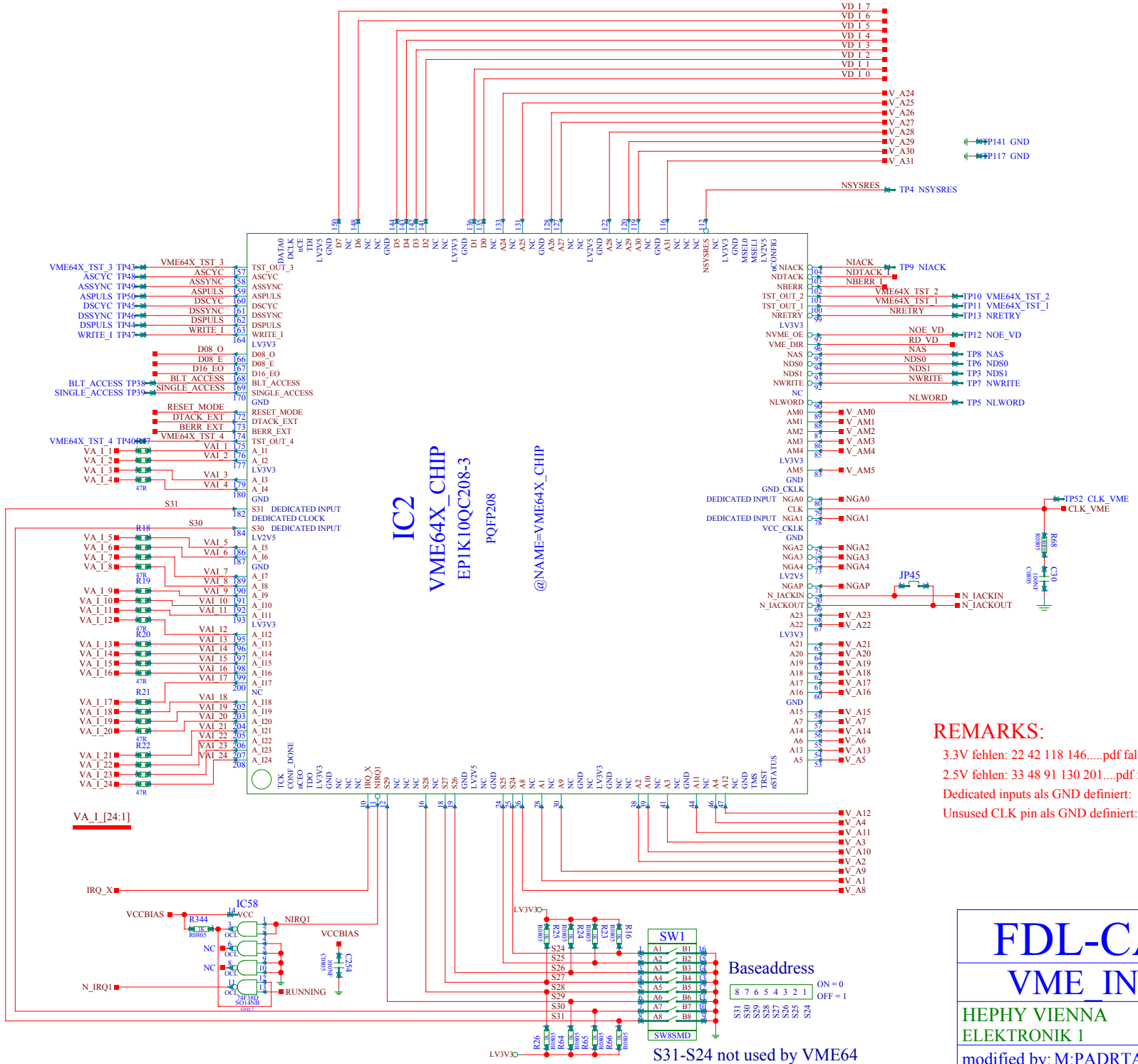
LV2V5 and LV1V8 will not be connected on the Backplane-9U

Stecker und Signale mit GTL und TIM schematic vergleichen

FDL-CARD-9U

VME_INTERFACE

HEPHY VIENNA ELEKTRONIK 1	sheet 1 of 3
modified by: H. BERGAUER	5-17-2004_10:14
checked by: A TAUROK	8-18-2003_16:53



REMARKS:

3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Referenz, HB 20080

2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Referenz, HB 200

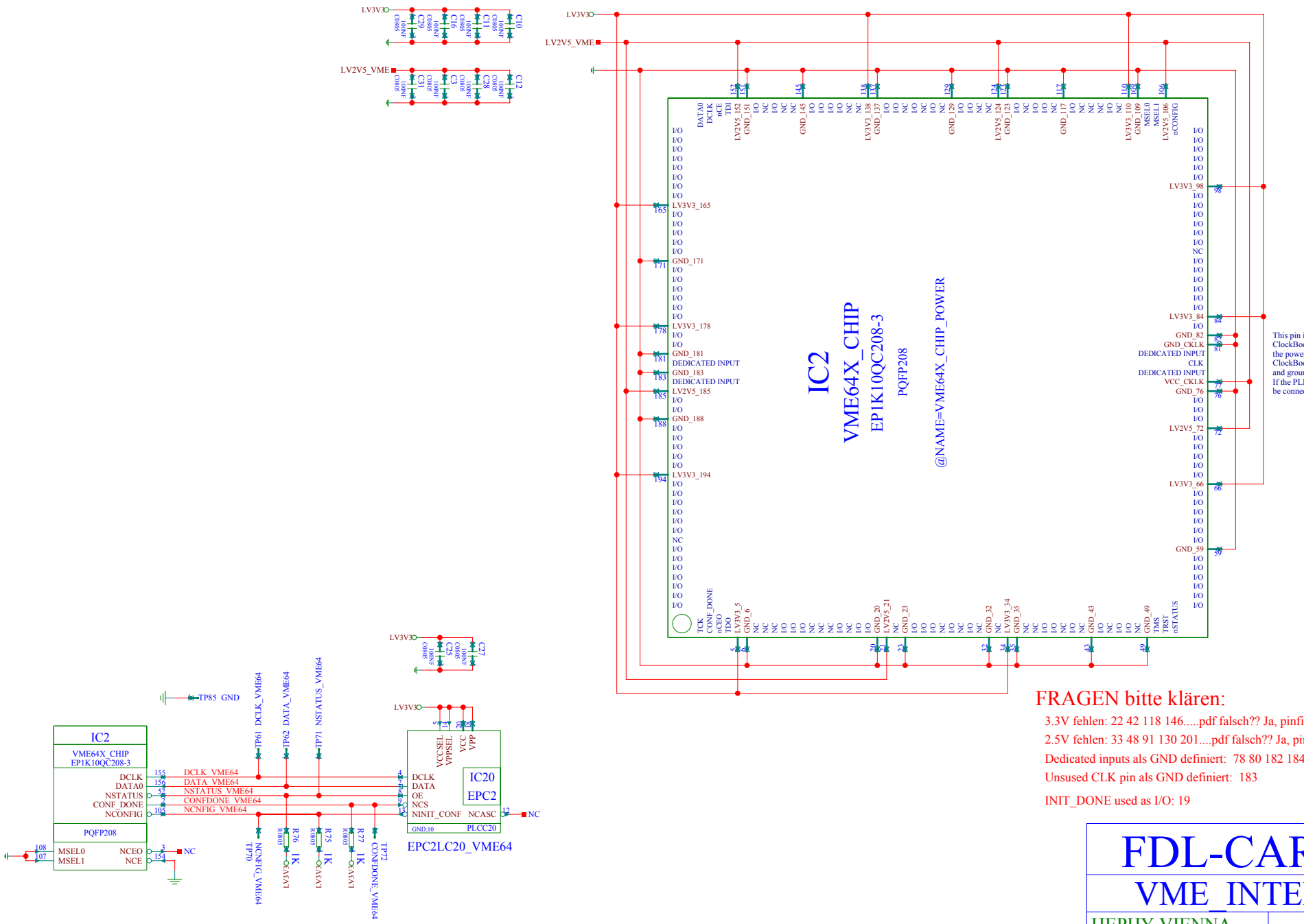
Dedicated inputs als GND definiert: 78 80 182 184

Unused CLK pin als GND definiert: 183

FDL-CARD-9U

VME_INTERFACE

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 3
modified by: M:PADRTA	5-11-2004_17:48
checked by: AT+MP	110504



A.T. Aug03: See configdevices.pdf:
Do not insert R75, R76, R77 when internal pullup R are used in IC20: EPC2
All pull-up resistors are 1 k.

FRAGEN bitte klären:

3.3V fehlen: 22 42 118 146.....pdf falsch?? Ja, pinfile ist Referenz, HB 200803

2.5V fehlen: 33 48 91 130 201....pdf falsch?? Ja, pinfile ist Referenz, HB 200803

Dedicated inputs als GND definiert: 78 80 182 184

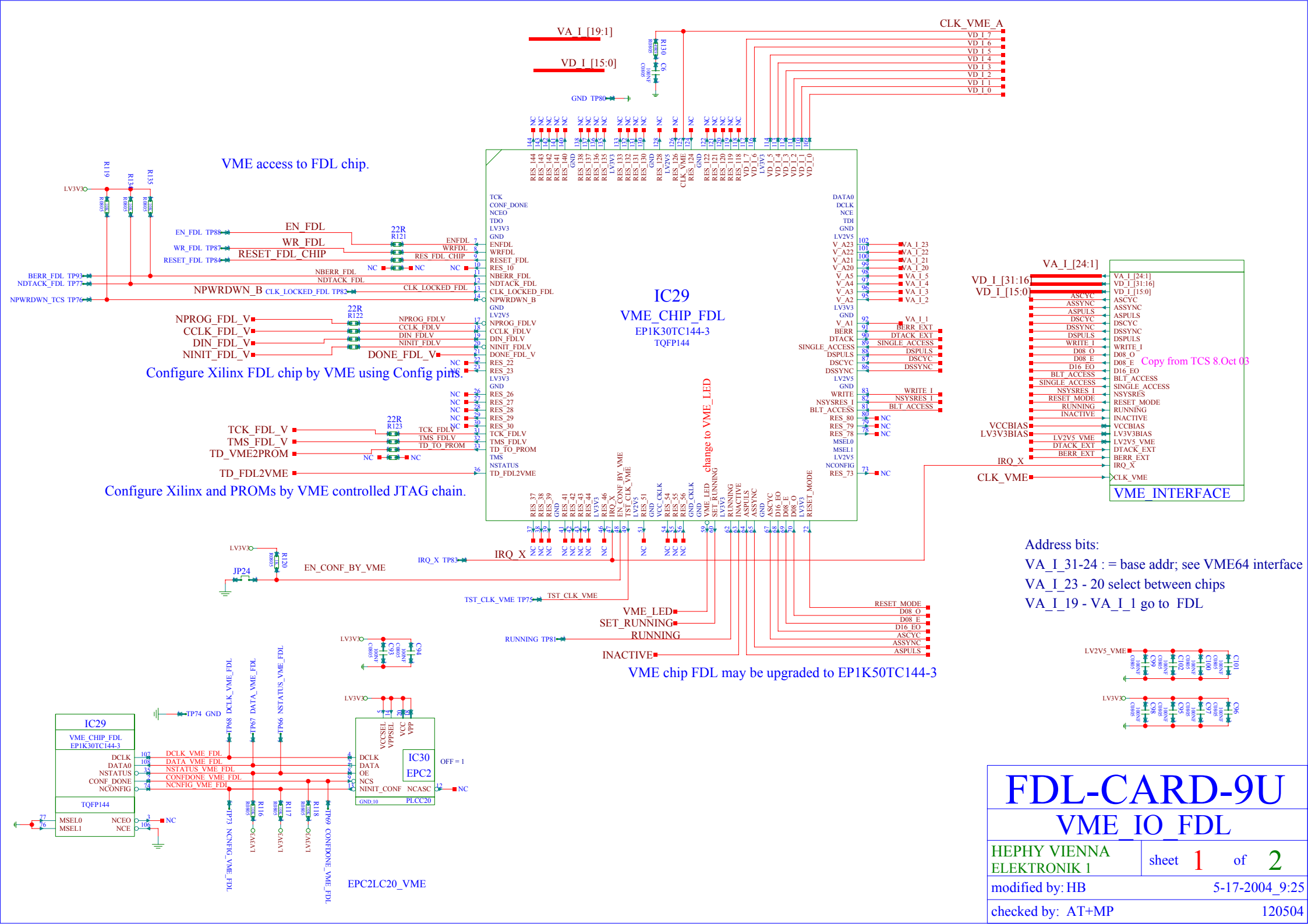
Unsused CLK pin als GND definiert: 183

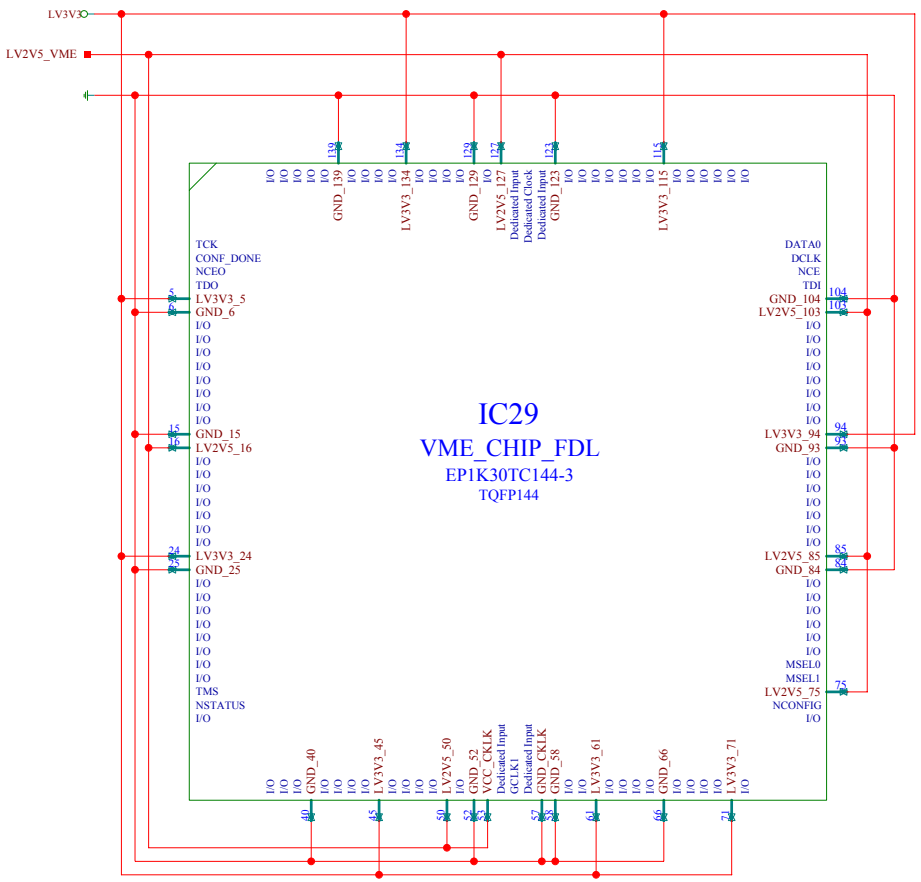
INIT_DONE used as I/O: 19

FDL-CARD-9U

VME_INTERFACE

HEPHY VIENNA ELEKTRONIK 1	sheet 3 of 3
modified by: H. BERGAUER	5-11-2004_17:54
checked by: AT+MP	110504

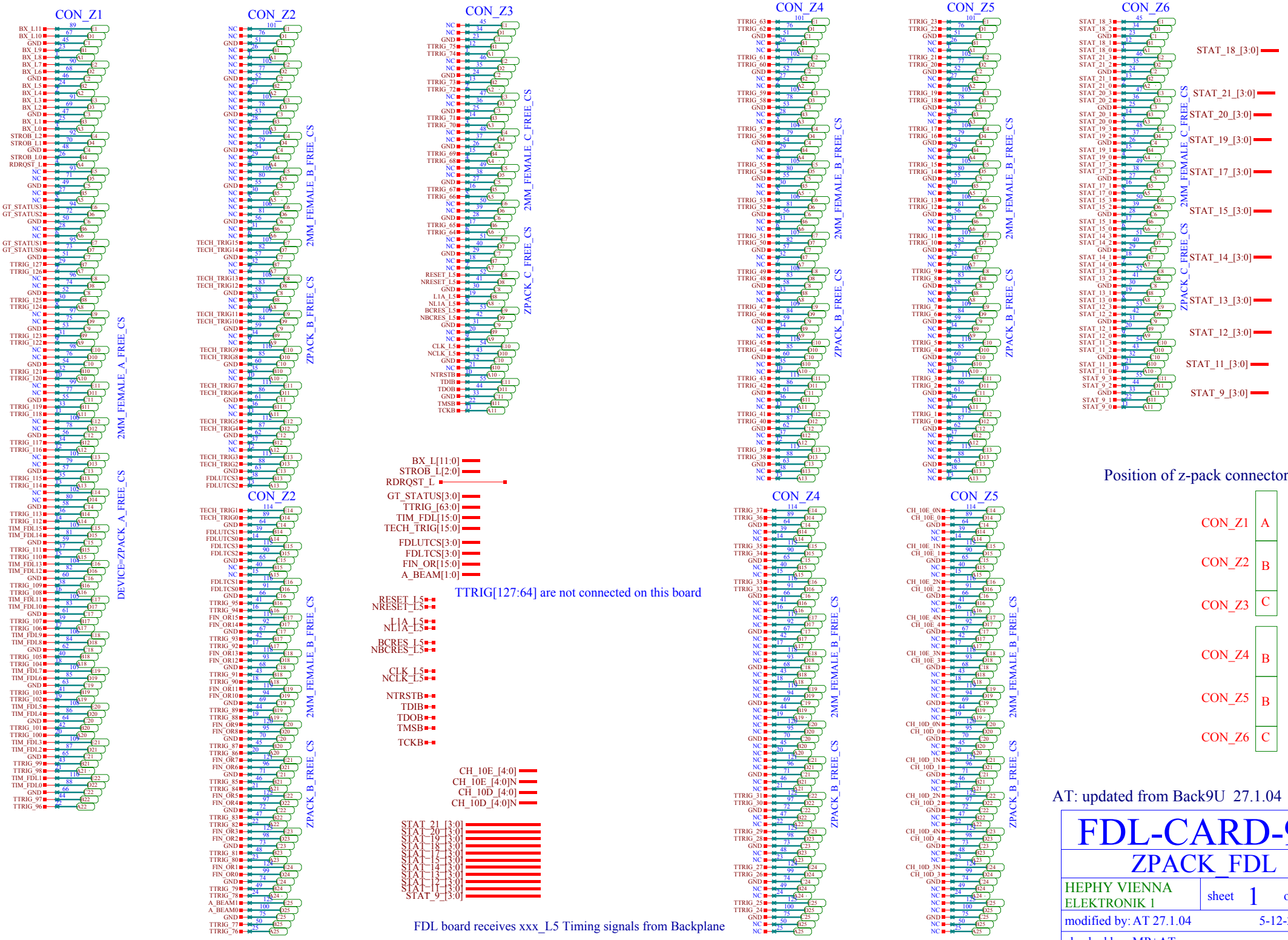

VME access to FDL chip.
IC29
VME_CHIP_FDL
EP1K30TC144-3
TQFP144
Configure Xilinx FDL chip by VME using Config pins.
Configure Xilinx and PROMs by VME controlled JTAG chain.
change to VME_LED
VME chip FDL may be upgraded to EP1K50TC144-3
VA_I [19:1]
VD_I [15:0]
CLK_VME_A
VA_I [24:1]
VD_I [31:16]
VD_I [15:0]
VME_INTERFACE
Copy from TCS 8.Oct 03
EN_FDL
WR_FDL
RESET_FDL_CHIP
NPROG_FDL_V
CCLK_FDL_V
DIN_FDL_V
NINIT_FDL_V
DONE_FDL_V
TCK_FDL_V
TMS_FDL_V
TD_VME2PROM
TD_FDL2VME
IRQ_X
EN_CONF_BY_VME
TST_CLK_VME
VME_LED
SET_RUNNING
RUNNING
INACTIVE
CLK_VME
Address bits:
VA_I_31-24 : = base addr; see VME64 interface
VA_I_23 - 20 select between chips
VA_I_19 - VA_I_1 go to FDL
IC30
EPC2
PLCC20
EPC2LC20_VME
FDL-CARD-9U
VME_IO_FDL
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 2
modified by: HB 5-17-2004_9:25
checked by: AT+MP 120504



FDL-CARD-9U

VME_IO_FDL

HEPHY VIENNA ELEKTRONIK 1	sheet 2 of 2
modified by: HB	5-17-2004_9:25
checked by: AT+MP	120504


CON_Z1
CON_Z2
CON_Z3
CON_Z4
CON_Z5
CON_Z6
2MM_FEMALE_A_FREE_CS
DEVICE=ZPACK_A_FREE_CS
2MM_FEMALE_B_FREE_CS
ZPACK_B_FREE_CS
2MM_FEMALE_C_FREE_CS
ZPACK_C_FREE_CS
BX_L[11:0]
STROB_L[2:0]
RDRQST_L
GT_STATUS[3:0]
TTRIG_[63:0]
TIM_FDL[15:0]
TECH_TRIG[15:0]
FDLUTCS[3:0]
FDLTCS[3:0]
FIN_OR[15:0]
A_BEAM[1:0]
TTRIG[127:64] are not connected on this board
RESET_L5
NRESET_L5
L1A_L5
NL1A_L5
BCRES_L5
NBCRES_L5
CLK_L5
NCLK_L5
NTRSTB
TDIB
TDOB
TMSB
TCKB
CH_10E_[4:0]
CH_10E_[4:0]N
CH_10D_[4:0]
CH_10D_[4:0]N
STAT_21_[3:0]
STAT_20_[3:0]
STAT_19_[3:0]
STAT_18_[3:0]
STAT_17_[3:0]
STAT_15_[3:0]
STAT_14_[3:0]
STAT_13_[3:0]
STAT_12_[3:0]
STAT_11_[3:0]
STAT_9_[3:0]
FDL board receives xxx_L5 Timing signals from Backplane
Position of z-pack connectors
CON_Z1 A
CON_Z2 B
CON_Z3 C
CON_Z4 B
CON_Z5 B
CON_Z6 C
AT: updated from Back9U 27.1.04
FDL-CARD-9U
ZPACK_FDL
HEPHY VIENNA
ELEKTRONIK 1
sheet 1 of 1
modified by: AT 27.1.04
5-12-2004_11:44
checked by: MP+AT
120504